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矽鍺量子點奈米級記憶元件及陣列之製作與研究(1/3)

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矽鍺量子點奈米級記憶元件及陣列之製作與研究

Study and Fabrication of SiGe Quantum Dots Memory Device and arrays

計畫編號：NSC 93-2215-E-002 -015-

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一、中文摘要

今日 MOSFET 已經佔有超過 88%的 IC 市場比例；原因是 MOSFET 能縮小到比其它形式的元件更小的尺寸，使其成為 IC 的主要元件。當單電子的電晶體，其以量子效應取代古典電荷的傳輸原理。在此，量子效應的穿隧將單一電子的量化電荷規則化。

目前記憶體元件之特性乃是利用將電子儲存於浮動閘極中，藉由臨界電壓的位移來判別記憶與否。由於微影、膠體化學與磊晶成長的進步，本計畫擬採用半導體或金屬材料來製作量子點，並藉由量子點可儲存電子的特性來取代浮動閘極，達到應用於記憶體元件的目標。

本計畫分三階段進行，第一階段主要目摽為量子點製程，製作 MOS 結構以作電容、電流等電性量測；第二階段為製程記憶體元件，對其做電性及可靠度等相關記憶元件特性的量測；第三階段為製作 EEPROM，並做電性及光電特性的量測。

關鍵詞：量子點、單電子記憶體、奈米結構。

二、本年度計畫緣由與目的

Most of modern non-volatile memory devices are based upon the electron storage in the so-call “floating gate” underneath the MOS gate. The 1 or 0 bit can then be memorized and differentiated by telling the threshold voltage shift of this MOS transistor. The development of modern porous materials, polymer science and epitaxial technology has been rapidly progressing recently. The project is proposed to apply the nano-scale semiconductors in the floating gate memories.

Three major quantum dots or wires

including MOCVD and E-Bean Writer achieved SiGe QD. It will be applied in the planer-type MOS memory cells for this research.

First of all, simple metal-insulator-semiconductor (MIS) structures will be fabricated to measure and analyze their electrical characteristics using standard current-voltage and capacitance-voltage measurements. The study of their capabilities in charge trapping and long term storage will be followed. After optimization of the MIS structures, the quantum dot memory cell will be studied in terms of its program, erase and read characteristics. The reliability and compatibility with existing thin process of these memory cells will be further evaluated finally.

In the first year of this research, we focus on the fabrication of fundamental structure of memory devices, and its basic memory characterization. The key points of this structure are the growth of high quality tunneling oxide and the fabrication of high density and uniform quantum dots layer. Besides the SiGe semiconductor-material dots, we use gold dots to be compared. In order to make electrical test, we fabricate the MOS structure. We make typical C-V (capacitance- voltage) test and measure its C-V curve to confirm its memory characterization.

三、執行進度

1. Ge nano-dots growth

We present an extensive study about the formation of SiGe dots on SiO_2. The formation of Ge dots in this work is grown in commercially CVD system, the Sirius 400 UHVCVD of Unaxis. The SiGe dot fabrication sequence is as follows: a 3-nm-thick tunneling oxide layer is grown on a (100)-oriented p-type Si substrate via rapid thermal oxidation (RTO). Before the RTO of SiO_2, Si wafers were cleaned by RCA process. The SiO_2 on Si wafers sent to the loading chamber which is pumped down to 10^{-6} torr were transferred in reactor of UHVCVD. Pure silane (SiH_4) is used as Si source precursor and germane (GeH_4) as the Ge source gas. The UHVCVD is hot-wall processing at 550^{o}C growth temperature. A series of experiments were studied at deposition time of 30mins, 120mins, and 150mins. The evolution of the Ge dots has been observed by SEM (show as Fig.1.). We found that the density of Ge dots were larger as the deposition time was longer. By continually accumulating the Ge atoms, the dot size is larger as the time evolution. The size distribution was inhomogeneous, and was difficult to control. So the advanced research and study of Ge dots growing on SiO_2 are required and continued.

2. Gold nano-dots MOS

Fig.2. shows our basic structure, including the P-type substrate, thermal oxide, nano-dots layer, control oxide, and contacts. In order to gate the tunneling characterization, we design two kinds of thickness, 3nm and 6nm. In the part the nano-dots layer, we fabricate different types of materials of dots. Besides the initial SiGe

nano-dots, we also use gold nano-dots to make comparisons. We believe that these two different types of material have different carrier transports mechanism, and we will make further study and research about it. On the nano-dots layer we design a control oxide layer about 40nm to prevent carrier tunneling to the gate. After the basic structure is accomplished, we make the contacts on the top and bottom to fabricate MOS structure. A typical high frequency C-V measurement is tested by HP4284A.

First, we grow the tunneling oxide layer. The silicon wafer is cleaned in standard RCA recipes, dipped in 10% hydrofluoric acid, rinsed in de-ionized water and dried, followed by a thermally grown 3/6nm-thick dry SiO_2 layer as a tunneling oxide on p-type (100) silicon substrate at 950^{o}C.

In the part of fabrication of gold nano-dots layer, we apply chemical process. We use gold nano-particle solution which is synthesized by chemical process. First we use clean the organic contaminant with reactive ion etching (RIE) system. Then, chemical surfactant is coated on the tunneling oxide. After several minutes the surface of tunneling oxide will be stuck with negative charged organic molecules. Then we spray the gold nano-particle solution. After waiting about 1hours the gold particles adhered with positive charged molecules combine with the initial negative charged molecules, and they indirect attach on the surface of tunneling oxide. At last we use RIE system again to clean the residual organic molecules and the nano-dots layer is accomplished.

We take SEM pictures of the gold nano-dots layer and measure their shape, dimensions, and density (show as Fig.3.). These gold nano-dots are almost round shape. Their diameter is about 20nm and has very small difference. The distribution of particle is random but the total number on a large enough area is uniform. The density of gold particles are about 10^{10} per centimeter square.

Finally the nano-dots layer capped with 44nm control oxide with plasma enhanced chemical vapor deposition (PECVD) system and 300nm Al gate deposition complete the gate stack formation of MIS capacitor. Last the samples are thermally annealed at 400^{o}C in either pure N_2 or forming gas (90%N_2 + 10%H_2) ambient.

The cross-sectional high resolution transmission electron microscope (HRTEM) of an oxide/Au nano-dots/oxide stacked structure is also show in Fig.4. It is clearly shown the Au nano-dots are embedded between tunnel oxide and control oxide, which are confirms the uniform size distribution of Au nano-dots of diameter nearly 18nm. Additionally we also fabricate a sample without gold particle to be a comparison.

3. 量測結果及討論

In the part of SiGe nano-dots devices, we still try to fabricate higher quality nano-dots layer. About these previous fabricated devices, their measurement data

are unstable and not complete. We still need to put more efforts on its fabrication.

In the part of gold nano-dots devices, Fig.5. shows the hysteresis curve of capacitance-voltage (C-V) measurement after a bias from -10V to +10V. All samples were held for 30 s at -10V before being swept to +10V and then held at this voltage for 30 s before returning to -10V. The holding time ensure that the structure are fully charged or discharged by the holding bias before commencement of the C-V sweep and any change in the sweep rate would not affect the flatband voltage shift, as evidenced by Yong Kim et al. The C-V hysteresis shows a significant threshold -voltage shift up to 1.7V, which is enough to be defined as 1 or 0 for the circuit design. The trapped charge density can be electrically calculated through the threshold-voltage shift by $\triangle V_t = Q_t \times t_{control} / \varepsilon_{ox}$. Q_t is the density of trapped charge(C/cm2 in unit) in Au nano-dots. Setting $t_{control}$ = 44nm, $\triangle V_t$ = 1.7V in sample A, and ε_{ox} = 3.9×8.885 × 10^{-14} F/cm, the number of electrons trapped in the Au nano-dots was calculated to be 8.36 × 10^{11} cm^{-2}. It is indicated the every Au nano-dots trapped almost close to 70 electrons, due to the Coulomb blockade effect.2 The sample B shown the $\triangle V_t$ = 2.48V with the thinner tunneling oxide owning close to 100 electrons to be calculated.

In this work, several oxide stacked structure embedded with Au nano-dots has been demonstrated for application in memory devices. The deeper potential well of metal nano-dotls shows large charge storage and long retention time than Si nano-dots device has been reported. Our results also show the low operating voltage to achieve the memory window up to 1.7V(2.48V), which is enough to be applied in memory device.

四、總結

We have successfully designed and fabricated MIS device with gold nano-dots layers. The SiGe nano-dots layer also gets preliminary achievement. Our devices with gold nano-dots layer shows high storage capacity and operation at low bias voltage. Our further work is to fabricate dot layer with higher density and focus on its electric characterization and reliability issue.

五、圖表及註解

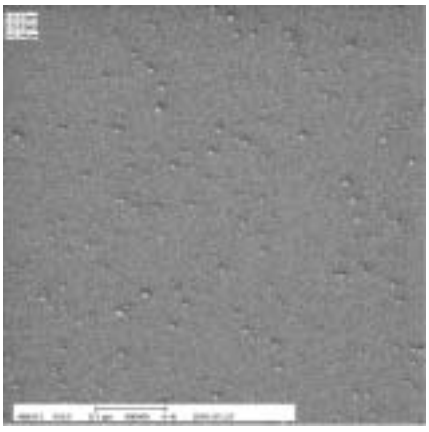

Fig.1.(a).

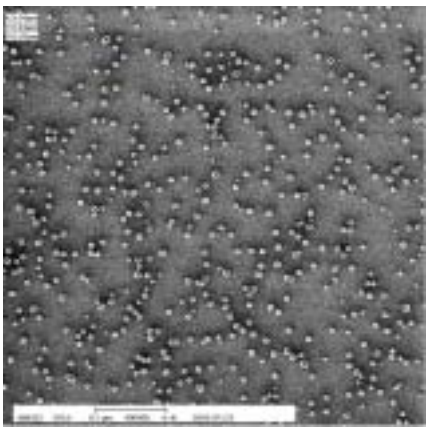

Fig.1.(b).

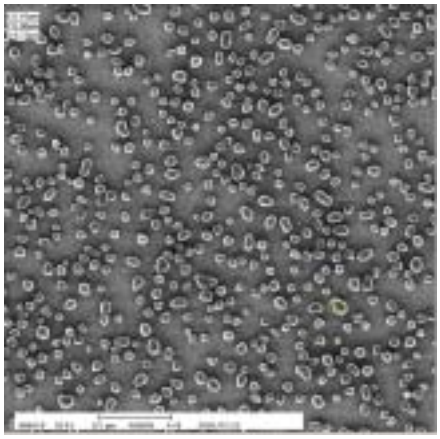

Fig.1.(c).

Fig.1. SEM picture of SiGe nano-crystal layer grown with UHVCVD with different operation parameters and time. (a) is grown during 30 minutes; (b) is grown for 120 minutes; (c) is grown for 150 minutes.

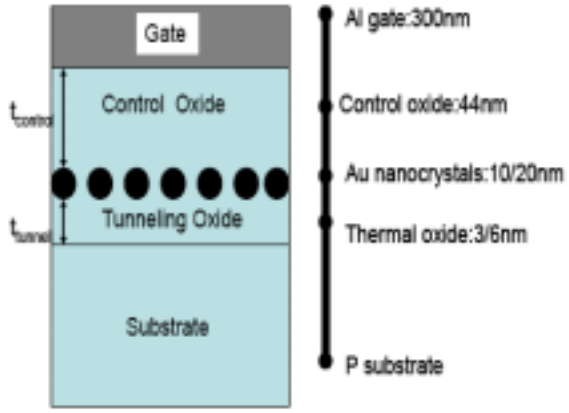

Fig.2. Schematic cross section of MOS capacitor with Au nano-dots.

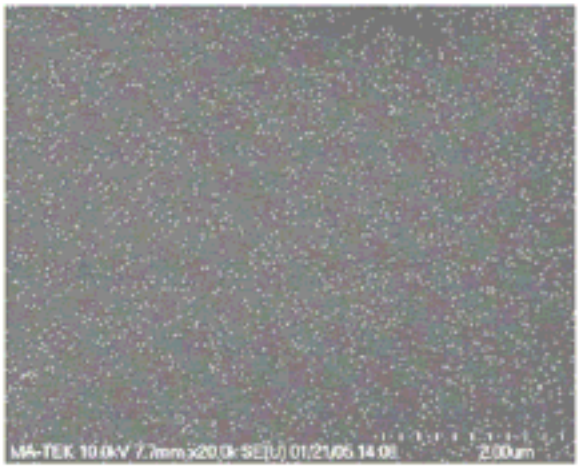

Fig.3. SEM picture of typical Au nano-dots deposited on SiO_2 with a density of 1.2×10^{10} cm^{-2}.The mean size is equal to 20nm.

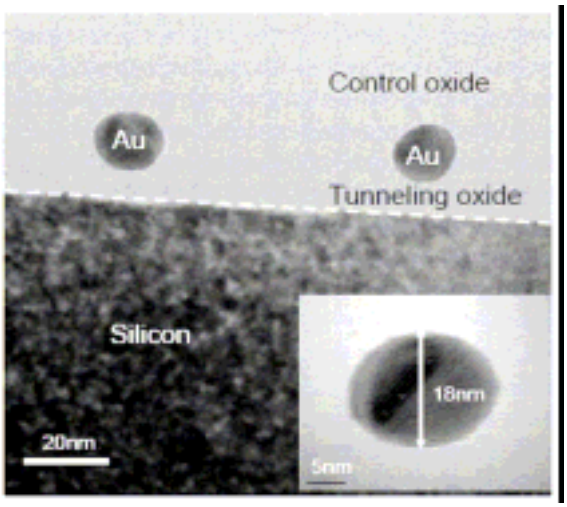

Fig.4. Cross-sectional HRTEM of stack structure and showing single Au nano-dot of diameter nearly 18nm.

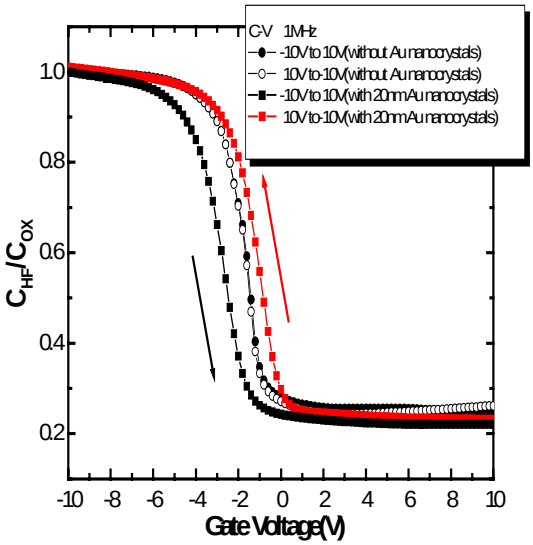

Fig.5. Typical high-frequency C-V characteristics of MOS capacitor incorporated Au nano-dots.

六、參考文獻

1. S. Tiwari, F. Rana, K. Chan, H. Hanafi, W. Chan, and D. Bbuchanan, in IEDM Tech. Dig (1995) 521.
2. Y. Shi, K. Saito, H. Ishikuro, and T.

Hiramoto, J. Appl. Phys. 84 (1998) 2358.
3. E. W. H. Kan, W. K. Choi, and W. K. Chim, J. Appl. Phys. 95 (2004) 3148.
4. T. C. Chang, S. T. Yan, C. H. Hsu, M. T. Tang, J. F. Lee, Y. H. Tai, P. T. Liu and S. M. Sze, Appl. Phys. Lett. 84 (2004) 2581.
5. R. Ohba, N. Sugyama, K. Uchida, J. Koga, and A. Toriumi, in IEDM Tech. Dig. (2000) 313.
6. C. Lee, A.Gorur-Seetharam and E. C. Kan, IEDM Tech. Dig. (2003) 557.
7. T. C. Chang, P. T. Liu, S. T. Yan and S. M. Sze, Electrochem. Solid-State Lett. 8(3) (2005) G71.
8. J. J. Lee and D. L. Kwong, IEEE Trans. Electron Devices 52 (2005) 507.
9. M. Takata, S. kondoh, T. Sakaguchi, H. Choi, J-C. Shim, H. Kurino and M. Koyanagi, IEDM Tech. Dig. (2003) 553
10. Z. Liu, C. Lee, V. Narayanan, G. Pei, and E. C. Kan, IEEE Trans. Electron Devices 49 (2002) 1606.
11. S. F. Hu, R. L. Yeh and R. S. Liu, J. Vac. Sci. Technol. B 22(1) (2004) 60
12. Y. Kim, H. J. Cheong, K. H. Park, T. H. Chung, H. J. Bark, J. Yi, S. H. Bang and J. H. Cho, Semicond. Sci. Technol. 17 (2002) 1039.
13. T. Feng, H. Yu, M. Dicken, J. R. Heath and H. A. Atwater, Appl. Phys. Lett. 86 (2005) 033103-1