Oxide Roughness Enhanced Reliability of MOS Tunneling Diodes

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I. Introduction

The Si/SiO_2 interface in metal-oxide-semiconductor field-effect transistors (MOSFETs) plays a major role in the electrical properties of inversion layer electrons. As oxide scaling down, the roughness of the gate oxide interface is no longer negligible. Several groups have reported the effect of interface roughness on device electrical performance. Some have found the interface roughness can degrade MOSFET channel mobility due to surface scattering [1,2]. Nakanishi et al. have proposed the surface roughness of interface will degrade the time-dependent dielectric breakdown (TDDB) characteristics of MOS capacitors, and large surface roughness enhances the tunneling current through the oxide [3]. We have reported the roughness enhanced electroluminescence efficiency in the MOS tunneling diodes [4]. In this paper, we investigate the interface roughness effect on oxide degradation in MOS tunneling diodes.

II. Experiments

The rougher Si/SiO_2 interface was achieved by very high vacuum prebake ($<3x10^{-6}$torr, maintained by a turbo pump) before the growth of ultrathin gate oxide, and the interface roughness was measured by atomic force microscopy (AFM). The ultrathin gate oxide of the MOS diode was grown by rapid thermal oxidation (RTO), and the oxide thickness was measured by ellipsometry. The MOS diodes have Al gate electrodes with circular areas defined by photolithography. The reliability measurement was carried out using an HP4156A semiconductor parameter analyzer.

III. Results and Discussion

The oxide roughness scattering can change the electron momentum and decrease the perpendicular electron energy as the electrons tunneling from the Al gate electrode impact the Si/SiO_2 interface of the NMOS diodes biased at negative gate voltage (accumulation bias). The electron impact energy perpendicular to the Si/SiO_2 interface is reduced, and thus the effective voltage acceleration factor decreases significantly. A rough NMOS diode with oxide roughness of 0.85nm and oxide thickness of 2.2 nm shows little gate voltage fluctuation under constant current stress of -30 A/cm^2 (Fig.1), while a flat NMOS diode with oxide roughness of 0.06 nm and oxide thickness of 1.3 nm shows serious gate voltage fluctuation (soft breakdown) under much smaller constant current stress of -3A/cm^2 (Fig.2). Fig. 3 shows the time evolutions of gate tunneling current for the flat and the rough PMOS tunneling diodes with the oxide thickness of 2.7 nm and 3 nm, respectively, under CVS at gate voltage (V_g) of 2V. The area size of devices is $3x10^{-4}$ cm^2. The flat PMOS device with the oxide roughness of 0.15 nm reveals degradation after ~2200 sec stress, while the rough PMOS devices with the oxide roughness of 1.46 nm shows very little gate current fluctuation under the same stress condition. Note that the rough device has a larger injection current density than the flat device under the same stress voltage. The two dimensional electrical field in the rough oxide is responsible for the gate current increase of the rough devices (Fig. 5 (a)). The hole can tunnel through the non-perpendicular path with larger electric field (ε_1). Fig. 4 shows the Weibull plot of the charge to breakdown (Q_{BD}) characteristics for both the flat and the rough PMOS tunneling diodes under CVS at V_g =2V. It is very clear that the oxide degradation starts much earlier in the flat devices as compared to the rough devices. The rough PMOS tunneling diodes reveal improved reliability than the traditional flat PMOS tunneling diodes. Two kinds of current components exist in the PMOS tunneling diodes. The electron current tunnels from Si conduction band to Al and the hole current tunnels from Al to Si valence band (Fig.5 (b)). The hole can break the Si-O bond [5] by the released energy as the

hole relaxes to the valence bandedge in Si, while the electron tunneling from Si to Al can not damage the Si/SiO_2 interface, since there is no excess electron energy at the Si/SiO_2 interface. In the PMOS devices with rough oxide, the injected holes tunneling from the Al gate to the silicon substrate are scattered by the rough Si/SiO_2 and Al/SiO_2 interfaces, and thus the hole momentum perpendicular to the interface is reduced. The perpendicular hole momentum seems crucial to break the Si-O bonds. The reduction of this momentum prevents the defect formation at Si/SiO_2 interface and leads to enhanced reliability in the rough devices. Since no deuterium isotope effect has been observed in the hole injection condition, the rough Si/SiO_2 interface may be a feasible method to improve the oxide reliability during the hole injection. Fig. 6 shows the speculative mechanism of the roughness-enhanced oxide reliability in PMOS tunneling diodes. However, more evidence is needed to understand the details of the enhancement mechanism. The AFM measurements show that both surface roughness and interface roughness have similar magnitude (Fig.7). A conformal growth of the oxide is assumed in the device modeling.

To further investigate the effect of oxide roughness on reliability, the light emission at bandgap energy [6] is measured. The time evolution of emission intensity in NMOS device for rough oxide has very slight variation during the stress time, while that for flat oxide degrades 20 % after 1400 sec stress (Fig.8). The similar results are also found in the PMOS devices (Fig. 9). The degradation of light emission indicates the formation of interface states, which act as non-radiative recombination centers. The current stress generates more interface states in the flat oxide than that in the rough oxide. The carrier scattered by the oxide roughness in the rougher devices have lower energy perpendicular to the interface (Fig. 6), and the formation of interface states becomes inefficient. The oxide roughness scattering can also provide the energy relaxation path for the high-energy electrons bombarding the Si/SiO_2 interface by radiative recombination [4], where the phonon and roughness scattering provide the required momentum (Fig.10). The rougher oxide has larger light emission efficiency due to roughness scattering (Fig.11). The gate current of the NMOS devices with rough ultrathin oxide (<3nm) also increases due to the two dimensional electric field (Fig. 5(a)). The roughness enhances the radiative recombination of the tunneling holes and the light emission efficiency increases with increasing oxide roughness (Fig. 11 & 12).

IV. Conclusion

The ultrathin oxide reliability is enhanced by introducing oxide roughness, which is responsible to the reduction of impact electron/hole energy perpendicular to the Si/SiO_2 interface, and the decrease of voltage acceleration factor. The rough oxide can be a novel technology to improve both the electrical and optical reliability of MOS devices.

Acknowledgments

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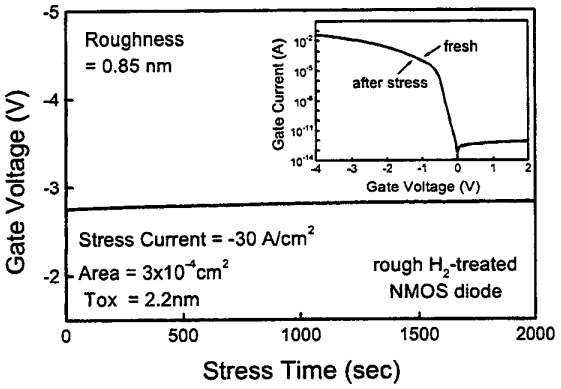

Fig. 1. The time evolution of gate voltage of the rough H_2-treated NMOS diode under $-30A/cm^2$ constant current stress. Due to the reduction of injected electron energy by oxide roughness scattering, soft breakdown is not observed after stress. The inset is the current-voltage curves before and after stress.

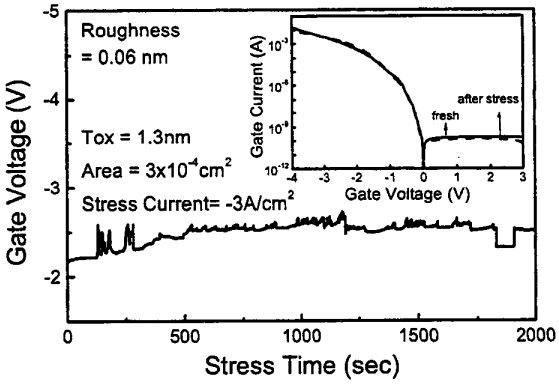

Fig. 2. The time evolution of gate voltage of the flat H_2-treated NMOS diode under $-3A/cm^2$ constant current stress. The device reveals soft breakdown after stress. The inset is the current-voltage curves before and after stress. Note that the stress current density is much smaller than that in Fig. 1.

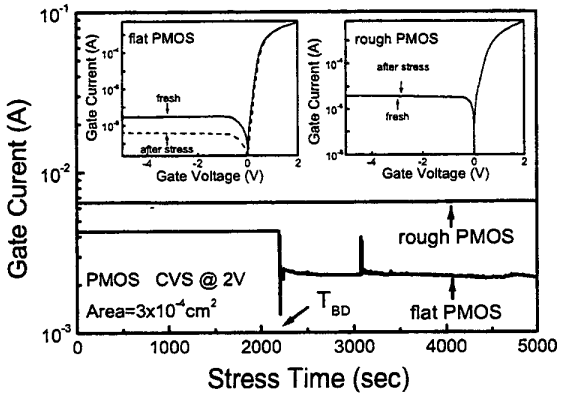

Fig. 3. The time evolutions of gate current of the flat and the rough PMOS tunneling diodes under 2V constant voltage stress. The insets are I-V curves before and after stress (left: the flat device, right: the rough device).

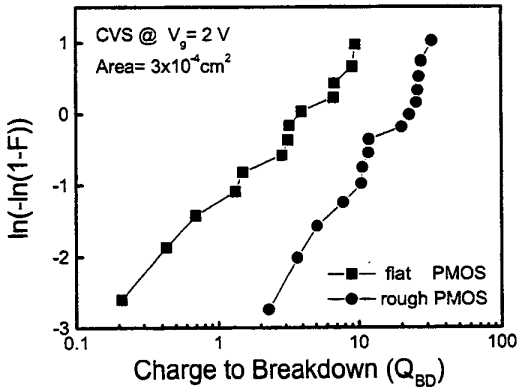

Fig. 4. The Weibull plot of the charge to breakdown (Q_{BD}) characteristics for the flat and the rough PMOS tunneling under CVS at V_g=2V.

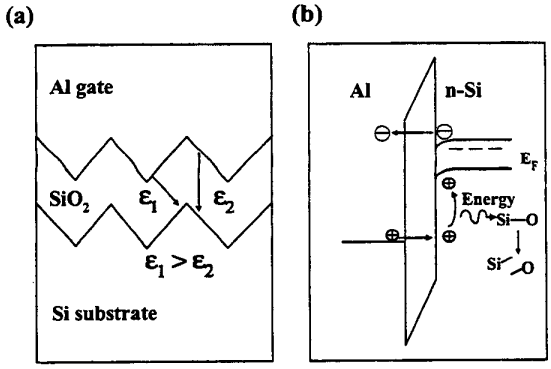

Fig. 5. (a) The illustration of two-dimensional electric field effect (ε_1) in the rough oxide to yield high current density, as compared to the flat devices. The hole can tunnel through the non-perpendicular path with larger electric field (ε_1). (b) The schematic current transport mechanism in the PMOS tunneling diode. The hole tunneling from the Al to silicon can break Si-O bonds by the released energy as the hole relaxes to the valance bandedge.

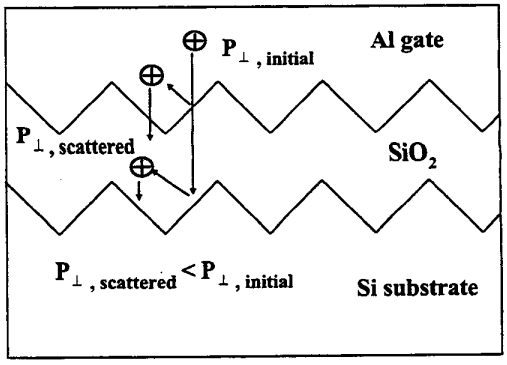

Fig. 6. The illustration of the speculative mechanism of the roughness-enhanced reliability. The hole impact energy perpendicular to the Si/SiO_2 is reduced due to the surface and interface roughness scattering.

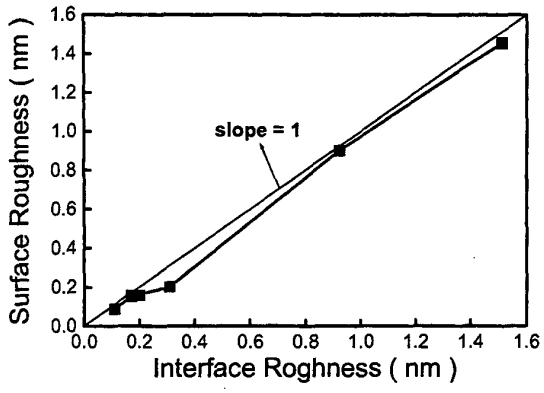

Fig. 7. The interface roughness (Si/SiO_2) vs the surface roughness of various samples measured by AFM. The similar magnitude between surface roughness and interface roughness implies the conformal growth of oxide.

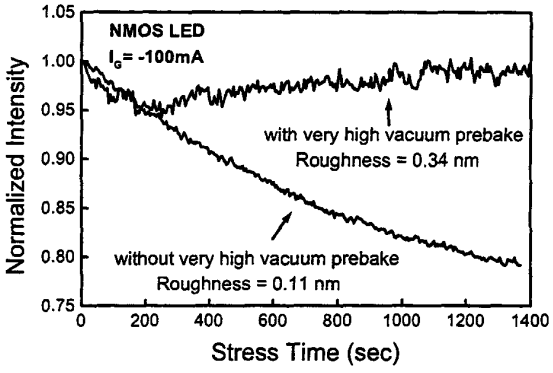

Fig. 8. The time evolutions of light emission intensity for the rough and flat NMOS LED, respectively. The intensity degrades about 20% after 1400 sec stress for the flat NMOS diode, while the intensity degrades very slightly after stress for the rough device.

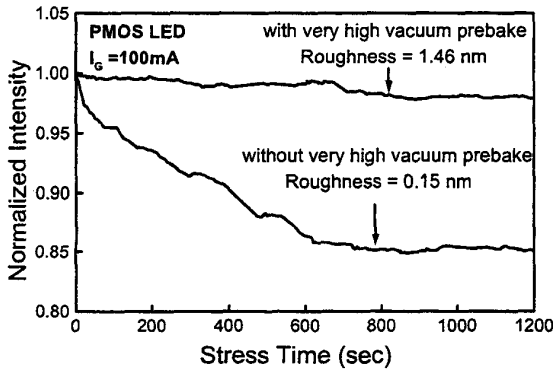

Fig. 9. The time evolutions of light emission intensity for the rough and flat PMOS LED, respectively. The rough PMOS diode shows much less emission intensity degradation than that of the flat PMOS diode.

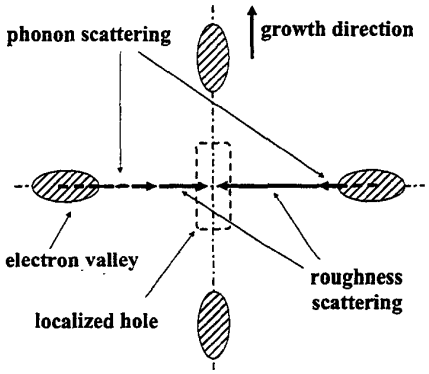

Fig. 10. The speculative mechanism in the reciprocal space of the radiative recombination in NMOS tunneling diode. The roughness and phonon scattering can provide the required momentum.

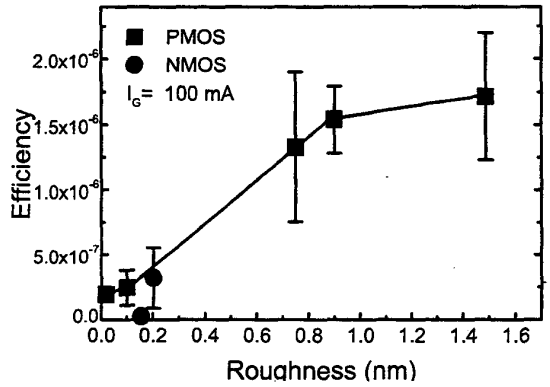

Fig. 11. The external quantum efficiency vs oxide roughness of MOS LED. The error bar is the standard deviation of external quantum efficiency measured by a set of devices. The devices with rougher oxide have larger light emission efficiency.

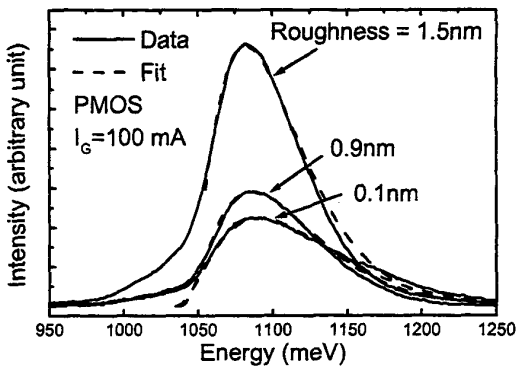

Fig. 12. The electroluminescence from the PMOS devices with various oxide roughness with the fitting curves of the electron-hole-plasma model. The roughness enhances the light emission intensity.