Analysis and Design of CMOS Broadband Amplifier with Dual Feedback Loops

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ABSTRACT

We present a broadband amplifier with 10.5dB gain and a 3-dB bandwidth of 1.7GHz using CMOS 0.25um process in this paper. The technique of dual feedback loops was used in the amplifier for terminal impedance matching. Derived formulas for voltage gain (or S_{21}), input return loss(or S_{11}), output return loss (or S_{22}) as well as transimpedance gain with open load and 50 Ω load (or Z_{21} and Z_T) have been used for the analysis and design of this amplifier. This circuit only dissipates 25 mW dc power.

Key words: Broadband amplifier, dual feedback, CMOS 0.25um, and dc power

1.INTRODUCTION

Broadband amplifiers are used in a large variety of applications, such as wireless systems, instrumentation, and optical communications [1]. Among the variety of broadband amplifiers, the Kukeilka configuration [2] is one of the popular circuits. However, no detail analysis of this kind of circuit implemented in CMOS technology was presented.

In this paper we present the derived analytic expressions of voltage gain, input return loss, output return loss and transimpedance gain for the CMOS Kukeilka circuit. Trade-offs among input impedance matching, voltage gain and bandwidth were found. Predicted results (12.8dB gain and 2.0GHz bandwidth) from our theory were found in good agreement with the simulated (12.3dB gain and 2.1GHz bandwidth) and measured results (10.5dB gain and 1.7 GHz bandwidth).

2.Principles of Circuit Design

The schematic of the Kukeilka broadband amplifier using CMOS technology is shown in Figure 1. The circuit consists of an input stage NMOS M1 driving an output stage NMOS M2. The local feedback resistor Rf1 and the global feedback resistor Rf2 are used for the input and output 50 Ω matching. Clearly this amplifier can be approximated by a two-pole system with open loop poles of $?_{P1}$ and $?_{P2}$. Local series feedback resistor Rf1 is used to adjust $?_{P1}$ while local shunt resistor Rf2 and series resistor Rs2 are used to adjust $?_{P2}$ so that the two poles are brought to be coincident. Then the global feedback resistor Rf2 is selected for a required loop gain to attain the maximally flat condition. However, since this amplifier tends to give over-damped characteristics [2], source peaking capacitance Cs2 [2,4] are connected in parallel with Rs2, respectively, to overcome this problem. The expressions for voltage gain, current gain, input/output impedances, close-loop poles and frequency responses of S parameters are described as follows.

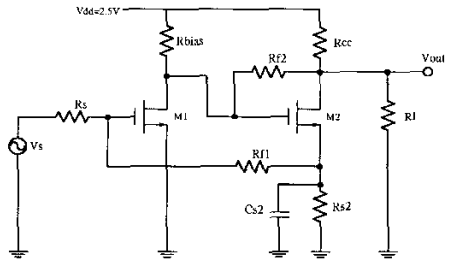


Figure 1. The schematic of the dual feedback broadband amplifier

2.1 Voltage and Current Gain

The open loop circuits of the dual feedback circuit for the calculations of open loop voltage and current gain are shown in Figures 2 and 3, respectively. From Figure 2, the voltage gain Vout/Vin without global feedback is given by

$$A_V = \frac{V_{out}}{V_{in}} \approx g_{m1} R_{K1} G_{m2} (R_{f2} // R_{cc} // R_L) \approx g_{m1} R_{f2} (1 - \frac{R_{K1}}{R_{f2}}) \qquad (1)$$

where Gm2=gm2/(1+(gm2+gmb2)Rs2), gmb2 is the transconductance of M1 due to body effect, gm1 and gm2 are the transconductances of M1 and M2 respectively. Hence the total voltage gain is

$$A_{VSF} = \frac{V_{in}}{V_S} \frac{V_{out}}{V_{in}} = \frac{R_{in}}{R_{in} + R_S} A_V \qquad (2)$$

where Rin is the input resistance of this circuit with global feedback, and it will be derived later.

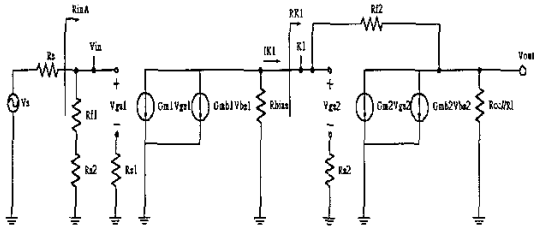


Figure 2 . Small-signal circuit for open loop voltage gain

From Figure 3, the formula of current gain without global feedback can be obtained

$$A_I = (R_{f1} + R_{s2}) \times g_{m1} \times \frac{R_{f2} + R_{cc} // R_L}{1 + G_{m2}(R_{cc} // R_L)} \times G_{m2} \tag{3}$$

Therefore the total current gain is given by

$$A_{IS} = \frac{I_{out}}{I_S} = \frac{I_{out}}{I_{in}} \frac{I_{in}}{I_S} = A_I \frac{R_S}{R_S + R_{f1} + R_{s2}} \tag{4}$$

Finally, the loop gain T can be determined to be

$$T = A_{IS} \times \beta_I = \frac{A_I \times \beta_I}{1 + (1 + A_I \beta_I) \frac{R_{in}}{R_s}} \tag{5}$$

where the feedback factor $\beta_I = R_{s2}/(R_{f1}+R_{s2})$.

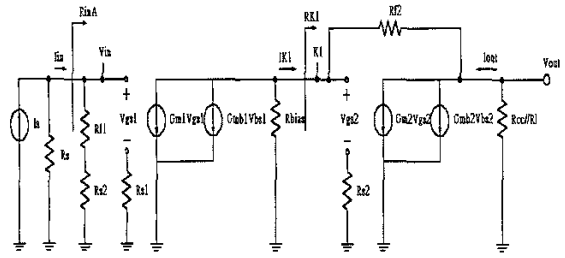


Figure 3. Small-signal circuit for open loop current gain

2.2 Input and Output Impedance

By inspection of Figure 3, the input resistance with feedback is

$$R_{in} = \frac{R_{f1} + R_{s2}}{1 + A_I \beta_I} = \frac{R_{f1} + R_{s2}}{1 + g_{m1} \frac{R_{f2} + R_{cc} // R_L}{1 + G_{m2}(R_{cc} // R_L)} G_{m2} R_{s2}} \tag{6}$$

On the other hand, the output resistance can derived directly from it definition and is given by

$$R_{out} = R_{out}' // R_{cc} = \frac{R_{f2} + R_{K2}}{1 + G_{m2} R_{K2}} // R_{cc} \tag{7}$$

where R_{K2} and is defined as

$$R_{K2} = \frac{V_{O1}}{I_{K2}} = \frac{R_s + R_{f1}}{R_s g_{m1} G_{m2} R_{s2}} \tag{8}$$

and Rout'= $(R_{f2}+R_{K2})/(1+G_{m2}R_{K2})$.

2.3 Close-loop Poles

Careful analysis of broadband amplifier without global feedback [2] yield the approximation pole positions as

$$\omega_{P1} \approx \frac{g_{m1}}{\frac{C_{g1} \times g_{m1}}{1 + \frac{g_{m1} \times R_{s1}}{1 + g_{mb1} \times R_{s1}}} \times \left[(R_s + R_{s1}) // (R_{f1} + R_{s2}) \right]} \tag{9}$$

$$\omega_{P2} \approx \frac{g_{m2}}{\frac{C_{g2} \times g_{m2}}{1 + \frac{g_{m2} \times R_{s2}}{1 + g_{mb2} \times R_{s2}}} \times \left[\frac{R_{f2} + (R_{cc} // R_L)}{1 + G_{m2} \times (R_{cc} // R_L)} + R_{s2} \right]} \tag{10}$$

where Cg1 and Cg2 are total gate capacitance of M1 and M2, respectively.

In close-loop circuit, the two open-loop poles will be brought closer by loop gain and eventually become complex conjugate if loop gain is large enough. The positions of the close-loop poles are given by

$$P_1, P_2 = -\frac{1}{2}(\omega_{p1} + \omega_{p2}) \pm \frac{1}{2}\sqrt{(\omega_{p1} + \omega_{p2})^2 - 4(1+T)\omega_{p1}\omega_{p2}} \tag{11}$$

2.4 Frequency Responses

Once two poles and DC voltage gain be known, we can determine the frequency response of S_{21} easily. That is

$$S_{21} = \frac{2A_{VFS}}{\left(1 + \frac{s}{P_1}\right)\left(1 + \frac{s}{P_2}\right)} \tag{12}$$

It is known that S_{11} and S_{22} have the same pole as S_{21} and the zeros of S_{11} ($?_{Z1}$ and $?_{Z2}$) and the zeros of S_{22} ($?_{Z3}$ and $?_{Z4}$) can be obtained by replacing R_S with $-R_S$ in and R_L with $-R_L$ in the expression of poles [5], respectively. The results can be put in the following forms

$$S_{11}=\frac{Z_{in}-R_S}{Z_{in}+R_S}=\frac{R_{in}-R_S}{R_{in}+R_S}\cdot\frac{\left(1+\frac{s}{\omega_{Z1}}\right)\left(1+\frac{s}{\omega_{Z2}}\right)}{\left(1+\frac{s}{P_1}\right)\left(1+\frac{s}{P_2}\right)} \quad (13)$$

$$S_{22}=\frac{Z_{out}-R_L}{Z_{out}+R_L}=\frac{R_{out}-R_L}{R_{out}+R_L}\cdot\frac{\left(1+\frac{s}{\omega_{Z3}}\right)\left(1+\frac{s}{\omega_{Z4}}\right)}{\left(1+\frac{s}{P_1}\right)\left(1+\frac{s}{P_2}\right)} \quad (14)$$

2.5 Transimpedance Gain

The open-loaded transimpedance gain can be calculated by

$$Z_{21}=\frac{A_I}{1+A_I\cdot\beta_I}\times(R_{f2}//R_{CC})\frac{1}{(1+\frac{s}{P_1'})(1+\frac{s}{P_2'})} \quad (15)$$

where P_1' and P_2' are the two poles given by (11) but with R_S = 8 and R_L = 8 . In the 50O -loaded system, the transimpedance gain can be shown to be

$$Z_T=\frac{S_{21}}{1-S_{11}}\cdot 50 \quad (16)$$

3.Experimental Results and Discussions

The schematic of the CMOS broadband amplifier has been shown in Figure 1. This circuit was fabricated with 0.25um process and the size of M1 and M2 are both 0.24um x 320um. The total power dissipation is only 25mW.The resistors have the following values: Rbias = 650O , Rcc = 150O , Rf1 = 80O , and Rf2 = 650O . The die photograph of the finished circuit is shown in Figure 4.

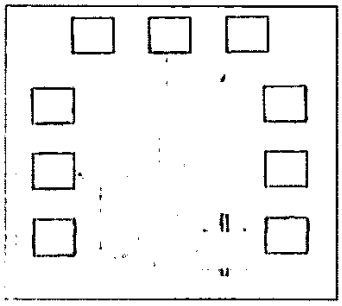


Figure 4. die photograph of the CMOS broadband amplifier

HP8510 network analyzer in conjunction with the cascade probe station was used to measure the characteristics of this broadband amplifier. The simulated, measured and predicted results are shown in Figure 5(a), Figure 5(b), Figure 5(c), Figure 5(d), and Figure 5(e) for S_{21}, S_{11}, S_{22},Z_{21} (open load transimpedance) and Z_T (50O load transimpedance), respectively.

The measured S_{21} exhibited a flat response with a 3-dB bandwidth of 1.7GHz and in band return loss $|S_{11}|$ and $|S_{22}|$ were smaller than –10dB. The predicted S_{21} at low frequency by the method we proposed is 12.8dB, in good agreement with the simulated S_{21} 12.3dB. The measured result is about 2dB lower than our prediction, which is possibly due to substrate loss that is not modeled. The simulated $|S_{11}|$ and $|S_{22}|$ also agreed well with the measured values as shown in Figure 5(b) and 5(c), respectively. Also shown are the calculated values of frequency responses from our theory for S_{21}, S_{11}, S_{22}, Z_{21}, and Z_T. Reasonably good agreement with the experimental results is found. The predicted bandwidth is 2.0GHz, which is comparable to the simulated result of 2.1GHz but higher than the measured result of 1.7 GHz. The discrepancy may be due the parasitic substrate capacitances. From Figure 5(d) and 5(e), we can find their difference is about 6dBO , because one is open-loaded and the other is 50O -loaded.

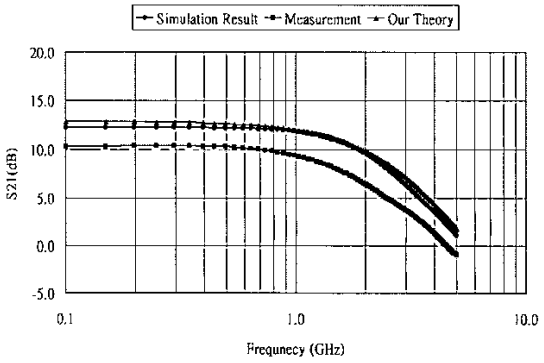


Figure 5(a). Simulated, measured and predicted results of S_{21}

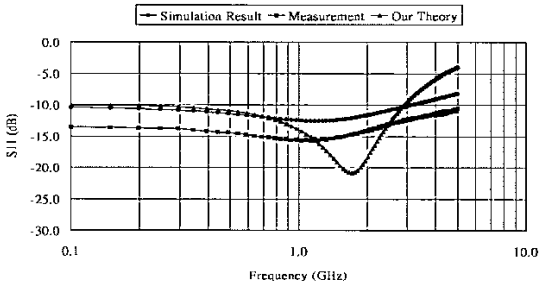


Figure 5(b). Simulated, measured and predicted results of S_{11}

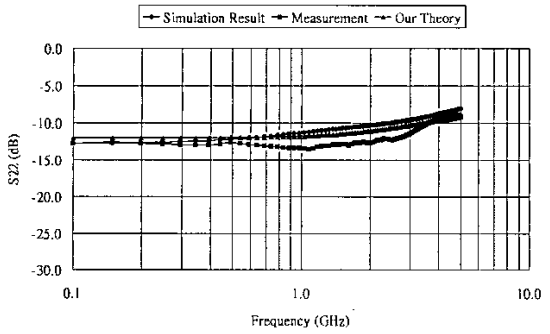


Figure 5(c). Simulated, measured and predicted results of S_{22}

Finally, the transimpedance gain with open load is 51.5dBO and a 3-dB bandwidth is 1.5 GHz of measured results while it with 50 O load is 43dBO and a 3-dB bandwidth is 2.3GHz. The group delay shown in Figure 6 is 150psec at low frequency and has a 3-dB bandwidth of 1.7 GHz.

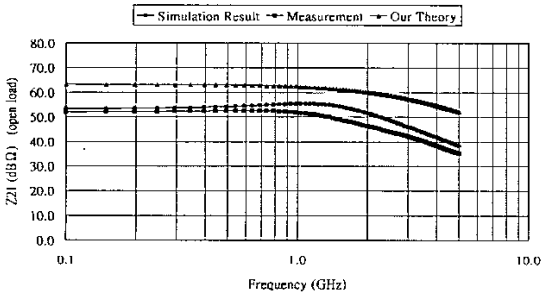


Figure 5(d) . Simulated, measured and predicted results of Z_{21}

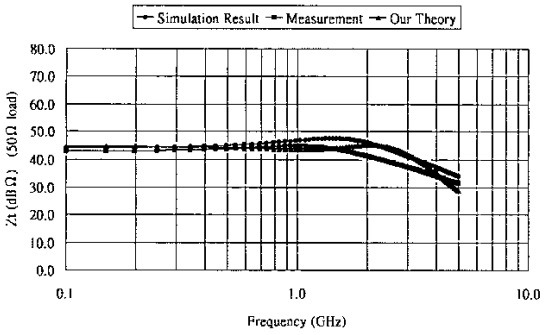
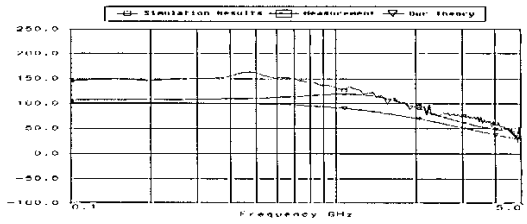


Figure 5(e) . Simulated, measured and predicted results of Z_T



4.Summary

The methodology of the analysis and design of CMOS broadband amplifier with dual feedback loops is proposed.

Figure 6 . Simulated, measured and predicted results of Group Delay

Expressions of voltage gain, current gain, transimpedance gain, input impedance and output impedance are also derived. A general method for the determination of the frequency responses of input/output return losses from the poles of voltage gain was also presented. The experimental results showed that small signal gain of 10.5dB and a 3-dB bandwidth of 1.7GHz with in band input/output return losses less than −10dB were obtained. The calculated values of small signal gain, bandwidth, input/output resistance, and frequency responses agreed well with those from experimental results. Thus the verification of our proposed equations was demonstrated..

5.Acknowledgements

Our thanks to CIC for allowing us to fabricate this work, and to Ping-Yu Chen and Horng-Wei Chiou for giving help on chip testing.

6.References

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