High SCR Design for One-Transistor Split-Gate Full-Featured EEPROM

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***Abstract*—A high source-coupling ratio design for full-featured EEPROM composed of one-transistor split-gate cells with a cell area of less than 22 F^2 is proposed. This is in contrast to a traditional cell that requires an extra select transistor and is not area economic when compared to the new design cell. In this design, the cell adopts poly–poly Fowler–Nordheim tunneling to erase, and an inhibited source voltage is used for the unselected cell to achieve bit erase. It has demonstrated excellent program and erase disturb margins and passed 300 k program/erase (P/E) cycling test. It was found that after P/E cycling stress, the cell gains a better erase disturb immunity.**

***Index Terms*—Disturb, full-featured EEPROM, source-coupling ratio (SCR), split-gate.**

I. Introduction

WHEN compared with standard Flash memory, full-featured EEPROM has the advantage of low power consumption (because block-erase is not necessary) and simple data file structures (since bit/byte program and erase can be performed) [1]. Recently, portable systems, IC cards, smart-cards etc., have become more and more popular, and usually have low power requirements. Therefore, developers of these systems are more liable to adopt high-endurance full-featured EEPROM rather than Flash memory. In this letter, a high source-coupling ratio (SCR) split-gate cell with poly–poly Fowler–Nordheim (F–N) tunneling to erase and source-side injection (SSI) to program is reported [3], [5]. It is known that the SSI has higher injection efficiency than the channel hot electron [5]–[7]. The cell has passed a 300-k program/erase (P/E) cycling endurance test and that can compete with other technologies [2], [8]–[10]. In addition, since the cell has enough margin to pass a 300-k times erase and program disturb test, error correcting circuitry would be not necessary in the circuit design [2]. Using inhibited source voltage on the unselected cell avoids the occurrence of F–N tunneling when the word-line (WL) is forced to a high voltage to erase the cell. As the cell already has a built-in select transistor, it does not require a stand-alone select transistor, unlike that usually used for most full-featured EEPROM with stack-gate cells. Such a select transistor needs to tolerate high voltage stress, so large device dimension is unavoidable. The cell is 4 F in width (bit-line + source-line), and ~5.5 F in length. The cell area can be less than 22 F^2. In addition, the split-gate cell is not subject to the over-erase issue [4] similar to the problem faced by the stack-gate cell. With these features, the periphery circuit overhang can be further reduced, especially for low density EEPROM applications. Finally, it was found that after P/E cycling stress, the cell has a better erase disturb window due to the fact that the electrons will be trapped in the tunnel oxide when F–N tunneling proceeds, retarding the electrons from tunneling through the oxide, especially in the low oxide electric-field region.

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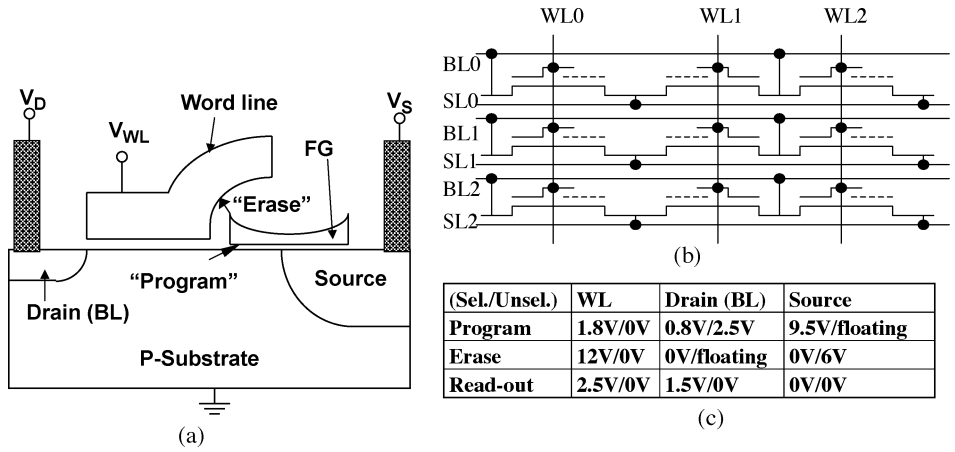
II. Device Fabrication

Double polysilicon 0.25-μm CMOS technology was used to fabricate the split-gate EEPROM cell with a sharp floating-gate (FG) edge [field-enhanced structure; see Fig. 1(a)] [3], [5]. After growing the first gate oxide, i.e., FG oxide, poly-Si and SiN layers were deposited sequentially by low-pressure chemical vapor deposition. The FG was defined by using photolithography, and the SiN layer was removed by using a dry etching to expose the FG area. Next, polysilicon oxidation was performed to generate a bowl-shaped poly structure. After removing the residual SiN, a poly etch was performed using poly-oxide as a hard mask, and the FG with a sharp tip structure was, thus, finished. Interpoly-oxide was then deposited to form both the tunnel oxide and the WL oxide. Finally, the WL was formed by depositing and patterning the second polysilicon. The FG-connected cell has the same structure as a normal cell except that a contact was placed on the FG so as to bias it directly. The memory array schematic diagram is shown in Fig. 1(b). The disposition of source line and WL is orthogonal.

III. Results and Discussion

The typical full-featured EEPROM cell operations are shown in Fig. 1(c). While programming the cell, the drain node is 0.8 V for the selected cell, and 2.5 V for the unselected cell. The V_S is 9.5 V and the SCR is around 70%, which is of benefit when coupled with the FG to a high potential and attracting the hot electrons generated around the gap region between the WL and FG. While erasing the cell, the V_S is 0 V for the selected cell, and 6 V for the unselected cell, as the 6 V source voltage will couple the FG to a higher potential due to high SCR design in this cell. Consequently, the voltage difference between the WL and the FG will not be high enough to allow the occurrence of F–N tunneling.



(Sel./Unsel.)	WL	Drain (BL)	Source
Program	1.8V/0V	0.8V/2.5V	9.5V/floating
Erase	12V/0V	0V/floating	0V/6V
Read-out	2.5V/0V	1.5V/0V	0V/0V

(c)

Fig. 1. (a) Cross section of the split-gate cell under study. (b) Memory array schematic diagram. (c) Typical cell operation conditions.

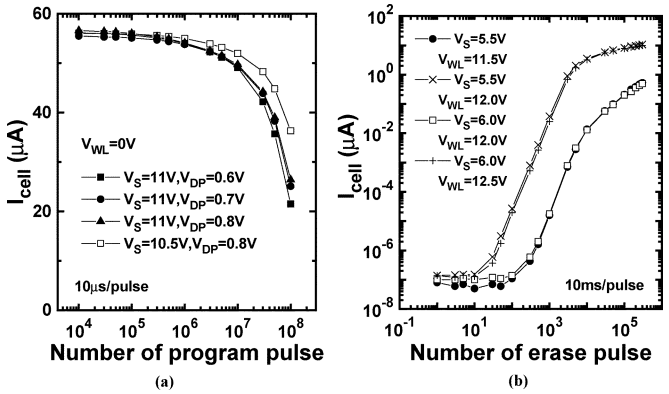


Fig. 2. (a) Program disturb: $I_{\rm cell}$ versus programming times under different programmed drain ($V_{\rm DP}$) and source ($V_{\rm S}$) voltage. The WL voltage ($V_{\rm WL}$) is 0 V and the pulsewidth is 10 μs for all conditions. (b) Erase disturb: under different WL and inhibited source voltages. The pulsewidth is 10 ms.

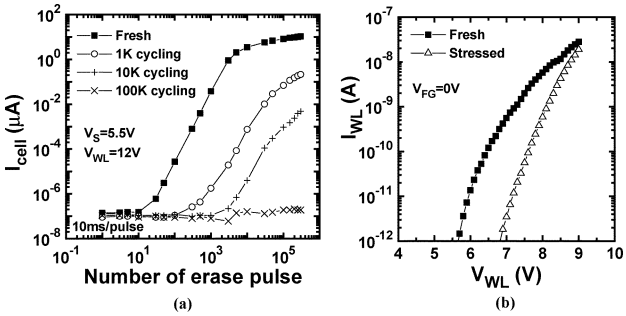


Fig. 3. (a) Erase disturb performance for the cell under different P/E cycles. The disturb testing condition is 12-V WL voltage and 5.5-V inhibited source voltage. (b) The voltage of the stressed tunnel oxide at 1-pA tunneling current shows 1.1-V less than that of fresh tunnel oxide. The *I–V* current is taken from the FG-connected cell mini-array.

The program disturb for full-featured EEPROM is more stringent than for Flash memory because there is no bulk-erase to refresh the cells each time, i.e., the number of times that the erased cell needs to tolerate the program disturb should be equal to the level of the cycling endurance time, which is usually more than 100 k times for smart-card applications. As shown in Fig. 2(a), it was found that a higher source voltage as well as a lower drain voltage during cell programming has a more serious cell current drop and a lower program disturb performance. The cell still requires more than 5×10^7 times of program pulse, at 10 μs per pulse, before the cell current drops to the half of the original, which is at least 2 orders in magnitude larger than 100 k. Unlike Flash memory performing sector or block erase, full-featured EEPROM needs to perform bit erase, so must have immunity to erase disturb. It is important to choose an inhibited source voltage for the unselected cell while the cell is erased. In Fig. 2(b), either the higher WL voltage or lower inhibited source voltage will cause a faster and more serious cell current increase. By using a 12-V WL voltage to perform the cell erase and a 6 V inhibited source voltage, the programmed cell continues to have a current lower than 1 μA even after 300 k times of erase pulse (10 ms per pulse). In addition, after P/E cycling stress, the cell will show an erase disturb immunity that is better than that of a fresh cell. The more cycling stress the cell takes, the more resistant to erase disturb it becomes. As shown in Fig. 3(a), after 1-k P/E cycling stress, using a 5.5-V inhibited source voltage and a 12-V WL voltage, the cell can pass the erase stress test 300 k times with a pulsewidth of 10 ms, and the cell current is still lower than 1 μA. This can be explained by the fact that when the cell is being erased by F–N tunneling, electrons will be trapped in the tunnel oxide, retarding the electrons tunneling in the low oxide electric-field region. In Fig. 3(b), the voltage for the fresh tunnel oxide is 1.1 V lower than that of the stressed oxide at tunneling current level of 1 pA. The current–voltage (*I–V*) data is taken from the FG-connected cell mini-array, which explains why the erase disturb margin will become larger when P/E cycling is performed. Nevertheless, the electron trap phenomenon in the tunnel oxide has a negative impact on the erase efficiency of the cell after P/E cycling stress. As illustrated in Fig. 4(a), the cell can pass the P/E cycling test 300 k times, where the erase condition is $V_{\rm WL} = 12$ V, 10 ms, and the program condition is $V_{\rm S} = 9.5$ V, 10 μs. Electrons trapped in both tunnel oxide and FG oxide [6] causes the erased state cell current to decrease after cycling. Fig. 4(b) shows no significant current change after a 720-h, 250 °C bake. The cells for the data retention test have 300-k P/E cycles as the precondition.

IV. Conclusion

In this letter, a high SCR split-gate cell for full-featured EEPROM, with small cell area characteristic was employed,

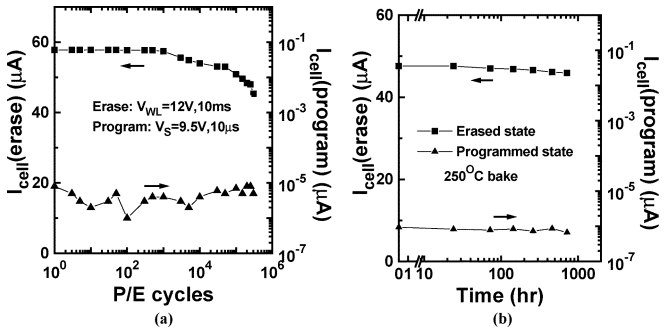


Fig. 4. (a) P/E cycling endurance test can pass 300 k times. (b) The data retention result for the cells after 300-k P/E cycling stress. The baking temperature is 250 °C.

meaning that an extra select transistor is not necessary. The cell has a low power operation where the cell is erased using a sharp poly edge, poly–poly F–N tunneling, and is programmed using SSI. High SCR design allows the use of an inhibited source voltage on the unselected cell to perform bit erase. Excellent program and erase disturb margins were shown. Unlike the stack-gate cell, the split-gate cell is over-erase free, so the periphery circuit can be simple. The cell described here can pass a P/E cycling endurance test 300 k times, which, as a result, makes it one of the best candidates for full-featured EEPROM memory.

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