Time-based frequency band selection method for phase-locked loops

T.-H. Lin and Y.-J. Lai

High-performance phase-locked loops (PLLs) often require voltage-controlled oscillators (VCOs) employing both discrete and continuous tuning mechanisms to satisfy a wide frequency range and a low VCO tuning gain simultaneously. An auxiliary circuit is required to facilitate the selection among a group of discrete bands. An agile technique to search for an optimum VCO frequency band is proposed. The search is based on measuring the period difference between a reference and the VCO-divided signals. The VCO band selection circuit is implemented with a 10 GHz PLL in a 0.18 μm CMOS process and consumes only an extra 3 mA. The band selection time is less than 4 μs.

Introduction: A PLL typically requires a wide tuning range to cover the desired frequency band and tolerate the process-voltage-temperature (PVT) variations. However, as supply voltage decreases and PLL operating frequency increases, VCO tuning gain (K_{VCO}, MHz/V) increases, thus degrading PLL noise and spur performance. A way to keep K_{VCO} low is to adopt both discrete and continuous tuning in the VCO, i.e. use multiple overlapped discrete frequency bands to cover the desired frequency range [1]. This topology requires a VCO band selection circuit to find the optimum band that covers the desired frequencies. Time spent on the band search adds to PLL settling time, resulting in an increased overhead in communication systems. To address this issue, we propose a fast VCO band selection method.

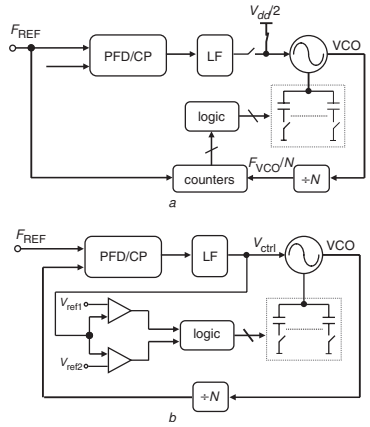

Fig. 1 *Conventional VCO band selection techniques*

a Open-loop approach
b Closed-loop approach

Conventional VCO band selection techniques: Existing VCO band selection techniques fall into two categories: open-loop and closed-loop methods. Fig. 1*a* shows a typical open-loop technique [2]. During operation, the PLL is opened at the loop filter (LF) and V_{ctrl} is connected to a reference voltage (usually $V_{dd}/2$). The band select circuit consists of counters that count the F_{REF} and F_{VCO}/N signal cycles until one of the counters overflows. This indicates which signal is faster/slower, and proper band adjustment can be made. This process repeats until the search criteria are met. To avoid possible errors due to initial phase uncertainties between two signals, the counts must be long enough. Therefore, the band selection time cannot be made small. In the closed-loop approach shown in Fig. 1*b*, the PLL tries to lock the VCO to a desired frequency. When the loop is settled, V_{ctrl} is measured against the predefined voltage range (between V_{ref1} and V_{ref2}). If V_{ctrl} is outside this range, another VCO frequency band will be selected (by proper capacitor array setting). V_{ctrl} is then checked again. Such operation repeats until V_{ctrl} finally falls into this desired range [1]. Since the PLL loop must settle before valid voltage comparison can be made, the band selection process can be slow.

Concept of proposed VCO band selection method: The proposed scheme is also an opened-loop method. Rather than comparing frequencies by counters, this approach compares two signals through measuring their period difference. This is accomplished by observing the relative phase positions of the two rising edges and falling edges. The operation principle is shown in Fig. 2. The signals from divider and reference paths (F_{VCO}/N, F_{REF}) are first divided by 2, such that the divider output pulse widths equal the signal periods. Initially, the voltage across the capacitor C_1 is reset to V_{ref}. Next, consider the two cases illustrated in the bottom of Fig. 2. When $F_{VCO}/2N > F_{REF}/2$, the phase difference of the two rising edges is smaller than that of the two falling edges. This results in a net effect of charging the capacitor C_1 and raises the charge pump (CP) output voltage (V_C). The comparator output will then be an indicator of which signal is faster/slower and this information is used to adjust the VCO frequency band.

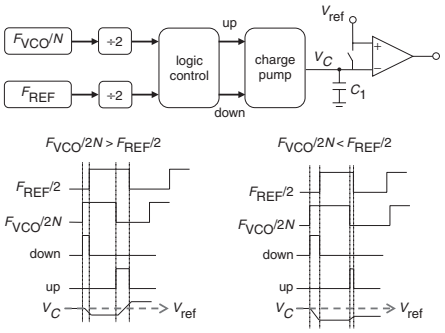

Fig. 2 *Conceptual illustration of proposed VCO band selection method*

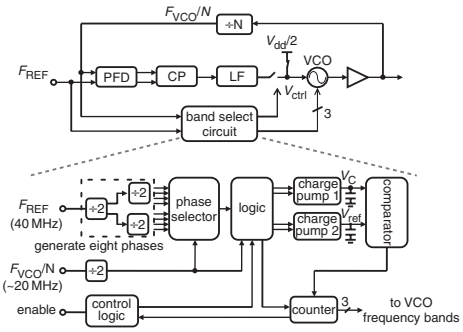

Fig. 3 *Block diagram of 10 GHz PLL with proposed VCO band selection circuit*

Architecture of VCO band selection: Fig. 3 shows the proposed band selection architecture is shown in Fig. 3. This method requires a proper phase relationship between $F_{VCO}/2N$ and $F_{REF}/2$ (where $F_{VCO}/2N$ leads $F_{REF}/2$). A phase selector circuit is developed to produce a reference signal with a proper phase. To increase the phase resolution, eight phases are generated from a 40 MHz F_{REF} signal. The reference signal out of the phase selector has a phase lagging that of $F_{VCO}/2N$ by 45–90°. A proper phase relationship increases the comparison accuracy, and prevents the following CPs from operating near the dead-zone region.

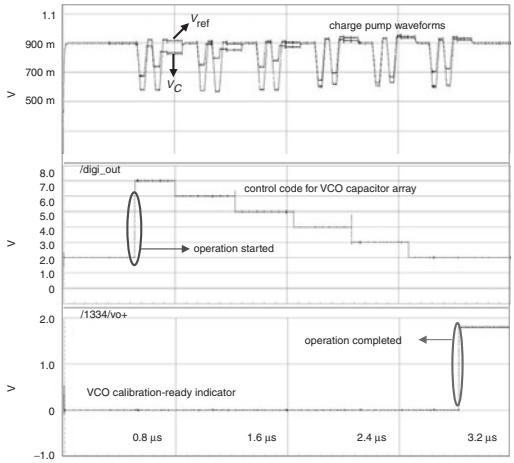

Fig. 4 *Operation of VCO band selection*

The method of generating V_{ref} can greatly affect the comparison accuracy. Owing to the nature of the switching operation of the CP (alternating the up/down currents), the voltage V_C, has a non-ideal switching component superimposed on top of the desired waveforms. To cancel out this effect, the reference voltage generation also incorporates a CP. This essentially forms a pseudo-differential topology, and other non-idealities, such as power line noise coupling or substrate noise pickup, can be largely cancelled as well.

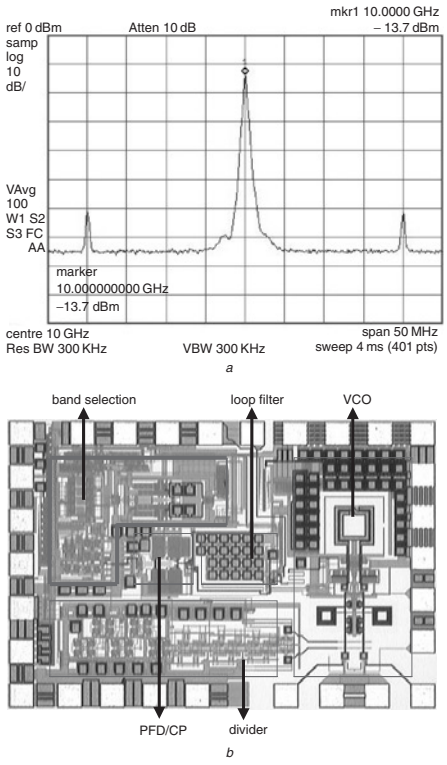

Fig. 5 *PLL output spectrum at 10 GHz and chip photo*

a PLL output spectrum
b Chip photo

In principle, each comparison can be completed in one $F_{VCO}/2N$ period, thus the band selection process is fast. In the actual implementation, each comparison cycle is repeated twice to enhance the circuit accuracy and robustness.

PLL implementations and results: The 10 GHz integer-N PLL block diagram is also shown in Fig. 3. When powering on, the PLL first enters the VCO band selection mode, during which, the loop is opened, and V_{ctrl} is set to $V_{dd}/2$. Once the operation is completed, the PLL then closes the loop and locks to the desired frequency. The band selection operation is illustrated in Fig. 4. The initial frequency band setting is 111 (decimal code 7, corresponds to the lowest VCO frequency band). As seen from the Figure, when V_C is lower than V_{ref} (i.e. F_{VCO}/N is slower than F_{REF}), the band selection circuit acts to decrease the code by 1, thus raising the VCO frequency. This process repeats until F_{VCO}/N is just faster than F_{REF}. At this point, a calibration ready signal is asserted to enable the PLL closed-loop locking. The worst case band selection operation (stepping from 111 to 000 sequentially) can still be completed in less than 4 µs. The band selection time can be further reduced with a binary search scheme.

This 10 GHz PLL with the proposed band selection circuit is fabricated in the TSMC 0.18 µm CMOS process. All circuit blocks are integrated on chip. In this work, VCO tuning range is divided into eight bands. The chip is measured with a 1.8 V supply and consumes 44 mW. The band select circuit dissipates only an extra 3 mA. The measured frequency range is 8.67–10.12 GHz, corresponding to 14.5%. The PLL output spectrum at 10 GHz is shown in Fig. 5*a*. The reference spurs are lower than −48 dBc. The VCO phase noise at 1 MHz away from the 10 GHz carrier is −102 dBc/Hz. The chip occupies an area 1400 by 964 µm. The die photo is shown in Fig. 5*b*.

Conclusions: An agile VCO frequency band selection technique and its application to a 10 GHz CMOS PLL have been reported. The proposed method is based on measuring the relative signal periods. It completes the band selection much faster than other methods where either long count of signal cycles or waiting for PLL settling is required. This agile time-based technique enables fast-settling PLLs.

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