Int J Adv Manuf Technol (2006) 29: 372–378
DOI 10.1007/s00170-005-2508-1

ORIGINAL ARTICLE

H.T. Young · Hsi-Tien Liao · Hong-Yi Huang

Surface integrity of silicon wafers in ultra precision machining

Received: 27 July 2004 / Accepted: 6 December 2004 / Published online: 24 March 2006

Abstract Silicon wafers are the most extensively used material for integrated circuit (IC) substrates. Before taking the form of a wafer, a single crystal silicon ingot must go through a series of machining processes, including slicing, lapping, surface grinding, edge profiling, and polishing. A key requirement of the processes is to produce extremely flat surfaces on work pieces up to 350 mm in diameter. A total thickness variation (TTV) of less than 15 μm is strictly demanded by the industry for an 0.18 μm IC process. Furthermore, the surfaces should be smooth ($R_a < 10$ nm) and have minimum subsurface damage (< 10 μm) before the final etching and polishing. The end product should have crack-free mirror surfaces with a micro-roughness less than 1.8 Å. In this paper, experiments are conducted to investigate the effects of various parameters on the subsurface damage of ground silicon wafers.

Keywords Grinding · Lapping · Silicon wafer · Subsurface damage · Total thickness variation

1 Introduction

Silicon wafers are being used today in a variety of microelectronic applications. Because single crystalline silicon is hard and brittle, surface and subsurface damage is easily induced during machining processes such as sawing, grinding, and lapping. Pei [1] has investigated subsurface cracks on ground silicon wafers and found that the depth of these cracks is approximately equal to half of the diamond grit size used in the grinding wheel. Processes such as etching, polishing, and cleaning are then needed to remove this layer of damage. If the depth of damage can be minimized in the grinding or lapping process, time will be saved and cost will be substantially reduced in the subsequent processing.

Ductile and brittle modes of deformation can happen in the same brittle material, like single crystal silicon, and the transition between them can be controlled by changing the machining conditions [2]. A chip removal mechanism for brittle and ductile deformation using abrasive grain is shown in Fig. 1. Brittle and partial ductile chips occur simultaneously on the surface of ground silicon wafer, as shown in Fig. 2. The regime in which the deformation takes place, in the form of simple plastic flow, is also the favoured regime for ductile mode machining [3].

Many researchers have investigated the structure of subsurface damage on ground single crystalline silicon wafers [4–6].

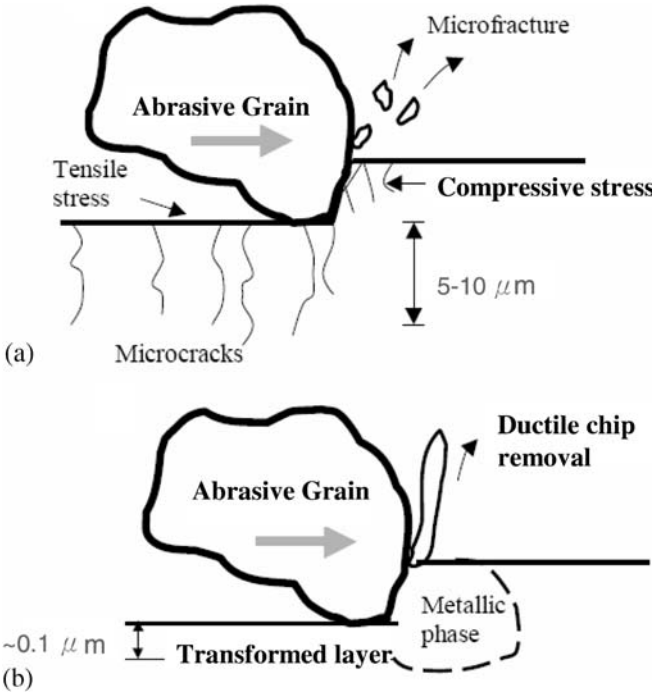


Fig. 1a,b. Chip removal mechanism **a** brittle **b** ductile

H.T. Young · H.T. Liao (✉) · H.Y. Huang
Department of Mechanical Engineering,
National Taiwan University,
No.1, Sec. 4, Roosevelt Road, Taipei, Taiwan 106, R.O.C.
E-mail: d88522025@ntu.edu.tw
Tel.: +886-3-5794340
Fax: +886-3-5771401

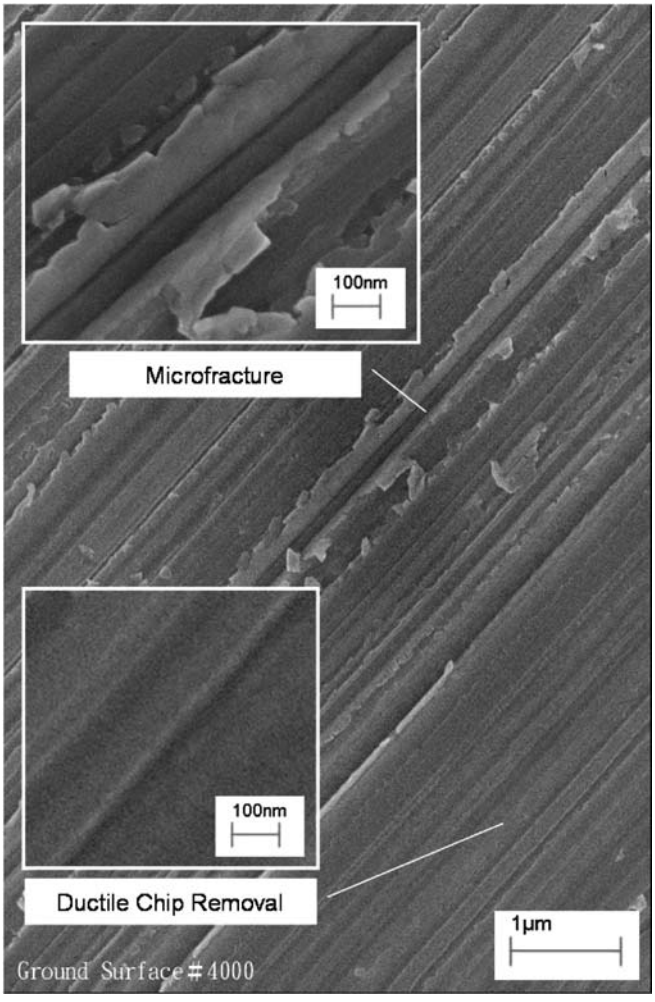


Fig. 2. SEM picture of surface of ground silicon wafer

The subsurface layer has an amorphous layer with a thickness of tens of nm on top of the ground surface. There is also oxygen and carbon penetration into this layer. Surface pittings, dislocations, and subsurface cracks with a thickness of a few tens of μm can occur in the vicinity area. At the bottom is a perfect single crystalline layer.

The subsurface cracks are measured by the depth that the subsurface damage layer reaches. It is critical to reduce the depth of cracks and to understand how cracks initiate and propagate into the material. Each individual grit on the grinding wheel creates a concentrated stress point from which cracks tend to initiate. The concentrated stress produces a crack normal to the surface under loading (called median cracks). Upon unloading, a crack parallel to the surface initiates and propagates (called lateral cracks). Usually, median crack formation is associated with strength degradation in the material, while lateral crack formation is associated with a material removal processes.

This study uses various methods to examine and measure subsurface damage. The results indicate that the grit size of the grinding wheel, the feedrate applied in the grinding process and the rotational speed of the wafer are the key factors. The subsurface damage of a lapped wafer is also investigated. Finally, a guideline is proposed to minimize subsurface damage in the grinding process of silicon wafers.

2 Experiments

The (100) surfaces of a single crystalline silicon wafer of 200 mm in diameter were ground with ultra-precision grinders, including an Okamoto VG-502 MK II 8 surface grinder (of different feed rate, chuck rotational speed) and a Cranfield Ultra Precision Face Grinding Machine (of different wheel rotational speed). Resin bonded diamond grinding wheels with grit sizes of mesh #325, #375, #800, #2000 were applied. Double side lapper SPEEDFAM DSM–12B and abrasive FUJIMI Fo#1200 were used for the corresponding experiments.

The operation of silicon wafer grinding is illustrated in Fig. 3. A silicon wafer is held on a rotary table and the grinding wheel is fed downwards. The wheel contacts with only half of the silicon wafer, to achieve better total thickness variation. While grinding, the wheel and the silicon wafer rotate in the same direction so that the wheel cuts the silicon wafer from centre to periphery. This arrangement, commonly used today, is called silicon wafer rotary grinding.

An example of silicon wafer lapping is demonstrated in Fig. 4. A silicon wafer is held on a carrier, driven by sun gear, between an upper and lower plate. An appropriate slurry with an abrasive is added and pressure is applied to lap the silicon wafer.

Two types of specimen were prepared to investigate subsurface cracks: a cross-sectional view specimen, which revealed the

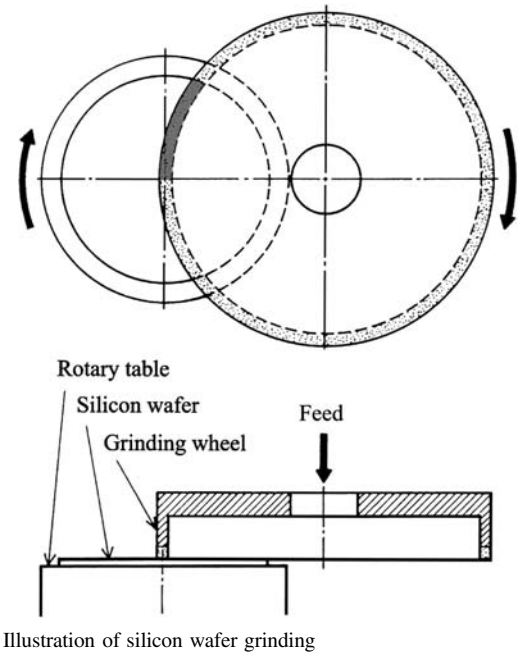


Fig. 3. Illustration of silicon wafer grinding

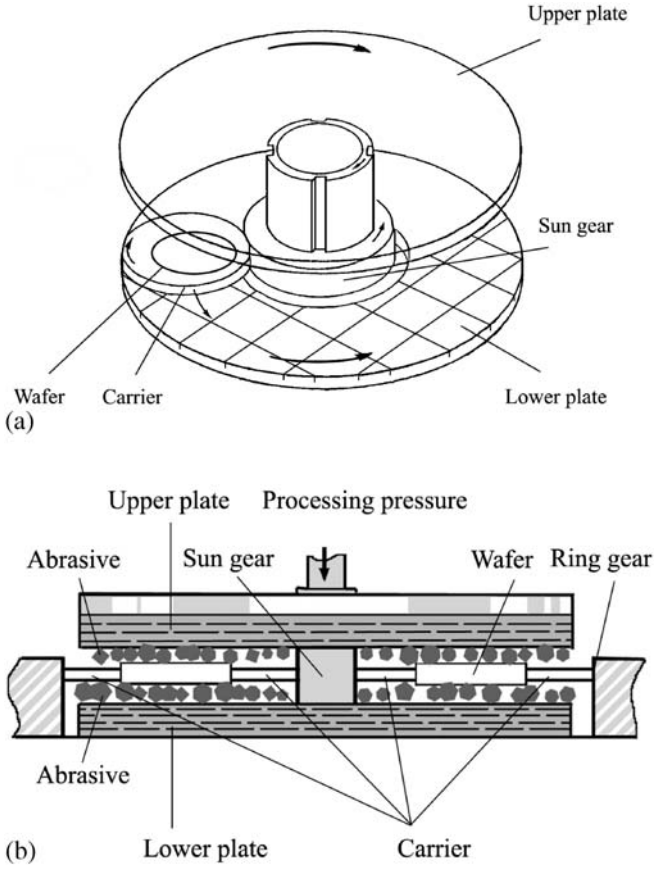


Fig. 4a,b. Illustration of silicon wafer lapping

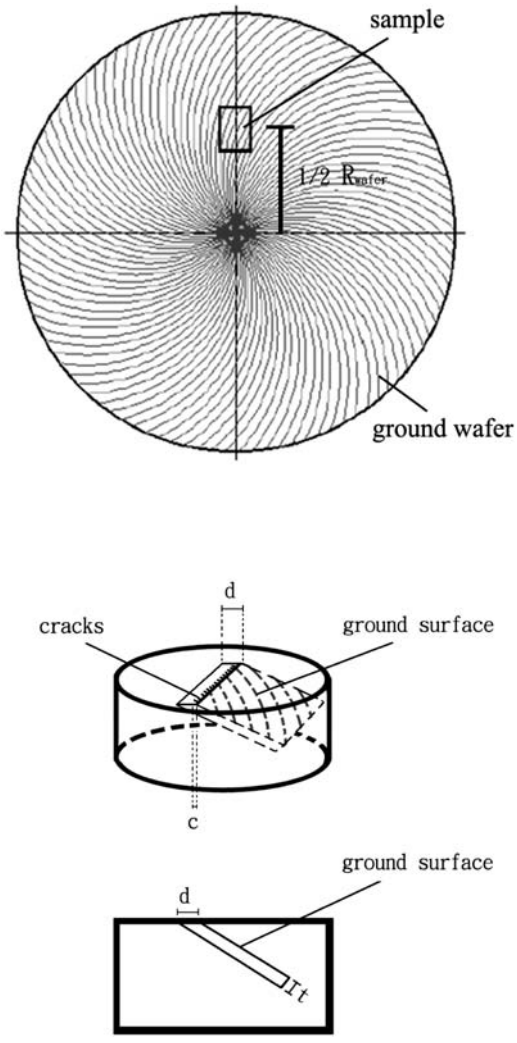


Fig. 5. Cross-sectional view of specimen preparation

structure of material perpendicular to the ground surface; and a plane view specimen, with its surface parallel to the ground.

The cross-sectional view specimen revealed the structure of subsurface cracks. To prepare the specimen, a rectangular sample with an area of 10 mm by 20 mm is cleaved from the ground wafer. The cleaved sample should always be taken from the same position of the wafer, as the sample position has a pronounced effect on subsurface cracks. The cross-section of interest is then angle polished and etched with Yang solution to make the subsurface cracks discernable (as shown in Fig. 5). The real crack depth c_{real} is then calculated as $c_{\text{real}} = t \times c/d$, where c is the measured crack depth, d is the width of the cross-section, and t is thickness of the sample.

The plane view specimen was used to show the distribution of subsurface cracks and surface pittings. The preparation process is similar to that used for the cross-section view specimen, but the interested plane is the ground surface.

3 Results and discussion

3.1 Microscopy observation

A photograph of a ground silicon wafer viewed by a magic mirror is shown in Fig. 6. The regular pattern on the surface of silicon wafer is called the grinding mark. The density of the grinding mark is related to the ratio of the chuck rotational speed and the wheel rotational speed. When the value of that ratio approaches 1, the highest density grinding mark is obtained.

The cross-sectional observations of the subsurface structure on ground and lapped wafers are shown in Fig. 7. It is obvious that the cracks propagate in the same direction. In fact, cracks are separation planes of the material and have particular fracture modes in single crystalline silicon [7]. According to fracture mechanics, it is easier for cracks to propagate along the crystal planes of lowest fracture toughness. There is little difference between subsurface cracks on the ground wafer and the lapped wafer, though some cracks formed a few μm under the lapped surface, as shown in Fig. 7b.

The plane view observation of the subsurface cracks and pittings on ground and lapped wafers are shown in Fig. 8. The cracks on the ground wafer were distributed along the scratching path of grits but the cracks of lapped wafer, shown in Fig. 8c and d, were not. There are two types of cracks observed in the ground

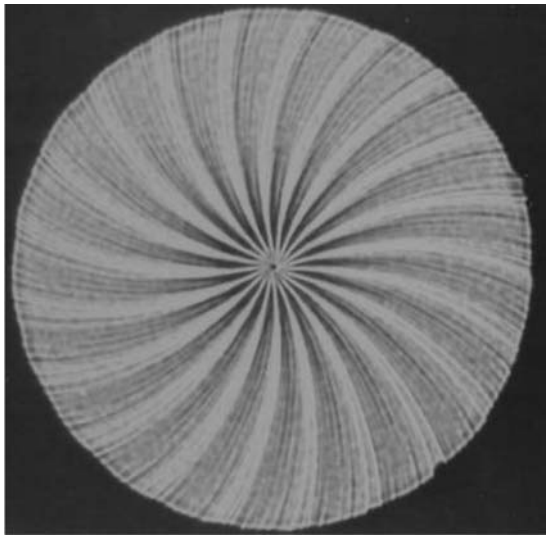
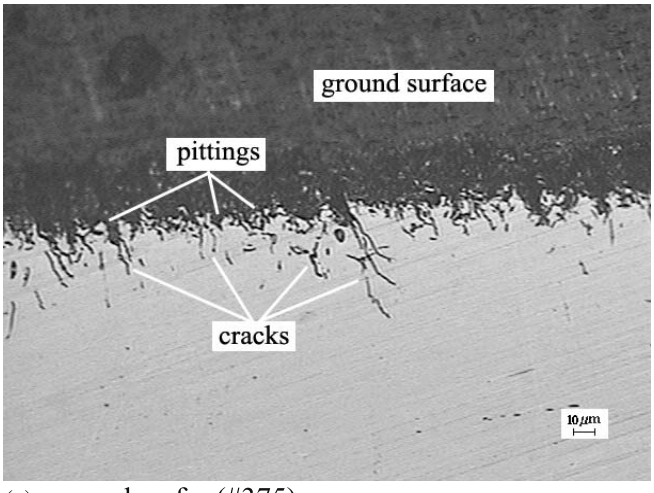
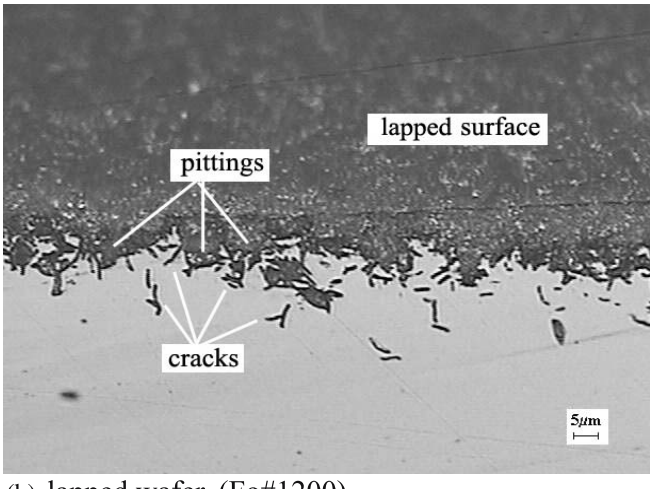


Fig. 6. Photo of ground silicon wafer viewed by magic mirror



(a) ground wafer (#375)



(b) lapped wafer. (Fo#1200)

Fig. 7a,b. Cross-sectional observations of subsurface cracks. **a** ground wafer (#375) **b** lapped wafer. (Fo#1200)

wafer, shown in Fig. 8b: chevron cracks and partial cone cracks. From the scratching test on silicon wafers [8], it is concluded that the chevron cracks came from a sharp grit while the partial cone cracks came from a blunt grit.

The surface of silicon wafers machined by grinding with mesh grit sizes of #2000 and #4000 are shown in Figs. 9 and 10, respectively. The thickness of the subsurface damage layer on the ground silicon wafer with mesh #2000 is approximate 1.2 μm, while for mesh #4000 the thickness is approximately 0.6 μm. Grinding of silicon wafers produces some partial ductile streaks on the ground surfaces. However, under optimal grinding conditions, more partial ductile mode surfaces could be obtained. This resulted in significantly shortened polishing time for producing an acceptable surface finish.

3.2 The grain depth of cut of ground silicon wafer

A great deal of research has been done to predict median cracking in static indentation and scribing test. All of the results show that bigger forces of indentation cause deeper median cracks. It's also been suggested that if the force of each grit is reduced, the subsurface cracking will be reduced. It is difficult, however, to grind a wafer to the desired geometry if the force is used as the control variable. The other, more practical approach is to control the grain depth of cut d_g. It is an indirect way to control the force and easily implemented as a control variable by regulating grinding variables such as feed rate, grain size, wheel rotational speed, and chuck rotational speed. Furthermore, ductile grinding of silicon wafers will be achieved by controlling the condition $d_g < d_c$, where d_c is the critical cutting depth of single crystalline silicon.

Sharp et al. have analyzed the grain depth of cut in plunge grinding, using computer simulation and an analytic model [9]. The relation between grain depth of cut and grinding parameters can be rewritten for wafer grinding as follows:

$$d_g = 7.37R\left(\frac{f' r_1 \omega_1}{L w_2 F_v \omega_2^2}\right)^{0.4} \tag{1}$$

where R is half the grain size, f' is the feed rate in μm/min, r_1 is the distance from wafer center to the sample location, ω_1 is the chuck rotational speed in rpm, w_2 is the thickness of the diamond cup wheel, and ω_2 is the wheel rotational speed in rpm. $F_v = 0.18$ is the grain volume fraction in the binder and $L = 300$ mm is the mean circumference of the grinding wheel used in the experiments.

3.3 Results of grinding

The results of grinding are shown in Fig. 11. The maximum depth of subsurface cracks is related to the grain depth of cut and can be minimized by controlling it, i.e., using finer grain size, lower feedrate, lower chuck rotational speed, and higher wheel rotational speed. However, the maximum depth of subsurface cracks and wheel rotational speed ω_2 are not as related as we expected. From Eq. 1, d_g is proportional to $(1/\omega_2)^{0.8}$ and thus the curve should be more abrupt than it appears in Fig. 11e.

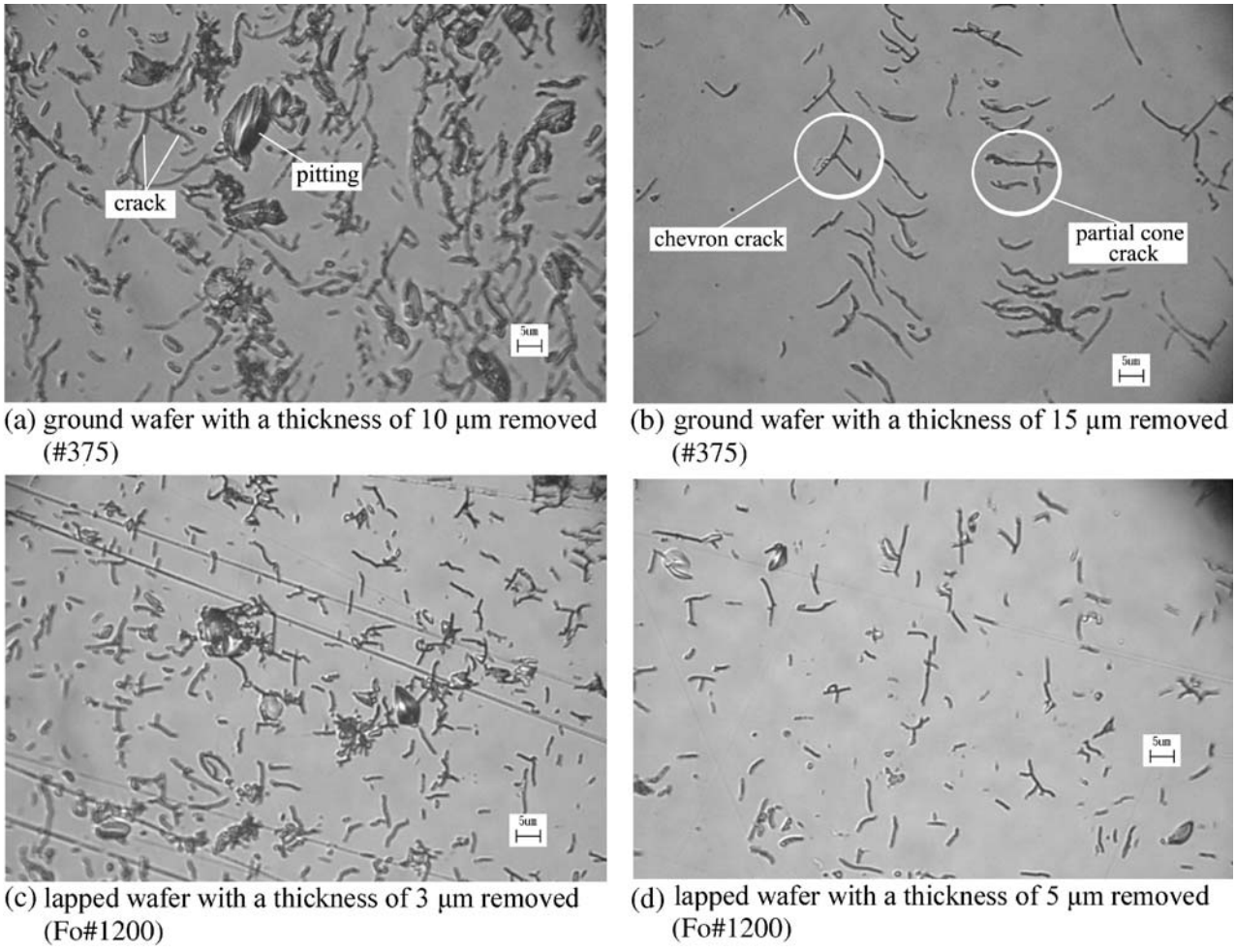


Fig. 8a–d. Plane view observations of subsurface cracks. **a** ground wafer with a thickness of 10 μm removed (#375) **b** ground wafer with a thickness of 15 μm removed (#375) **c** lapped wafer with a thickness of 3 μm removed (Fo#1200) **d** lapped wafer with a thickness of 5 μm removed (Fo#1200)

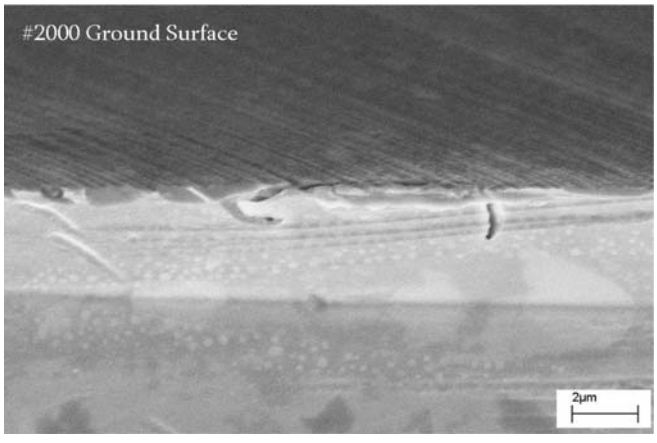


Fig. 9. SEM picture of subsurface damage layer of ground silicon wafer with grit size of mesh #2000

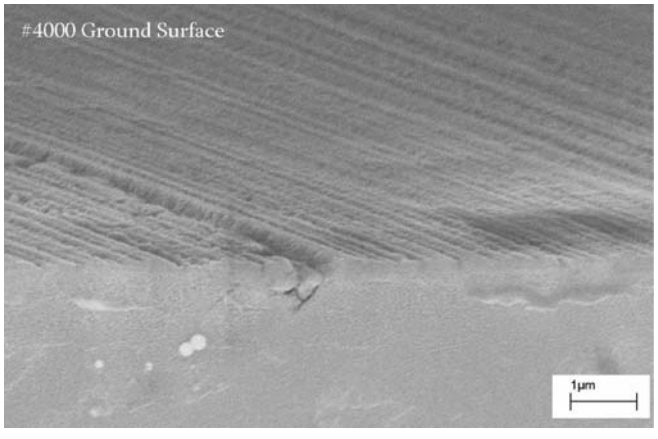


Fig. 10. SEM picture of subsurface damage layer of ground silicon wafer with grit size of mesh #4000

There are two possible explanations for this phenomenon. The first is resonance. Because the grinding machine will be at resonance while working at a wheel rotational speed of 1200 rpm, it could cause deeper depth of subsurface cracks. The second explanation is thermal expansion. The thermal expansion could be several μm during grinding, and could be even

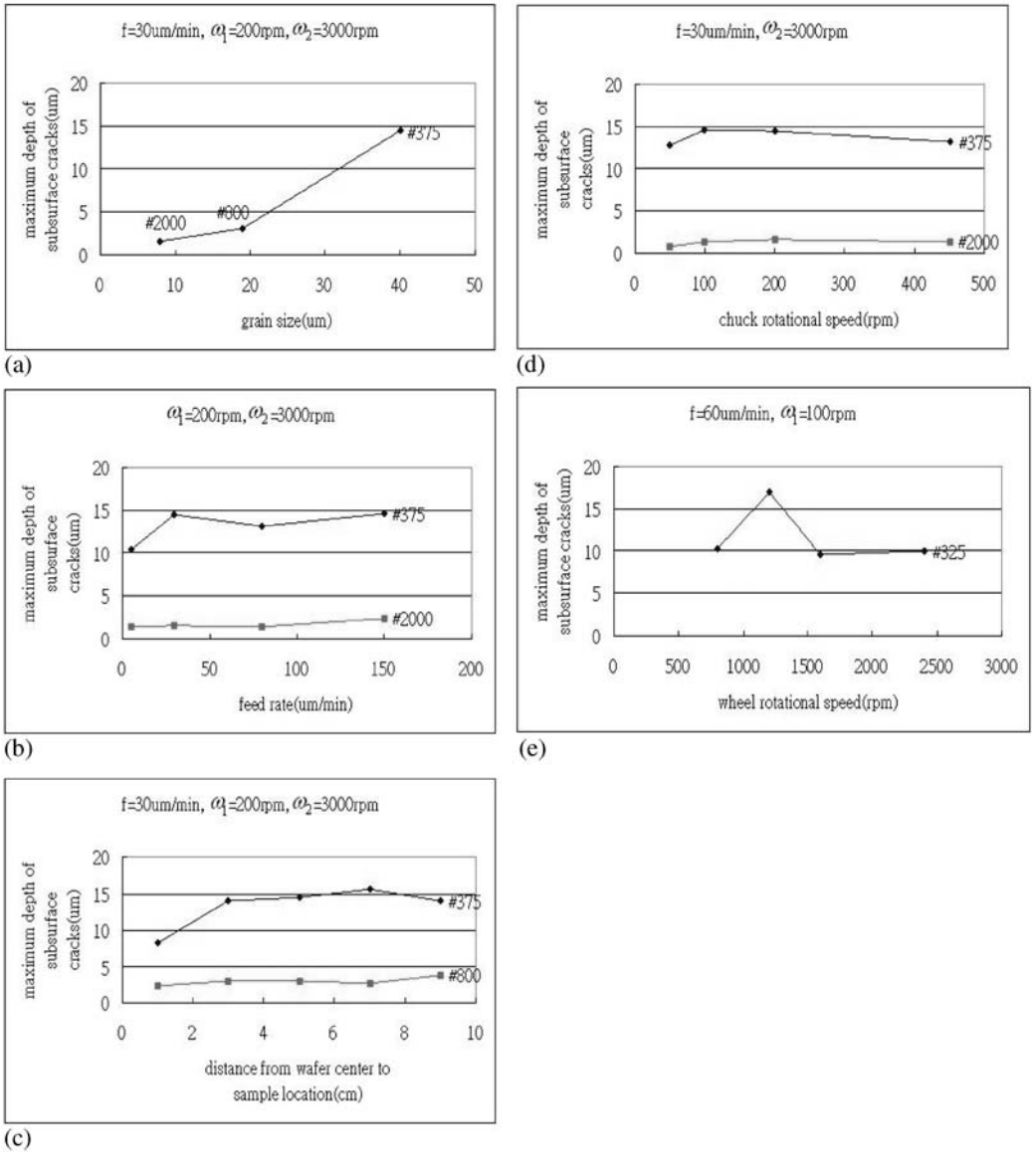


Fig. 11a–e. Effect of grinding parameters on the maximum depth of subsurface cracks

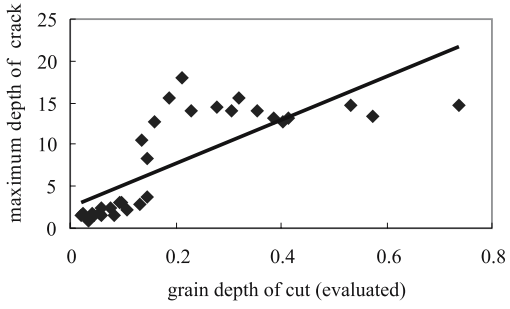


Fig. 12. Effect of evaluated grain depth on the maximum depth of subsurface cracks

worse at higher wheel rotational speeds [10]. For this reason, we may have underestimated the real value of d_g at higher wheel rotational speeds and, hence, the result is not as we expected.

It should also be noted that the depth of subsurface cracks should be approximately equal to half of the diamond grit size used in the grinding wheel ([1]). The experimental results, however, show the depth of subsurface cracks to be equal to one-third of the diamond grit size used in the grinding wheel. It is suggested that the results will vary with different grinding machines or grinding conditions. The effect on the maximum depth of subsurface cracks of evaluated grain depth of cut is shown in Fig. 12.

4 Conclusion

The subsurface cracks of ground and lapped silicon wafers were investigated and compared. There were chevron and partial cone cracks observed from plane-view specimens of ground silicon wafers. It was found that larger grit sizes resulted in deeper

cracks. The grinding wheel grit size was the dominant factor in crack formation observed in the present investigation. The deeper crack could also result from a faster feed rate or a higher chuck rotational speed. A higher wheel rotational speed, however, would lead to shallower cracks. The grain depth of cut on ground silicon wafers was derived in this study and used as the control variable to reduce subsurface cracks. Ductile regime grinding can be achieved by setting the condition $7.37R\left(\frac{f' r_1 \omega_1}{L w_2 F_v \omega_2^2}\right)^{0.4} < d_c$, as an appropriate set of grinding parameters. Reduced polishing time and improved surface quality can be realized with the presence of ductile streaks.

References

1. Pei ZJ, Billingsley SR, Miura, S (1999) Grinding induced subsurface cracks in silicon wafers. Int J Mach Tools Manuf 39:1103–1116
2. Zhong ZW (2003) Ductile or partial ductile mode machining of brittle materials. Int J Adv Manuf Technol 21:579–585
3. Atkins AG, Mai YW (1985) Elastic and plastic fracture. EllisHorwood, Chichester, UK
4. Zhang LC, Yasunaga, N (1997) Advances in abrasive technology. World Scientific, Singapore
5. Jeynes C, Puttick KE, Whitmore LC, Gartner K, Gee AE, Millen DK, Webb RP, Peel RMA, Sealy BJ (1996) Laterally resolved crystalline damage in single-point-diamond-turned silicon. Nucl Instrum Methods Phys Res B 40:431–436
6. Chen LQ, Zhang X, Zhang TY (2000) Micro-raman spectral analysis of the subsurface damage layer in machined silicon wafers. J Mater Res 15(7):1441–1444
7. Tsai YL, Mecholsky JJ Jr (1991) Fractal fracture of single crystal silicon. J Mater Res 6(6):1248–1263
8. Misra A, Finnie I (1979) On the scribing and subsequent fracturing of silicon semiconductor wafers. J Mater Sci 14:2567–2574
9. Sharp KW, Miller MH, Scattergood RO (2000) Analysis of the grain depth of cut in plunge grinding. J Int Soc Precis Eng Nanotechnol 24:220–230
10. Lin CP (2002) A study on the characteristics of the surface profile of the ground wafer. Masters thesis, National Tsing Hua University