

# Defects of Base Metal Electrode Layers in Multi-Layer Ceramic Capacitor

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**An ultra-thin Ni-based metal used as the electrode layer in multilayer ceramic capacitor determines the dielectric performance of the capacitor. The warpage and the continuity of the inner electrode layers, and a dihedral angle between BaTiO<sub>3</sub> layers and metal electrodes of two ceramic capacitors (X7R and X5R) were characterized by optical microscopy and scanning/transmission electron microscopes. The results show that the warpage of the chips is closely related to the discontinuity of the inner electrode. The discontinuity takes place mainly because of Rayleigh instability of the Ni layer, but is less induced by the tensile stress from sintering.**

## I. Introduction

MULTILAYER ceramic capacitors (MLCCs) have been developed for decades. The thickness of the electrode and BaTiO<sub>3</sub> (BT) layers has been reduced to a micrometric range to diminish the size while maintaining the dielectric performance of the capacitors. However, this process introduces several structural defects in the base metallic electrode layer, such as warpage of the layers, and discontinuity of the inner electrode. No published technical literature has systematically analyzed these defects. Studies have reported several interesting microstructures of the BT materials. Core-shell structure,<sup>1,2</sup> dislocation loops,<sup>2</sup> and glass-phase boundaries<sup>3</sup> were observed using a transmission electron microscope (TEM).

For many ceramic systems (including composites), the mechanical and sintering properties depend strongly on microstructural factors.<sup>4</sup> The phenomenological evidence of the distribution of dihedral angles has been widely discussed as to show the effect on the sintering behavior of a MgO-doped Al<sub>2</sub>O<sub>3</sub> system.<sup>5</sup> The distribution of dihedral angles in a pure Al<sub>2</sub>O<sub>3</sub> system is broader because of surface faceting, but becomes narrower and sharper when a small amount of MgO is added, indicating a change in grain boundary energy.

This investigation examines the significant microstructure features of Ni layers in two MLCC chips, and attempts to understand how the defect features are affected by the interfacial properties of BT and Ni grains. We quantified these features to understand the causes of discontinuity of the thin Ni layer.

## II. Experimental Procedure

This work analyzed chip A (X5R 1210/10 μF) and chip B (X7R 1210/3.3 μF), supplied by Phycomp Taiwan Ltd. (Kaohsiung, Taiwan, Republic of China). The microstructural features of the chips were examined by observing two cross-sections of the

chips, which were the planes parallel and perpendicular to the BT layers and were marked as plane A and plane B, respectively. The polished cross-sections were observed by an optical microscope (OM, HFX-DX, Nikon, Sugaya, Japan), a scanning electron microscope (SEM, XL30, Philips Co., Eindhoven, Holland), and a TEM (2000FX, JEOL Co., Tokyo, Japan).

The following section describes the quantitative methods of the microstructural features.

### (1) Warpage Angle

The intercept of plane A, which is parallel to both BT and electrode layers, should show a single-phase layer, either a BT layer or an electrode layer. However, several close loops with an alternation of BT and electrode layers were observed, indicating that the chip became concave and caused the layers to bend, and then the layers in the chip lost their parallelisms. Therefore, the warpage angle was defined as the angle between the inner electrodes and plane A as follows:

$$\phi = \sin^{-1}(d/L) \quad (1)$$

where  $d$  denotes the thickness of either metal or BT layer, and  $L$  represents the separation between two close loops measured on the center line, as shown in Fig. 1(a).

### (2) Degree of Discontinuity ( $D$ )

A discontinuous metal layer was occasionally observed from plane B of the MLCC chip.<sup>6</sup> The degree of discontinuity of the metal layer was defined as

$$D = L_d/L_0 \quad (2)$$

where the  $L_0$  denotes the observed length, and  $L_d$  denotes the integral length intersecting with pores or defects in the observed area.

### (3) Dihedral Angle

The dihedral angle was measured from the triple point of two BT grains and one Ni grain. The relation between surface energy and dihedral angle of the metallic electrode to the BT phase could be expressed as

$$\gamma_{gb} = 2\gamma_i \cos(\theta/2) \quad (3)$$

where  $\gamma_{gb}$  and  $\gamma_i$  represent the free energy of BT grain boundaries and the BT/Ni interface, respectively. Additionally,  $\theta$  is the interfacial dihedral angle of grain boundary.

## III. Results and Discussion

### (1) Warpage of MLCC Chips

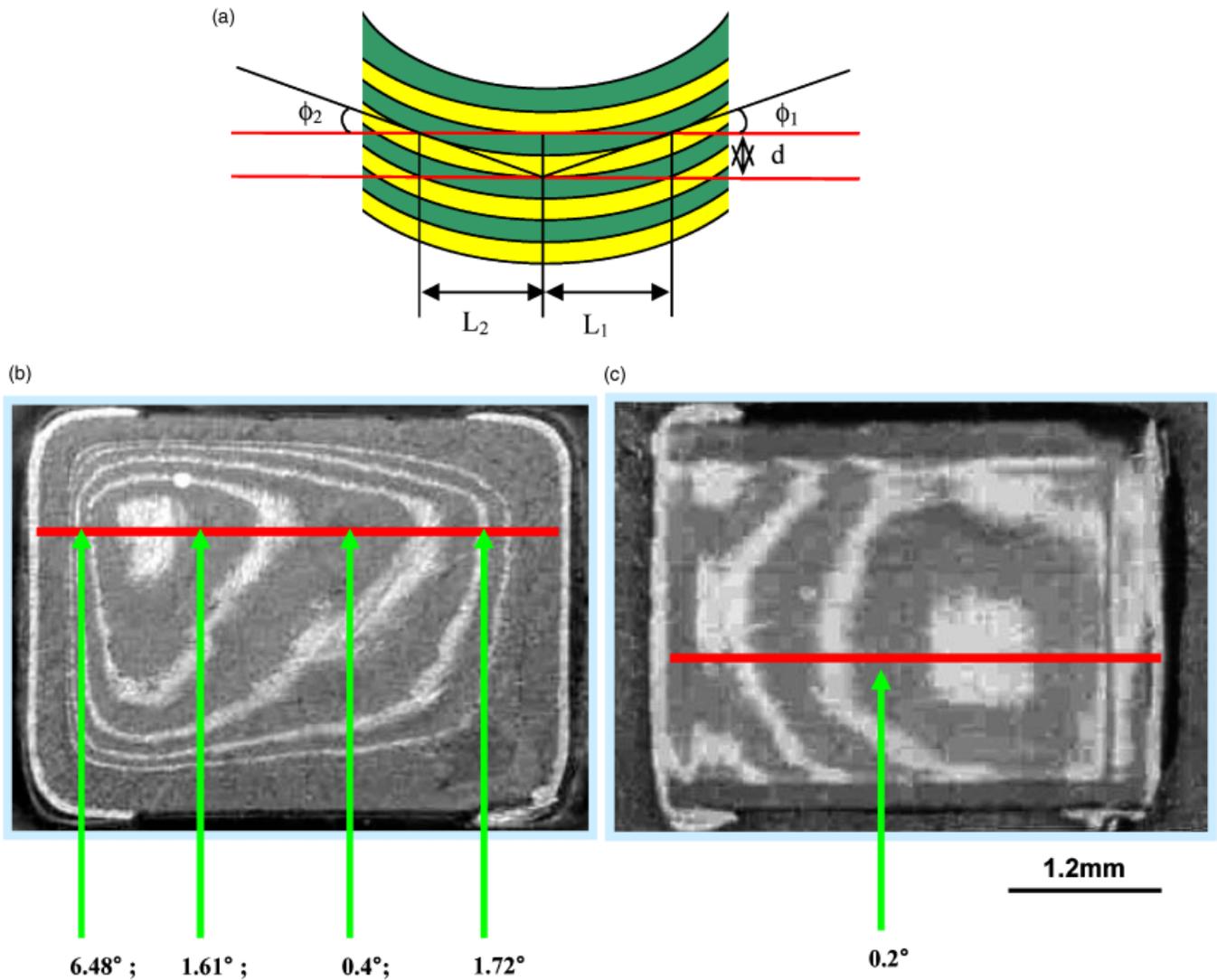
Notably, Figs. 1(b) and (c) shows two optical micrographs of plane A (200 μm below the surface of chips A and B). All samples demonstrate close loop structures. The warpage angles from left to right of chip A are 6.48°, 1.61°, 0.4°, and 1.72°, as shown

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**Fig. 1.** (a) Illustration of the warpage formation of the metal layers in multi-layer ceramic capacitor; top view of the cross-sections, and basal lines with warpage angles ( $\phi$ ) of (b) chip A (depth 200  $\mu\text{m}$ ) and (c) chip B (depth 300  $\mu\text{m}$ ).

in Fig. 1(b). In comparison, the warpage angles of chip B are always less than  $1.0^\circ$  (ca.  $0.2^\circ$ ) (Fig. 1(c)).

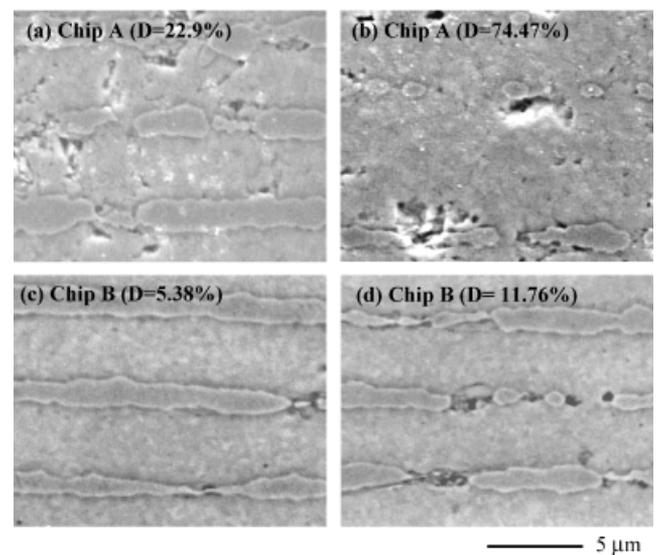
The average thicknesses of the Ni metal and BT layers are 2.5 and 4.5  $\mu\text{m}$  in chip A, and 1.2 and 3.5  $\mu\text{m}$  in chip B specimen, respectively. The factors that may affect the warpage angles include the ratio of the thickness and thermal expansion coefficient mismatch of the metal and BT electrode layers; the depth of the layer in the chips; and the sintering temperature. A larger warpage angle was often observed at the edges than that in the center of a chip.

### (2) Degree of Discontinuity ( $D$ ) of Inner Ni Electrode

The degree of discontinuity may indicate the quality of the internal electrode of MLCC. The electrode layer might disconnect and exhibit a fish-eye shape, as shown in Figs. 2(b) and (d). Figure 2(b) shows that some parts of the Ni electrodes were missing in chip A. The  $D$  values of the chips A and B ranged from 20.9% to 74.5% and from 5.4% to 15.5%, respectively.

The discontinuity value of the Ni layer varied in different positions of the chip is shown in Fig. 3. The lowest  $D$  value in chip A was about 10%, noted to be close to the volume fraction (10 vol%) of the BT particles added in the metallic layer. Additionally, the discontinuity was more severe near the middle-bottom position of the chip. The  $D$  value might be up to 75% (Fig. 2(b)).

As the microstructures demonstrate in Fig. 1, the warpage angles in chip A were greater than those in chip B. A strong discontinuity was often noted in the metallic layers near the



**Fig. 2.** Scanning electron microscope micrographs and degree of discontinuity ( $D\%$ ) of the samples: (a, b) chip A; (c, d) chip B.

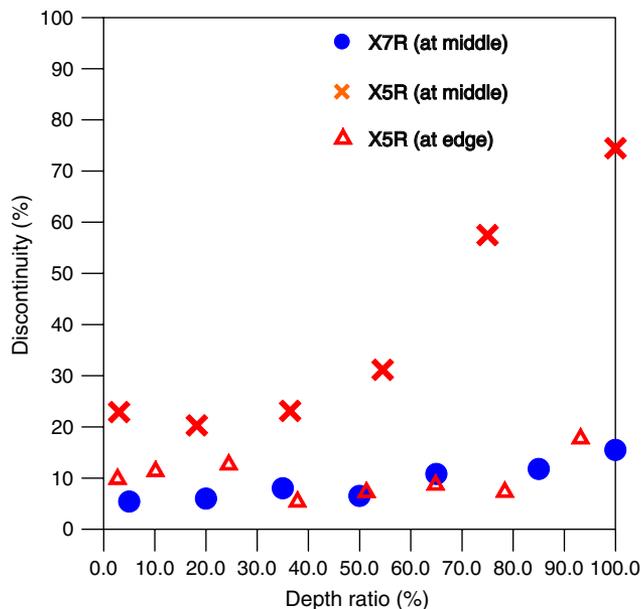


Fig. 3. Degree of discontinuity of the electrode layers of chips A and B as a function of removed depth ratio.

bottom of the chip, indicating that it was caused by the tensile force. The bottom layer underwent a tensile force if the chip bent concavely. The dielectric layers should crack first if the sintering stress is active and too strong, because the dielectric layer is three times thicker and more brittle than the metallic Ni layer. However, no dielectric layers were in a disconnected state. As the Ni layers under tensile stresses, Rayleigh instability induced at sintering temperature in the thin Ni layers might be responsible for the formation of the eye-shaped electrode layer.

(3) Distribution of Dihedral Angle

The dihedral angle, as displayed in the inset in Fig. 4, is a function of surface energies exerted on the triple junction of Ni/BT grains. The dihedral angle was measured from the magnified SEM micrographs or from TEM pictures. The angle of chip A ranged from 40° to 180°, and the average value was 115° (Fig. 4). In chip B, the dihedral angle was between 5° and 150°, averaging

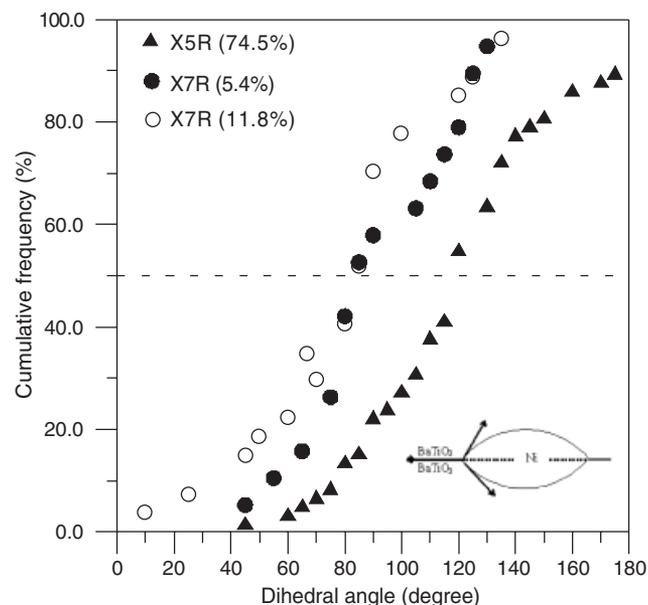


Fig. 4. Cumulative frequency vs. the dihedral angle of two multi-layer ceramic capacitor samples. The percentages shown next to the sample names are the removed depth ratio of the measured plane.

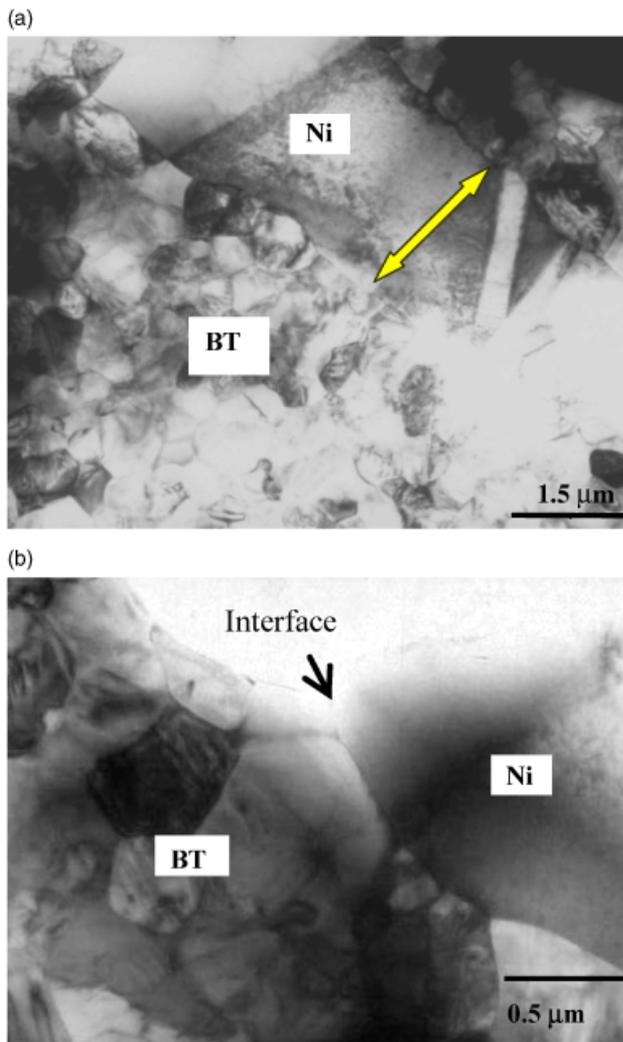


Fig. 5. Transmission electron microscope micrographs of the cross-section of (a) chip B and (b) chip A revealing the interface of the inner electrode (pointed by an arrow) and BaTiO<sub>3</sub> layer.

80°. The results showed that chip B had a better wetting property of Ni/Bt than did chip A, implying that a high dihedral angle followed Rayleigh instability that breaks up the electrode layers under tensile stresses during the solid-state sintering.<sup>4</sup>

Figure 5(a) shows the TEM bright-field image of the cross-section in chip B. There is a layer of Ni grains between the small BT particles. The boundaries of these Ni grains were large and straight, implying that the Ni grains were in the final state of sintering. The thickness of the Ni layer was about 1.2–1.5 μm, which was close to the thickness of Ni observed from SEM. The TEM image shown in Fig. 5(b) revealed a clear interface between the Ni and BT layers in chip A. There was no inter-diffusion between the Ni and BT layers. This result is consistent with the previous report on the Ni/Cu/BT system.<sup>7</sup>

IV. Conclusions

The structural defects in MLCC chips, including the warpage angle of the Ni electrode and BT layers, the dihedral angle and its distribution, and the ratio of the discontinuity of the metallic layer, were quantitatively investigated. A better connectivity of inner Ni electrode is closely linked to low warpage and narrow distribution of the dihedral angle of Ni layers relative to BT layers. Discontinuity of the Ni layers was occasionally observed, and was often found in the middle–bottom position of a concave chip, indicating that discontinuity occurred mainly by Rayleigh

instability and the influence of the tensile stresses induced from sintering.

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