

Lead-Free and Lead-Bearing Electronic Solders: Implementation, Reliability, and New Technology

C. Robert Kao



Twenty months after the banning of lead in electrical and electronic equipment by the European Union through the RoHS Directive¹ (Restriction of the use of certain Hazardous Substances in electrical and electronic equipment directive), lead-free electrical and electronic products have been in customers' hands long enough for us to assess fully their true field reliability. There is fortunately no large-scale catastrophe to report, and some people even think the lead-free transition went better than expected. Nevertheless, lead-free electrical and electronic products do have their unique problems that have to be resolved. These issues include the tin whisker problem,^{2,3} the massive spalling of intermetallic compounds,^{4,6} and the drop reliability problem,⁷ to name just a few. All of these issues were covered in the Interconnect and Packaging Technologies Symposium of the TMS 2008 Annual Meeting, March 9–13, in New Orleans.

This symposium was organized by Carol Handwerker, Srinivas Chada, Fay Hua, and Kejun Zeng. The full three-day program, covering areas in advanced interconnects, electromigration, tin whisker formation, mechanical behaviors, solidification, modeling, test methods, fundamental properties, interfacial reactions, phase transformation, and reliability, was well received by the audience. The four papers in this issue of *JOM* are selected from this excellent collection of presentations, and are authored by top experts in their respective fields.

The first paper, by K. Suganuma and K.-S. Kim, provides an in-depth analysis of the "black pad" problem, which is one of the most serious reliability concerns in the electronic industry nowadays. This article provides a detailed and up-to-date investigation of a problem that has been in existence for a long time. Two root causes responsible for failures are identified. The first is the corrosion of Ni-P during gold plating, and the second is the excess reaction of solder and Ni-P, leading to the formation of a weak phosphorous-rich layer. Strategies to mitigate the black pad problem are given in this paper.

In the second paper S.K. Kang et al. of IBM review the various solder-bumping technologies developed for flip-chip packages. Flip-chip solder joints, enjoying RoHS exemption until 2010, are among the few last places where lead-bearing solders can still be found in electronic products. The flip-chip solder joints receive the RoHS exemption because the use of lead-free solders in these joints is technologically challenging. In this paper, a new wafer-bumping technology known as C4NP (Controlled-Collapse-Chip-Connect New Process) is introduced. The development and implementation of lead-free flip-chip to 300 mm wafers is also covered.

The next paper is authored by D. Suh et al., researchers from Intel and Senju who present an excellent example of the development of an alloy for use as a low-temperature solder for electronic packaging applications. This Bi-In-based alloy can be reflowed at the relatively low temperature of 125°C, but exhibits excellent mechanical properties at high homologous temperatures. This paper demonstrates that even at a

time when SnAgCu seems to dominate in every application, opportunities still exist for new solders.

The last paper, by P.-C. Yang et al., deals with an increasingly important problem in advanced processor units, namely, the electromigration in flip-chip solder joints. Electromigration in flip-chip solder joints is a relatively new problem, and not much is understood at this stage. One of the co-authors of this paper, C. Chen, is one of the most prolific authors and top experts on the subject. This paper investigates the effect of pre-aging on lifetime during current stressing. It is found that proper pre-aging can substantially increase the solder joint lifetime. This study shows that proper processing alone is able to increase the electromigration resistance of electronic devices.

Many of the remaining papers presented at the 2008 Emerging Interconnect and Packaging Technologies Symposium will be published in the *Journal of Electronic Materials* later this year as a special issue on electronic solders.

References

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C.R. Kao is a professor with the Department of Materials Science and Engineering at National Taiwan University in Taipei City, Taiwan, and is the advisor to *JOM* and chair for the Electronic Packaging and Interconnection Materials Committee of the TMS Electronic, Magnetic & Photonic Materials Division.