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CMOS-MEMS 微鏡面裝置之設計與製作

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中文摘要

本研究利用 CMOS-MEMS 技術研製一微型鏡面陣列(micromirror array)。亦即,以積體電路晶圓代工廠所提供之標準 CMOS 0.35 μm 製程,同時配合微機電(MEMS)後製程技術來製作一數位式微型光連結裝置(digital multi-direction optical interconnect device)。主要目的乃期望能針對傳統大型光網路連結或是空間光內連結裝置的尺度和效能等提出一個切實可行的先期研發方案,此外基於光學微機電裝置之低插入損失(insertion loss) 和切換損失,此類的微型裝置亦十分切合現今所謂的短距離無線通訊(雷射通訊)之需求,如機房主機內部之 I/O 切換或是通道擷取等等。

Abstract

This work describes the fabrication of a micromachined micromirror by the conventional 0.35 μm CMOS process and a simple maskless post-CMOS process. The micromirror contains a rectangular mirror plate and four pairs of serpentine supported beams, is integrated with a 1 \times 4 demultiplexer and a four-stage charge pump circuits on a chip. Maskless dry and wet etching processes are the only requirement to suspend the structure. The primary limitation in the fabrication of microstructures has been overcome by the development of a hybrid processing technique, which combines both an anisotropic dry etch and an isotropic wet etch step. A highly reliable wet etching step with high selectivity between aluminum and sacrificial oxide is also reported. Experimental results reveal that the micromirror has a tilting angle of around 5 $^\circ$ at operation voltage of 22.5 V and a dynamic response less than 5 ms. The surface properties of the CMOS micromirror, detailed process flows, measurement set-up and the results are also presented in this work.

1. Introduction

The conventional CMOS process enables the co-integration on a single chip of mature integrated circuits with some smart mechanical microstructures. Various fabricating technologies, including LIGA, surface micromachining and bulk micromachining, have been proposed to meet particular industrial requirements. However, the specialized processes may not support the on-chip integration of MEMS devices and circuit. Therefore, the developments of a MEMS structure by a commercial CMOS batch fabrication process have attracted much attention [1, 2].

The advantages of using a micromachined micromirror are its low sensitivity to polarization and its functioning in a broad band. The development of MEMS-based mirrors for optical applications, including in projection display systems [3, 4], optical scanners [5, 6], variable optical attenuators [7-9] and other specific applications has attracted much interest recently [10]. Prior work on micromirror optical switching has demonstrated the feasibility of making surface or bulk micromachined micromirrors for light beams steering or for use in optical interconnect applications, by silicon deep etching or by the use of expensive SOI (silicon on insulator) wafers [11-14]. However, issues raised in the literature include high process complexity, high operation voltage or power consumption and process incompatibility with currently used CMOS process.

This work demonstrates a fully CMOS process compatible micromirror, which contains a mirror plate, a 1 \times 4 demultiplexer and a four-stage charge pump circuits. The standard 0.35 μm CMOS process and a completely CMOS compatible post-process

procedure are utilized to fabricate the device. The proposed micromirror is electrostatically actuated and is driven by a square wave with a 20 Hz repetition frequency. Experimental results indicate that the micromirror have a tilting angle of 5° at a driving voltage of about 22.5 V according to the triangular relationship, and a dynamic response less than 5 ms, as measured by a commercialized LDV system. The surface properties of the micromirror, detailed process flows, measurement set-up and experimental results are also presented.

2. Micromirror structure design

The device proposed herein is a micromachined micromirror using the conventional CMOS process. A 10×10 micromirror array with on chip circuits, as shown in Fig. 1, is designed as a testboard for examining the feasibility study of a fully CMOS process compatible micromirror. Therefore, this work investigating the integrating compatibility between standard CMOS process and MEMS devices, the surface quality of mirror plate after post-processing, and the measurement of the dynamic response of a micromirror. However, the total system mentioned previously, a 10×10 mirror array, is currently under test and development. Possible applications of the MEMS-based micromirrors include the optical attenuators, precise position sensors, high pixel density display without add-on bonding process or short range data transmission.

Electrostatic actuation is used to deflect the micromirror. Fig. 2(a) depicts the structure and dimensions of a mirror. It contains a top mirror plate with an aluminum layer with a thickness of $1 \mu\text{m}$, four bottom-fixed electrode plates and four pairs of supported beams. The top mirror plate is a movable electrode plate, and four bottom-fixed electrode plates are located under each side of the mirror plate. The gap between the fixed-electrode plate and mirror plate is about $5.6 \mu\text{m}$. The mirror includes four sets of parallel-plate electrodes, formed from four fixed-electrode plates and the top mirror plate. The supported beams are S-shaped serpentine structures, as indicated in Fig. 2(b). One end of the supported beams is

fixed to an anchor, which is stacked using metal layers and tungsten plugs (vias), and the other end is attached to the top mirror plate. The mirror plate is about $70 \times 70 \mu\text{m}^2$ areas and is about $1 \mu\text{m}$ thick. The area of each fixed-electrode plates is $25 \times 28 \mu\text{m}^2$. The mirror plate and the supported beams used in the CMOS process are all made from metals. All anchors comprise stacked metal and via layers. The top mirror plate is electrically connected to highly phosphorous-doped (p^+ doped) region in the silicon substrate to yield the same electrical potential between mirror plate and p^+ doped region.

For the operation of proposed micromirror, in the unactuated state, the mirror plate exhibits no action in relation to the fixed electrode plate, accounting for the fact that the angle between the incident and reflective light beams is almost the same because aluminum is highly optically reflective ($> 90\%$) [15]. Fig. 3 also shows a plot of micromirror reflectivity versus the thickness of metal coating for four different metals according to the simulated result by a commercial optical simulation tool - G-Solver. The wavelength of light used is $1.3 \mu\text{m}$ and the simulation is taken for normal incidence. No other metal coating add-on process is required in this work since the mirror plate is made by aluminum and the deposited oxide layer beneath the aluminum is polished by chemical-mechanical-polishing (CMP) in CMOS process. In the actuated state, a voltage is applied to a fixed electrode plate and to the top mirror plate. The mirror plate is pulled down by the electrostatic force, which changes the direction of the reflective light. The micromirror has four operating modes, because of the set-up of four parallel-plate electrode sets.

The electrostatic force, F_s , generated between the plates by the applied actuating voltage, V_{DC} , can be derived by considering the energy, E , stored between the plates.

$$F_s = \frac{\partial E}{\partial d} = \frac{1}{2} \frac{\partial C}{\partial d} V_{DC}^2 = \frac{1}{2} \frac{\epsilon_r \epsilon_0 A V_{DC}^2}{d^2} \quad (1)$$

Where A is the effective area of the plates; d is the air gap between the two plates, and ϵ_0 and ϵ_r are the permittivity of free space and

the relative permittivity, respectively. Hence, a normal out-of-plane force, F_s , is applied across an air gap, d , between the fixed electrode plate and the top mirror plate, resulting in a deflection.

The finite element method software, CoventorWare, is utilized to simulate the behaviors of the mirror. Fig. 4 illustrates the stress distribution of the micromirror in the actuated state. The deformation in the actuated state almost wholly occurs in the S-shaped flexures of the supported beams. The maximum stress, 13 Mpa, is below the yield strength of aluminum, about 90 Mpa, and thus the deformation of the micromirror can be operated in elastic range. Fig. 5 presents the relationship between the applied voltage and the tilting angle of the mirror plate. The maximum tilting angle of the micromirror is about 5° at a voltage of 22.5 V. The measured tilting angle deviates from the simulated tilting angle at the applied voltages above 10 V. This deviation is attributed mainly to the slightly softening of the supported beams after ion-bombardment in the reactive ion etching (RIE) processing step or the uncertainty in the exact geometry of the micromirror in the foundry process.

The circuit presented in this work has a 1×4 demultiplexer digital circuit and four four-stage charge pump circuits. Fig. 7(a) displays the simulated relationship between the input and output voltage of the 1×4 demultiplexer. The first four signal curves correspond to the output ports (outputs 1, 2, 3 and 4), which are connected to the four bottom-fixed electrode plates (bottom electrode pads 1, 2, 3 and 4) in the mirror, respectively. The last two signal curves are the input signal. Fig. 7(b) presents the truth table of the circuit. For example, if the input signal is set to A=1 (high) and B=0 (low), then the output signal will be sent into output port 2. A voltage signal would be then applied to the bottom-fixed electrode plate (pad 2) to pull down the mirror plate.

The MOS transistor fabricated by the $0.35\mu\text{m}$ CMOS process cannot be operated at over 5 V. Care must be taken to ensure the compatibility between the MEMS devices commonly operated at a higher voltage and the

currently used low-voltage MOSFET. Fig. 8 depicts a single-stage two-phase charge pump, compatible with low-voltage transistors [16]. The charge pump circuit is a cascade of voltage doubler stages; each stage can be realized with four low voltage MOS transistors and a pair of capacitors. The circuit is operated according to a two-phase clocking scheme and no specific output stage is required. After an initial transient state, the circuit enters a stationary state is reached. The output voltage is about 9.6 V at $1.3\mu\text{sec}$ from simulation. However, the output voltage does not suffice to drive the micromirror. Therefore, a cascaded four-stage charge pump is used to augment the output voltage. Fig. 9 plots the simulation results of the four-stage charge pump circuit. The final stage output voltage is about 24 V at $8\mu\text{sec}$. However, the real output voltage measured by the circuit is about 22.5 V, is smaller than the result of circuit simulation. Each output port in the 1×4 demultiplexer, as shown in Fig. 6, is connected to a four-stage charge pump then the output voltage of the 1×4 demultiplexer can be augmented to about 24 V.

3. Device fabrication

The micromachined micromirror is developed according to the Taiwan Semiconductor Manufacture Company (TSMC) CMOS foundry service and design rules. All post-process procedures require only maskless dry and wet etching and thus avoid the sticking problem. The post-CMOS process has two major steps. The process flow in Fig. 10 illustrates the development of CMOS compatible micromirror structure in cross section. Fig. 10(a) describes the schematic cross-sections view after TSMC process. Parts of the passivation nitride on the chip were removed in advance, and the top metal layer was exposed. The oxide layers under the mirror plate and the supported beams are sacrificial layers. Two main steps are involved in the post-CMOS process. Fig. 10(b) illustrates the use of anisotropic dry etching with CF_4/O_2 to etch the sacrificial oxide layers. This step removes some of the silicon dioxide beneath the top metal layer and forms some cavities through the etching holes. The suspended

structures of the micromirror are not all released. Accordingly, isotropic wet etching of oxide must be performed to release the incomplete suspended parts, as shown in Fig. 10(c). This step was completed using BOE (6 parts 40% NH_4F and 1 part 49% HF) and isopropyl alcohol solution (IPA). Critically, this step enhances the etching selectivity between Aluminum and silicon dioxide during wet etching by adding IPA to BOE solution. The suspended structure of the micromirror is released completely, and no sticking occurs after the overall post-processing. However, the etch time must be precisely controlled, to prevent a short circuit which could be caused by leaving a thin oxide layer to cover the bottom-electrode plates.

Table 1 summarizes the dry and wet etching steps along with the experimental parameters. The ratio of tetrafluoromethane (CF_4) and oxygen (O_2) is the decisional recipe when CF_4/O_2 RIE are applied to etch silicon dioxide anisotropically. Combining lower O_2 flow and low pressure produces a thin polymer passivating film on the silicon dioxide sidewall that inhibits lateral etching. As for the wet etching step in the final procedure, it is well known that one of the most difficult fabrication steps in surface micromachining is the sacrificial etch step and subsequent releasing of the moveable structures. Especially when aluminum is used as the main structures or the interconnect layers it is difficult to selectively etch the sacrificial oxide without attacking the aluminum. Traditional methods to prevent aluminum attack during sacrificial oxide etching are the protection of the metallization using photo-resist (PR) and the use of alternative etch solution like ‘pad-etch’ [17] or HF vapor etching technique. However these methods have disadvantages: PR protection is only possible when etch time are limited to several minutes due to adhesion problems. Special etch mixtures or methods can offer reasonable selectivity, but have a low oxide etch rate (pad-etch) and without a standard set-up of the etching process (HF vapor etching technique). In this work, an approach to etch sacrificial oxide with special procedure is proposed, as illustrated in Table 1. Addition of

IPA to the BOE is preferred since this makes it possible to maintain a liquid film on the surface the microstructures when they are taken out of the etching solution. The CMOS-MEMS chip should not be rinse in water for a long time, because water addition to the HF-based solution will result in rapid attack of the surface of aluminum due to the violent chemical reaction between hydrogen and oxygen ions. Fig. 11 shows some photographs of the micromirror structure following the post-CMOS process by SEM or optical microscope.

To reduce the operation voltage and to improve the performance, the S-shaped flexures must be bended or rotated like a pin joint-like mechanism and, in so doing, move smoothly and farther than otherwise. In the CMOS foundry service adopted herein, the via layer constitutes a tunnel in the oxide layer between the two metal layers. The use of the via layer to connect each metal layer not only expands the electrode, but also acts as an anchor, fixing the microstructure onto the silicon substrate. The suspended mirror plate and supported beams are made of the top metal layer (metal 4). Many etching holes are also designed in the mirror plate to reduce the etching time during the process.

In the previous design, a circular micromirror is also fabricated by CMOS process, as shown in Fig. 12. Owing to the violating of design rule which provided by IC foundry, several caves or grooves are formed on the top mirror plate and this design clearly is not suitable for the reflective type optical devices. Consequently, the proposed micromirror modifies the flatness and surface quality by obeying the minimum dimensions of the tungsten plugs (vias) and the metal layers without any violation of the design rules.

4. Experimental results

Fig. 13 shows the experimental set-up of the CMOS-MEMS micromirror. The top mirror plate and bottom-fixed electrode plate of the micromirror are connected to the grounded pad and the positive power pad, respectively, of the power supply system. A square wave with peak voltage of 22.5 V is applied to the mirror by the

circuit. The top mirror plate begins actuation around 15 V, as observed under a microscope. The switching dynamics is measured using a commercial laser-Doppler vibrometer (LDV) system (AVID). The response time is shown in Figs. 14(a) and (b). The rise time, corresponding to the recovery state of the micromirror, is about 3 ms and, the fall time, corresponding to the pulled-down state is 4.3 ms. The response time is fast enough for several MEMS micromirror applications.

Additionally, the surface quality of the mirror is also the important determiner of the success of various optical applications that requires a reflective type mirror with a surface roughness of better than one tenth of the wavelength and a larger radius of curvature, to ensure the flatness of the mirror. In this investigation, the surface roughness and curvature of the mirror were determined using an instrumental interferometer, the WYKO MHT III system, a non-contact, three-dimensional optical interferometric profiler. The root-mean-square (RMS), average roughness (Ra), and radius of curvature () of the surface were measured at 31.91 nm, 27.80 nm, and 58 mm, in the X-direction, and 36.31 nm, 30.87 nm, and 49 mm in the Y-direction, respectively, as shown in Figs. 15(a) and (b). These measurements reveal that the surface scattering is acceptable for commonly used reflective type optical components and verifies the compatibility between the standard IC process and the post-CMOS micromachining technology.

5. Conclusion

This work presents details of the design and fabrication of a micromachined micromirror by a fully compatible CMOS process. Experimentally, in this study we perform maskless etching process and obtain good results including high selectivity in wet etching and full release without damages of the structure or circuit. A highly reliable wet etching procedure with high selectivity is also reported in this work. Finally, the micromirror has a tilting angle of approximately 5° at an operation voltage around 22.5 V. The switching times are 3 ms and 4.3 ms for the rise and the

fall times, respectively. The whole procedure is simple and compatible with the CMOS process. This investigation not only reduces the developing time, but also minimizes the scale by following the advancing CMOS process. The micromirror proposed herein has a monolithic integration capability with circuits and is potentially for future applications in optics or other fields by the advanced VLSI process. For instance, some VLSI foundries have provided the thick top metal layer (2 or 3 μm) already for mixed signal or RF circuit. That will be a good option to develop CMOS-MEMS devices with better material property and device performance.

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Table 1 Experiment parameters of the dry and wet etching steps

Etch recipes for the sacrificial oxide		
Dry etching		BCE / IFA Wet etching
$CF_4 + O_2$		BH_3F (40%) + HF (40%) : 1
Pressure (mTorr)	10	Steps:
Power (Watt)	100	1. Acetone/ H_2O : 20 min (clean process)
Gas flow (sccm)	$36.8 CF_4 + 4 O_2$	2. BCE/IFA (9:1) : 40 min (etching step)
Temp. ($^{\circ}C$)	25	3. IFA : 15 min
Etch rate ($\text{\AA}/\text{min}$)	~ 300	4. H_2O : 5 min (remove reaction product on the top metal surface)
		5. IFA (or Acetone) : 15 min (rinse)
		6. Hot bake (120 $^{\circ}C$ for 30 min)
		Etch rate ($\text{\AA}/\text{min}$)
		~ 2500 (low etch rate but good selectivity)

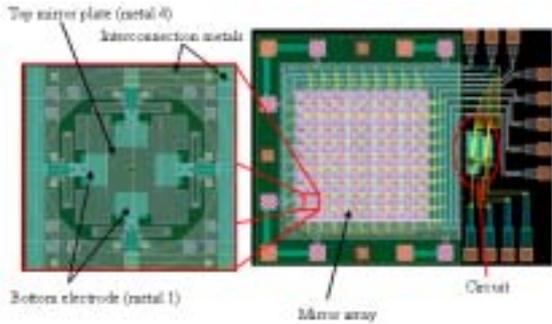


Fig. 1. Layout of the micromirror array with circuits.

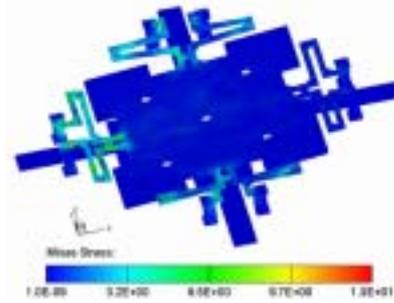


Fig. 4. Stress distribution in a micromirror structure.

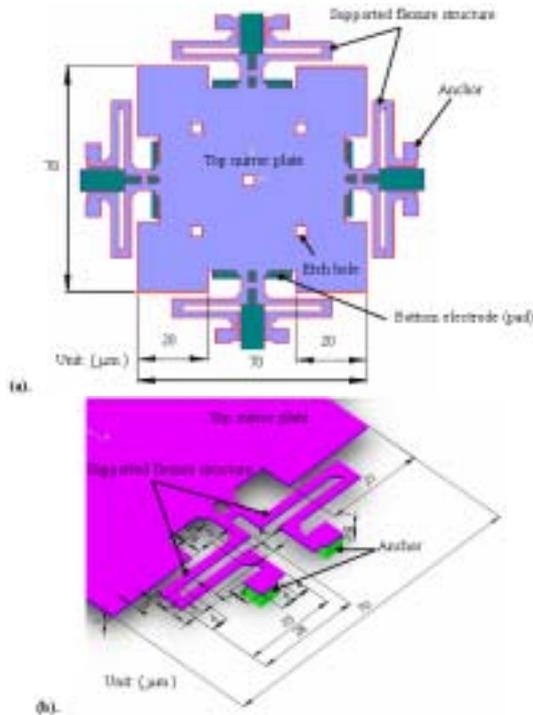


Fig. 2. Structure and dimensions of a micromirror structure: (a) mirror plate and fixed bottom electrodes, (b) flexural supported beams.

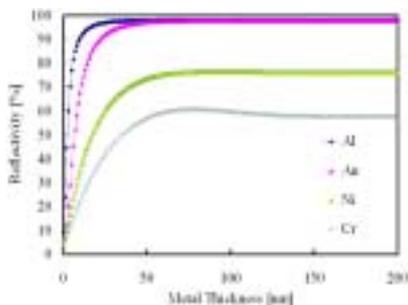


Fig. 3. Reflectivity as a function of metal thickness.

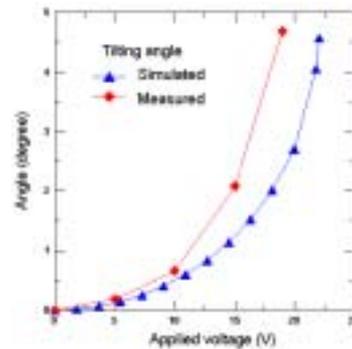


Fig. 5. Angular displacement versus applied voltage.

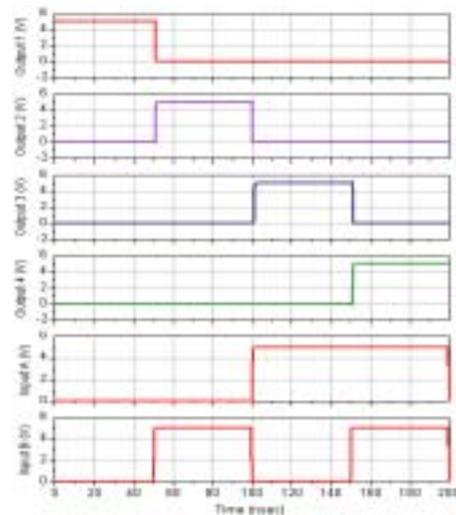


Fig. 7. Simulation of a 1×4 demultiplexer: output waveforms of the circuit, or the behavior of a micromirror when a 1×4 demultiplexer circuit is used.

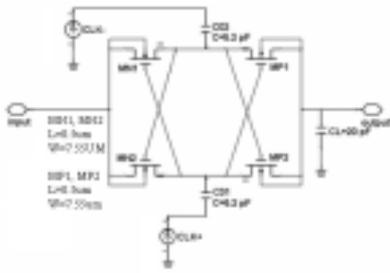


Fig. 7. Schematic of the single stage charge pump circuit.

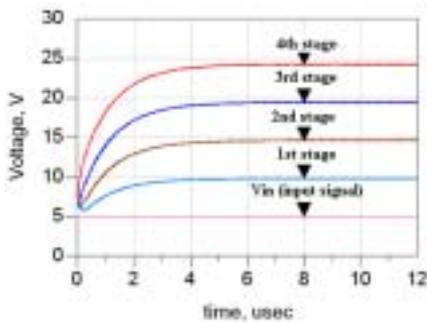


Fig. 8. Simulated signals obtained using cascaded four-stage charge pump circuit.

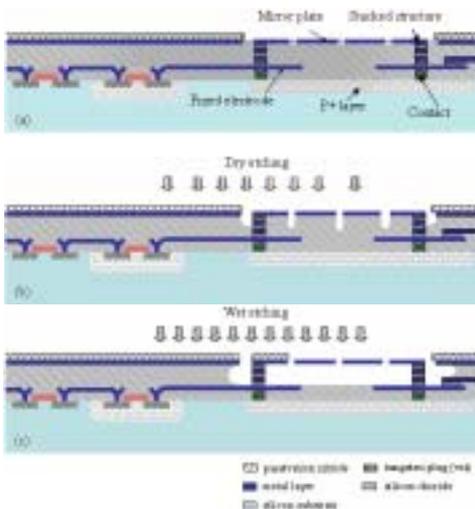


Fig. 9. Schematic process flow: (a) completion of the CMOS foundry process; (b) etching silicon dioxide layer by RIE; (c) removing silicon dioxide layer by BOE / IPA solutions.

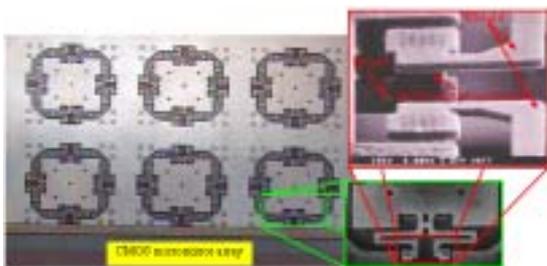


Fig. 10. Pictures of the micromirrors after the post-CMOS process.

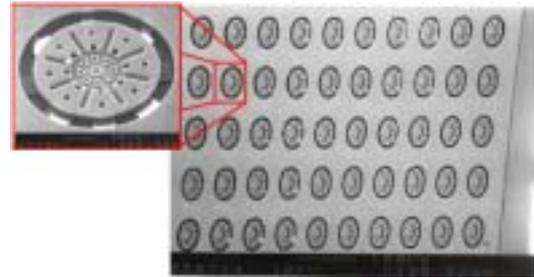


Fig. 11. SEM pictures show a circular micromirror array which violates the design rules. (Previous work)

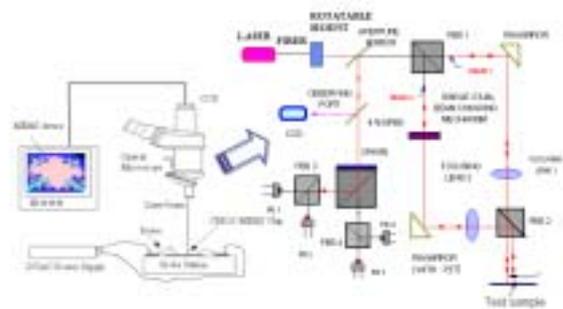


Fig. 12. Schematic optical measurement device (AVID) for the CMOS micromirror device.

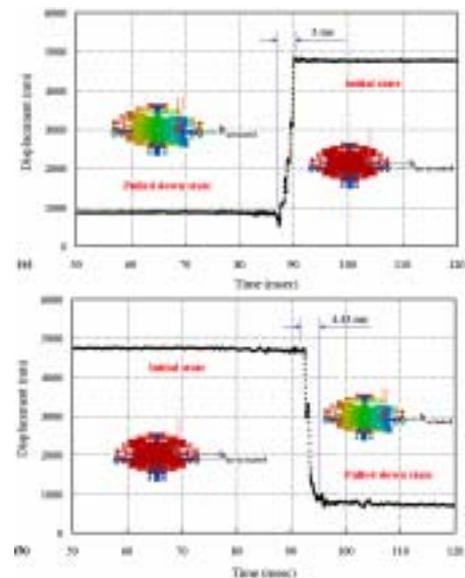


Fig. 13. The switching time of a micromirror: (a) rise time (3 ms) at the voltage released; (b) fall time (4.3 ms) with respect to the operation voltage (22.5 V).

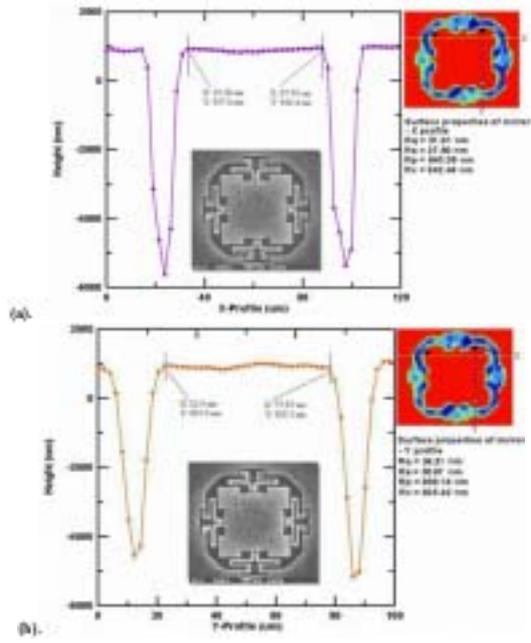


Fig. 14. Surface quality of the mirror plate obtained by WYKO interference measurement system: (a) X-direction profile; (b) Y-direction profile.