

LONG EDGES IN THE LAYOUTS OF SHUFFLE-EXCHANGE AND CUBE-CONNECTED CYCLES GRAPHS

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A direct method is devised to prove, without information-theoretic arguments, the $\Omega(N^2/\log^2 N)$ wire area lower bound for the shuffle-exchange and cube-connected cycles graphs. We further show the high occurrence of long edges in two ways: (1) In any layout, there are $\Omega(N/\log N)$ edges whose lengths are at least $N/32 \log^2 N$. (2) The edges whose lengths are at least $N/64 \log^2 N$ occupy $\Omega(N^2/\log^2 N)$ wire area.

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1. Introduction

In VLSI computation, if a solution to some problem is in the form of a communication graph of processors, an efficient layout is desired to implement the graph. Minimizing wire area is a critical concern due to the fact that layouts consuming a larger amount of chip area are more expensive to fabricate and less reliable. Speed of course is another critical factor in chip performance. Long wires raise propagation delays which can slow down the clock and hence reduce the throughput of the system. These are two of the major VLSI layout problems which have stimulated considerable interest in theoretical study [1].

For the formal model of VLSI graph layouts, we shall adopt the simple and widely accepted grid model [6,7]. Layouts are assumed to be on rectangular grids formed by horizontal and vertical grid lines which are spaced apart by unit intervals. The nodes of a graph are located only at the intersections of grid lines—the grid points. Edges are routed as wires through the grid lines to

connect nodes. Any two edges are not allowed to overlap for any distance, and an edge cannot overlap any node which is not an end-node of that edge. The layout area is defined to be the number of all grid points in the grid. The wire area, however, is the count of those grid points covered by the edges.

The shuffle-exchange [5] and cube-connected cycles [4] graphs are two pre-eminent structures for parallel computation because of their economic interconnection patterns. In them, the hardware cost and efficiency are traded off in search of the best compromise for a contemplated range of applications. Thompson [6] first showed that any layout of a graph which computes an N -point Fourier transform in T steps requires $\Omega(N^2/T^2)$ chip area. This implies that any layout of the N -node shuffle-exchange or cube-connected cycles graph requires $\Omega(N^2/\log^2 N)$ chip area. For the proofs, see also [7]. Leighton [3] then proved an analogous but stronger lower bound statement for the wire area. He also proved that any graph which computes an N -point Fourier transform

must have a wire which crosses $\Omega(N/T^2)$ other wires. This, in particular, means that any layout of the N -node shuffle-exchange or cube-connected cycles graph contains a wire of $\Omega(N/\log^2 N)$ length.

All the lower bound results mentioned above are indirectly derived through information-theoretic (area-time tradeoff) arguments. In this paper, we shall devise a method to prove these lower bounds directly. The basic idea is roughly as follows. If we separate some or all of the nodes of the graph into two parts, between them there must be at least a certain amount of communicating paths. According to the interconnection pattern of the graph, removing one edge can only destroy some communicating paths, hence there must be at least a certain number of edges connecting these two parts. By using this kind of information, we are not only able to derive wire area lower bounds but also lower bounds on the number of long edges. In fact, we strengthen Leighton's result by showing that there are $\Omega(N/\log N)$ edges which are at least $N/32 \log^2 N$ long. Furthermore, we show that the wire area occupied by the edges whose lengths are at least $N/64 \log^2 N$ is as large (up to a constant) as the whole wire area.

2. Communication power of edges

In order to extract the communication ability of a given graph, we shall consider 'path-edges' which are paths properly selected from the original graph. The concept of 'path-edge' will become explicit when we deal with those two particular graphs in the next section. We need a few definitions for describing the communication power of edges. 'Edges' used in this section really are 'path-edges' when applied to concrete examples in the next section.

Definition 2.1. The *diameter* D of a given graph is the smallest integer such that, for any two nodes i and j , i can be connected to j in at most D steps.

Definition 2.2. Let e be any edge, $1 \leq d \leq D$, $1 \leq h \leq d$. A *communication circle* can be defined as the set of node pairs

$$C(e, d, h) = \{ (i, j) \mid i \text{ and } j \text{ are nodes such that there is a } d\text{-step path from } i \text{ to } j, \text{ with } e \text{ as the } h\text{th step in the path} \}.$$

Definition 2.3. If e is an edge, we define the *pairing set* of e as

$$P(e) = \{ (i, j) \mid i \text{ and } j \text{ are nodes such that there is a path from } i \text{ to } j \text{ through } e \text{ and the number of steps in the path is at most } D \}.$$

To serve our purpose, we should constrain the graphs to be of bounded degree. In this paper, we are only interested in the case that the in-degree and out-degree of each node are bounded by 2, although the results obtained here can be extended naturally. The following easy lemma can be used to bound from above the size of communication circles and pairing sets.

Lemma 2.4. *If the diameter is D and the degree bound is 2, then, for any e , $1 \leq d \leq D$, $1 \leq h \leq d$,*

- (a) $|C(e, d, h)| \leq 2^{d-1}$,
- (b) $|P(e)| \leq D(2^D - 1)$.

Proof. (a) In $C(e, d, h)$, let m count the starting nodes with multiplicity and n count the ending nodes with multiplicity. It is clear that $m \leq 2^{h-1}$ and $n \leq 2^{d-h}$. So,

$$|C(e, d, h)| \leq mn \leq 2^{h-1} 2^{d-h} = 2^{d-1}.$$

(b) Since

$$P(e) = \bigcup_{1 \leq d \leq D, 1 \leq h \leq d} C(e, d, h),$$

we have

$$\begin{aligned} |P(e)| &\leq \sum_{d=1}^D d 2^{d-1} \leq D \sum_{d=1}^D 2^{d-1} \\ &\leq D(2^D - 1). \quad \square \end{aligned}$$

If we purposely choose a set of nodes S to be observed, we can define the communication power of an edge relative to that set as the number of communicating pairs through that edge with both starting and ending nodes in S . Also, the diameter,

if necessary, should be reduced to fit the situation of the set of observed nodes.

Definition 2.5. Suppose S is a set of observed nodes and e is any edge in the graph. We define the communication power of e relative to S as

$$P_S(e) = \{(i, j) \mid i, j \in S \text{ and } (i, j) \in P(e)\},$$

and define

$$R_S = \max_e |P_S(e)|.$$

3. Shuffle-exchange and cube-connected cycles

The shuffle-exchange graph consists of $N = 2^n$ nodes as shown for $n = 3$ in Fig. 1. Each node is associated with a unique n -bit binary number. Node i is linked to j via a shuffle edge (uni-directional dashed line) if j is the left cyclic shift of i . Two nodes i and j are linked via an exchange edge (bi-directional solid line) if i and j differ only in the rightmost bit. According to the interconnection pattern, any two nodes can be connected through a path of at most $2n = 2 \log N$ steps.¹ This is not good enough, and we should combine edges to lower the diameter somewhat. If we consider the shuffle-then-exchange and shuffle-only paths as the ‘path-edges’, we arrive at a new graph whose diameter is $\log N$ only. We shall observe all nodes in the graph, so $P_S(e) = P(e)$ for any e , and hence $R_S \leq N \log N$ by Lemma 2.4(b).

The cube-connected cycles graph consists of $N = n \log n$ nodes, organized as $\log n$ ranks of n nodes each. One example for $n = 2^3$ is shown in Fig. 2. Let us denote the i th node on the r th rank by p_{ri} . Node p_{ri} is linked to node $p_{r+1,i}$ via a cycle edge (uni-directional dashed line), where r is taken as an integer mod $\log n$. Node p_{ri} is also linked to p_{rj} on the same rank via a cross edge (bi-directional solid line) if i and j only differ in the r th bit from the right. We can select any rank, say rank 0, as the set of observed nodes S . Any two nodes in S can be connected through a path of at most $2 \log n$ steps. Again, this is not good enough, and we should consider the cycle-then-cross and cycle-only



Fig. 1. Shuffle-exchange graph.

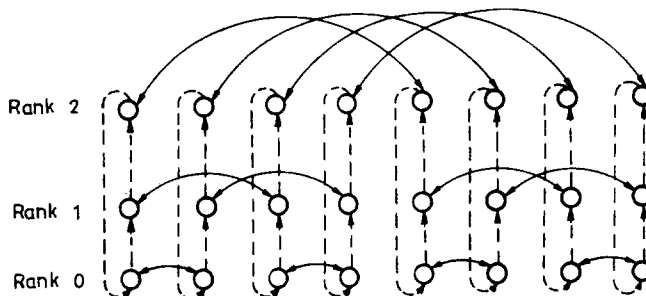


Fig. 2. Cube-connected cycles graph.

paths as the ‘path-edges’ and reduce the diameter to $\log n$. It is not hard to see that, for any edge e , $P_S(e) = C(e, \log n, h)$ for some h . Therefore, from Lemma 2.4(a), we know that $R_S \leq 2^{\log n - 1} = \frac{1}{2}n$.

4. Wire area and long edges

We will use a “#” sign partition technique due to Leighton [3] to prove wire area lower bounds and lower bounds on long edges. We observe the diagram in Fig. 3, where a given graph is laid out arbitrarily. We slice it vertically by two boundaries b_1 and b_2 with a single jog each, so that $\frac{1}{8}|S|$ observed nodes are to the left of b_1 , and the same number to the right of b_2 . Similarly, we divide the layout horizontally by another two boundaries, with $\frac{1}{8}|S|$ observed nodes above and below the top and bottom boundaries. We assume, without loss of generality, that the width w of the center rectangle is as great as the height.

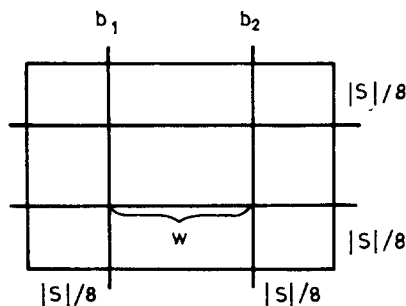


Fig. 3. “#” sign partition of layout.

¹ Throughout this paper, \log represents the base-2 logarithm.

Lemma 4.1. $w \geq |S|^2/32R_S$.

Proof. The number of observed nodes in the center rectangle is at least $\frac{1}{2}|S|$, and there are at least $\frac{1}{4}|S|$ in the rest area. So, there are at least $\frac{1}{2}|S| \times \frac{1}{4}|S| = \frac{1}{8}|S|^2$ node pairs across the perimeter of the center rectangle. By the definition of R_S we know that the perimeter should cut at least $|S|^2/8R_S$ edges. Hence,

$$4w \geq |S|^2/8R_S \quad \text{or} \quad w \geq |S|^2/32R_S. \quad \square$$

Lemma 4.2. *The wire area of any layout is $\Omega(|S|^4/R_S^2)$.*

Proof. Any vertical boundary between b_1 and b_2 must cut at least $(\frac{1}{8}|S| \times \frac{1}{8}|S|)/R_S = |S|^2/64R_S$ edges. Consequently, the occupied wire area between b_1 and b_2 is at least

$$w(|S|^2/64R_S) = |S|^4/(32 \times 64R_S^2). \quad \square$$

Theorem 4.3. *Any layout of the N -node shuffle-exchange or cube-connected cycles graph occupies $\Omega(N^2/\log^2 N)$ wire area.*

Proof. For the shuffle-exchange graph, as discussed in the previous section, we have $R_S \leq N \log N$, where $|S| = N$. By Lemma 4.2, we get the desired wire area lower bound. For the cube-connected cycles graph, $|S| = n$ and $R_S \leq \frac{1}{2}n$, therefore the wire area, by Lemma 4.2, is $\Omega(n^2)$, i.e., $\Omega(N^2/\log^2 N)$. \square

As regards Fig. 3 again, an observed node left to b_1 can be connected to any observed node right to b_2 by a path whose length is at least w . The average edge length in the path is at least w/D if the number of steps is not greater than D . So we are sure that there must be one edge in the path whose length is at least w/D . Such an edge is considered to be long.

Lemma 4.4. *In any layout, there are $\Omega(|S|^2/R_S)$ edges whose lengths are at least w/D .*

Proof. In any path connecting an observed node left to b_1 to an observed node right to b_2 , there is

at least one edge whose length is at least w/D . But such an edge can communicate at most R_S node pairs. We thus conclude that there are at least $(\frac{1}{8}|S| \times \frac{1}{8}|S|)/R_S = |S|^2/64R_S$ edges whose lengths are at least w/D . \square

Theorem 4.5. *Any layout of N -node shuffle-exchange or cube-connected cycles graph contains $\Omega(N/\log N)$ edges whose lengths are at least $N/32 \log^2 N$.*

Proof. The proof immediately follows from Lemmas 4.1 and 4.4. \square

For both graphs, if we take the sum of the lengths of the long edges, we find that the wire area occupied by the long edges is $\Omega(n^2/\log^3 N)$, which is slightly smaller than the lower bound of the whole wire area by a factor of $\log N$. Nonetheless, we can match up these two bounds by considering half-long edges also.

Lemma 4.6. *In any layout, the wire area occupied by the edges whose lengths are at least $w/2D$ is $\Omega(|S|^4/R_S^2)$.*

Proof. Use the same layout partition as before. In any path connecting an observed node left to b_1 and an observed node right to b_2 , if the total length of the path is L ($\geq w$) and there are y ($< D$) edges whose lengths are less than $w/2D$, then the length sum of the edges whose lengths are at least

$$\begin{aligned} w/2D &\geq L - yw/2D \geq L - yL/2D \\ &= L(D + (D - y)/2D) \geq \frac{1}{2}L. \end{aligned}$$

Recall that in the proof of Lemma 4.2 we estimate the whole wire area ($= \Omega(|S|^4/R_S^2)$) by this kind of paths. Since at least half of the length of these paths is occupied by those long and half-long edges, we have proven the lemma. \square

Theorem 4.7. *In any layout of N -node shuffle-exchange or cube-connected cycles graph, the wire area occupied by the edges whose lengths are at least $N/64 \log^2 N$ is $\Omega(N^2/\log^2 N)$.*

5. Concluding remarks

Another popular interconnection-economic structure is the butterfly (or unfold shuffle-exchange) graph [5], which is illustrated in Fig. 4. Unlike the cube-connected cycles graph, its cycle edges, instead of wrapped, are ended at the extra top rank. Besides, the cycle-then-cross and cycle-only paths in the cube-connected cycles graph are now considered as edges instead of 'path-edges' in the butterfly graph. Without altering the matter of layout complexity, we can view the vertical-up edges as bi-directional, and consider each vertical-up path from $p_{\log n+1,i}$ to p_{0i} as a 'path-edge'. If we observe rank 0, the relative diameter is $\log n + 1$ and $R_S \leq 2^{\log n+1-1} = n$. As a consequence, all the lower bounds previously obtained for the cube-connected cycles graph also apply to the butterfly graph.

The layout depicted in Fig. 4 is already chip area optimal for the butterfly graph. Chip area optimal layouts for the shuffle-exchange and cube-connected cycles graphs can be found in [2] and [4] respectively. As mentioned in [3], the wire area is worth minimizing because chips with lower

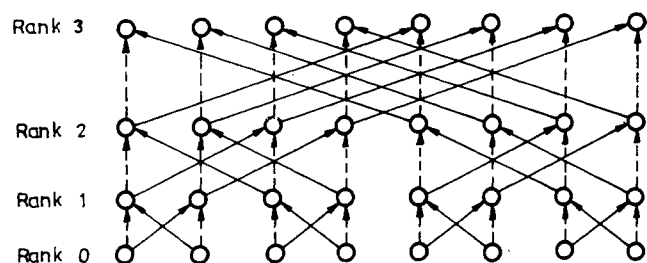


Fig. 4. Butterfly graph.

wire density will be less likely to be ruined by localized random errors. Unfortunately, the wire area is usually as large (up to a constant⁰ as the chip area. We redo the proof by baring down the nature of the interconnection patterns to avoid using any information-theoretic argument.

Along this line of proving process, we establish some lower bounds for the long edges. Our results indicate that there are somehow two very long edges which occupy at least a constant portion of the whole chip area. Drivers, which cost extra area, must be added to the long edges to either synchronize or speed up the system. Since long edges are 'almost everywhere', it will surely take a lot of engineering efforts to put these graphs on chips.

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