行政院國家科學委員會專題研究計畫 成果報告

單晶微波/毫米波雙向放大器之研製
研究成果報告(精簡版)

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□期中進度報告

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計畫參與人員：謝繼開，黃智宇

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單晶微波/毫米波雙向放大器之研製

Research and Development of Monolithic Microwave/Millimeter-wave Bi-directional Amplifiers

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一、中文摘要 (關鍵詞：雙向放大器，單晶微波/毫米波積體電路，薄膜微帶線)

本計畫為開發微波/毫米波之雙向放大器電路，實現的方法將使用互補式金氧半導體之積體電路技術。計畫目標是研究利用矽基製程技術，開發單晶微波/毫米波雙向放大器。本研究將利用在矽基板上的薄膜微帶線架構，開發雙向放大器中所需的微波/毫米波被動元件。雙向放大器設計中將使用薄膜微帶線與相關被動元件，以達到高效能、縮小化之晶片面積。

Abstract (Keywords: bi-directional amplifier, MMIC, TFMS)

This project proposes the research and development of the monolithic microwave/millimeter-wave bi-directional amplifiers using Si-based process technology. The major target of this project is to develop the Si-based monolithic microwave/millimeter-wave integrated circuit (MMIC) bi-directional amplifiers. This research will use the thin-film microstrip line (TFMS) on Si substrate and develop the microwave/millimeter-wave passive components for the bi-directional amplifier. The thin-film microstrip line and the related passive component will be used for the bi-directional amplifier design to achieve high performance and miniature chip size.

二、計畫緣由與目的

近年來無線通訊的高度發展，目前已經有許多無線通訊的產品應用於微波與毫米波的頻帶。例如全球衛星定位系統(GPS)、行動電話、無線區域網路(WLAN)、無線個人區域網路(WPAN)、無線電識別系統(RFID)、微波遙測(remote sensing)、衛星通訊、汽車防撞系統等。各種應用的快速發展發展使得頻帶的需求也日益殷切，也因此促使通訊系統向更高的頻段發展。隨著各類型的行動式無線通訊的普及，對於硬體的的需求也更朝向輕薄短小的目標發展。為了達到系統輕薄短小的要求，並且降低硬體製造成本，提高電路的可靠度，達成單一晶體化與多功能化，使用單晶毫米波積體電路(MMIC)的方式來實現是較佳的選擇[1]-[3]。

一般通訊系統的射頻前端收發器(transceiver)主要包含了發射電路(transmitter)、接收電路(receiver)與本地振盪訊號源(LO source)，如圖一所示。在發射電路中主要包含了功率放大器(power amplifier)、升頻混頻器(up-conversion mixer)與低通濾波器(LPF)；而接收電路中則為低雜訊放大器(low-noise amplifier)、降頻混頻器(down-conversion mixer)與低通濾波器。在一般分時多工(TDMA)的系統中是利用單刀雙擲切換器(SPDT switch)來達成選擇訊號路徑為發射路徑或是接收路徑。

為了簡化整個收發器的架構，縮小收發器的面積並且降低製造成本，我們可以使用雙向收發器的概念。在此雙向收發器中，我們可以使用被動混頻器的設計，即可同時達到升頻與降頻的功能。除此之外，我們則需要將低雜訊放大器與功率放大器整合成一

雙向放大器(bi-directional amplifier)，如圖二所示。因此如何設計特性良好的雙向放大器即是一重要的研究課題。

在微波與毫米波頻段，近年來有部分雙向放大器的相關研究文獻[4]-[8]。使用 MIC 實現的雙向放大器，其操作頻率低於 10 GHz，此電路是利用反射增益來實現全雙工的雙向放大器[4]-[5]。而操作頻率高於 10 GHz 甚至到毫米波頻段的雙向放大器則是採用砷化鎵高速電子移動率電晶體的積體電路技術來實現[6]-[8]。

相較於矽基積體電路(CMOS and SiGe BiCMOS)製程技術而言，以砷化鎵或磷化銦的積體電路技術所製作的電路具有較佳的增益與雜訊特性，因此過去操作頻率高於 20 GHz 電路幾乎都是使用砷化鎵或磷化銦積體電路製程技術。然而近年來矽基積體電路製程技術的快速發展，而矽基製程應用在微波與毫米波頻段的電路亦有相當的進展[9]-[15]。由於矽基製程具有高度積體化、低價格、省電等優點，因此其在微波與毫米波電路的應用受到相當大的注目。但受限於材料特性，其基板的的高頻介質損耗遠高於砷化鎵或磷化銦等材料，因此所設計製作的電路特性往往較為不理想。但是在研究上，仍可以發展應用在商用矽基製程上的特殊傳輸線架構，以降低介質損耗對電路特性的影響。一般可以使用共面波導(coplanar waveguide, CPW)或薄膜微帶線(thin-film microstrip line, TFMS)等特殊傳輸線。

在這個研究計畫中，我們利用國家系統晶片中心(CIC)所提供之 0.18 微米 CMOS 製程來開發微波/毫米波頻段雙向放大器。

三、研究方法與結果

最基本的雙向放大器可以採用將低雜訊放大器、功率放大器與兩個單刀雙擲切換器做整合設計，如圖三所示。此一架構所需要的元件與傳統收發機相仿，因此並不能達到使用雙向放大器進而縮小晶片面積的目的。為了達到減少元件數目，我們可以重複使用放大器元件(re-used amplifier)，並利用切換器做路徑的切換，如圖四所示。如此一來則可以縮小晶片所需要之面積。

以下是我們使用 0.18-μm CMOS 製程技術所設計的雙向放大器。

A. 24-GHz 雙向放大器

此雙向放大器的設計是採用兩級共源(common-source)放大器的架構，採用的製程為 0.18-μm CMOS。為了縮小面積，我們省去了切換器，而是利用打開與關閉放大器中電晶體的方式來達到切換所需要的路徑。圖五為完整電路圖，此雙向放大器由兩組兩級單端(two-stage, single-ended)放大器所組成，接收放大器之輸入匹配網路與發射放大器之輸出匹配網路為共用，且接收放大器之輸出匹配網路與發射放大器之輸入匹配網路亦為為共用，如此共用匹配網路可以減小所需晶片面積。為了能進一步簡化電路架構，在做切換時 M4 元件 V_{ds} 不關，而只將 V_{gs} 關掉($V_{gs} = 0$)，讓 V_1 的電壓同時提供 M_1 和 M_4 的閘級和汲級電壓。同理，V_2 的電壓提供 M_2 和 M_3 的汲極和閘極電壓。因此可利用 $V_3 \sim V_6$ 來控制所走的路徑。其中，V_1 與 V_2 皆為 0.8 V，$V_3 \sim V_6$ 為 1 V，總消耗功率為 11.9 mW。圖六為此雙向放大器之晶片照片，晶片尺寸為 0.51 x 0.56 mm^2。此電路已製作並量測完成，圖七為量測之增益與輸入/輸出之回返損耗(Return loss)。在 24 GHz，增益為 8.7 dB，輸入與輸出之回返損耗分別為 4 dB 與 11 dB，雜訊指數為 4.5 dB。

B. 2 ~ 20 GHz 寬頻雙向放大器

此寬頻雙向放大器是採用切換器做為路徑之切換，而放大器部分則為接收與發射共用，如圖八所示。與圖四之設計比較，我們僅使用兩個單刀雙擲切換器，可再進一步縮小晶片面積。為了達到寬頻的特性，切換器與放大器皆需要採用寬頻之架構。單刀雙擲切換器的架構如圖九所示，為串聯並聯串聯之架構，利用電感做匹配以增加頻寬，並利用 body floating 技術，在並聯電晶體的 bulk

加上負偏壓以改善線性度[16]。放大器則是採用分佈式放大器(distributed amplifier)，如圖十所示。完整寬頻雙向放大器包含了兩個切換器與兩級分佈式放大器。圖十一為寬頻雙向放大器之增益與輸入/輸出回返損耗模擬結果，其增益在 2 ~ 20 GHz 為 13 ~ 14 dB，輸入/輸出回返損耗皆大於 9 dB。接收模式之雜訊指數模擬結果為 6.5 ~ 8 dB，而發射模式之 P_{1dB} 為 1 ~ 3 dBm。整個電路之功率消耗為 110 mW。圖十二為電路佈局圖，晶片面積為 0.9 mm^2。此晶片已經製作完成，目前正在進行量測中。

四、計畫成果自評

本計畫使用晶片系統設計中心所提供之台積電 0.18 微米 CMOS 製程技術，已成功設計出操作於 24 GHz 之雙向放大器，並完成量測。此外針對寬頻雙向放大器亦利用相同製程，設計一操作於 2 ~ 20 GHz 之雙向放大器。由表一之比較結果，我們利用矽基製成技術所開發之雙向放大器所需要的面積遠比目前文獻上所發表使用砷化鎵技術所製作之雙向放大器小。此項研究成果可針對系統需求作設計，再針對完整之雙向收發機系統做進一步研究與開發。

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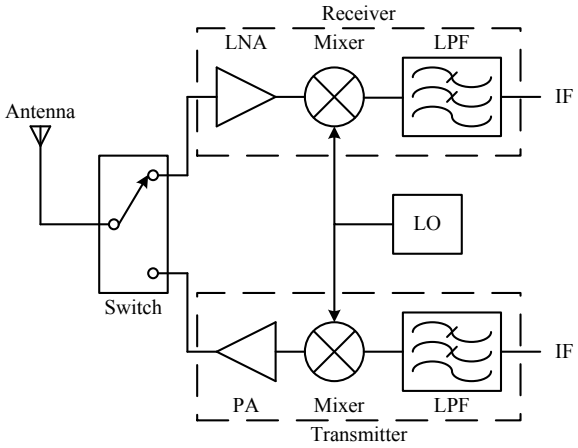
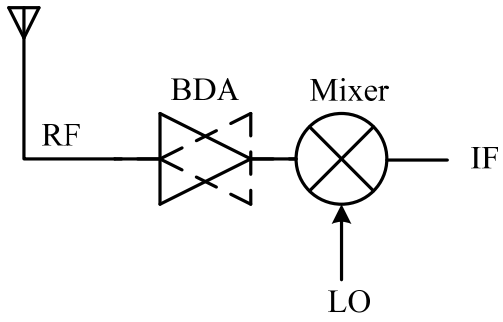
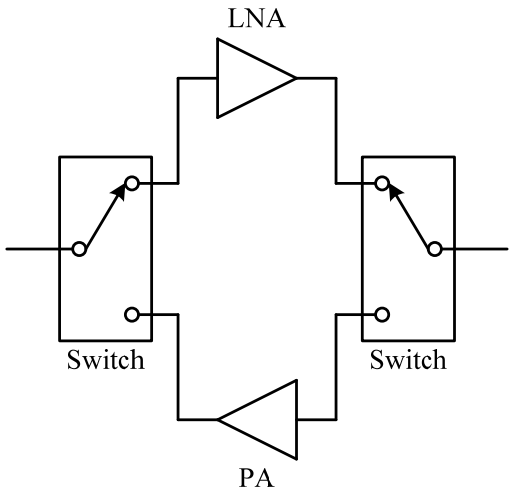


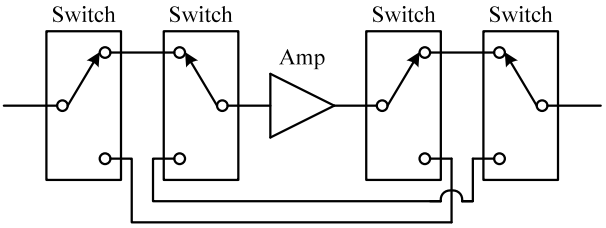
圖一、傳統收發器。



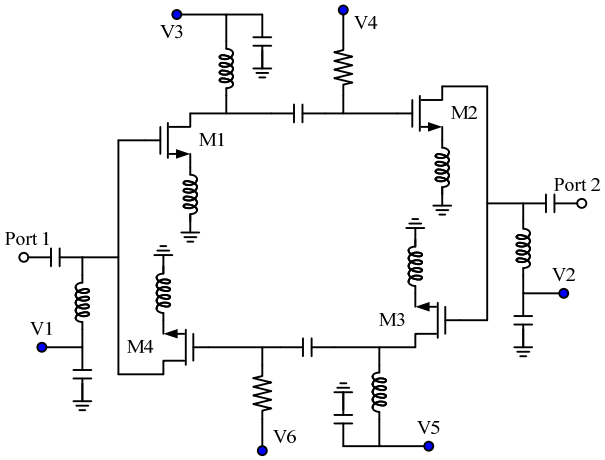
圖二、雙向收發器。



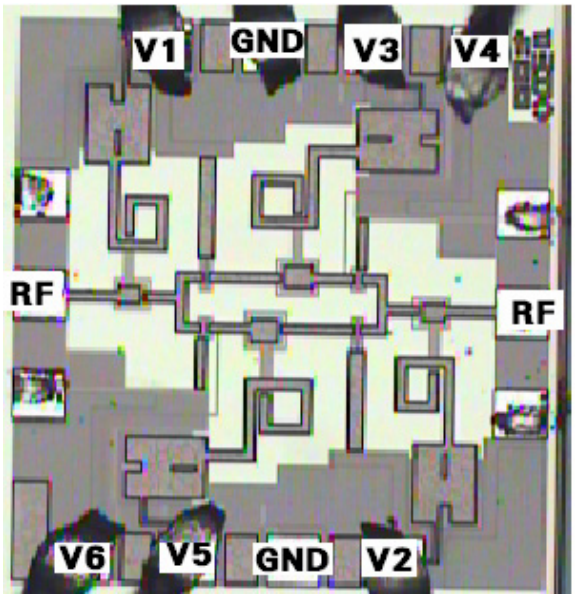
圖三、低雜訊放大器、功率放大器與切換器做整合設計之雙向放大器。



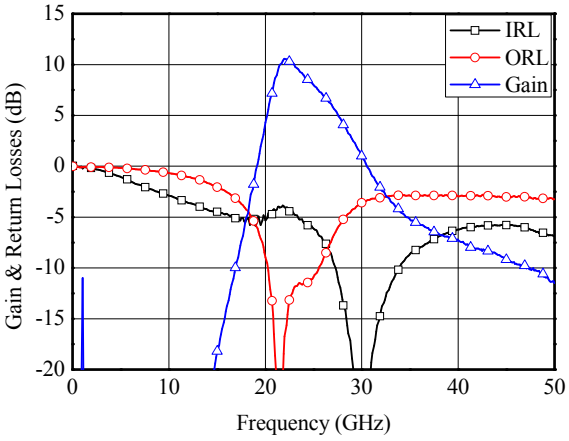
圖四、重複使用放大器元件之雙向放大器。



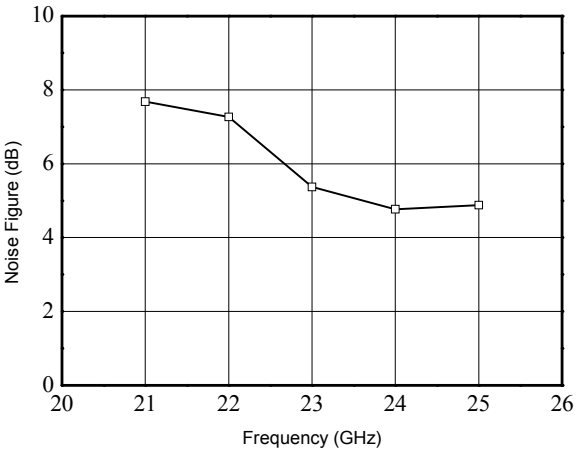
圖五、24-GHz 雙向放大器電路圖。



圖六、24-GHz 雙向放大器晶片照片。

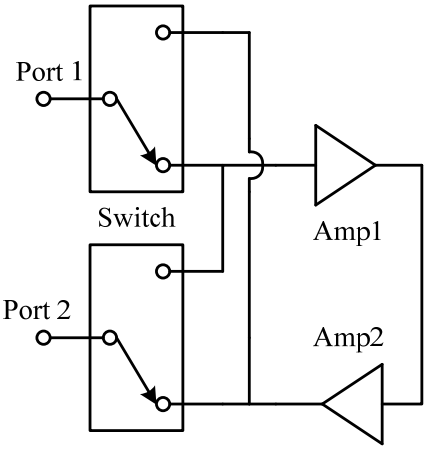


(a)

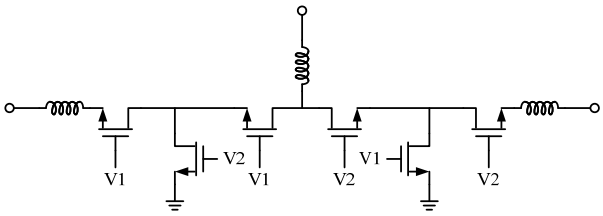


(b)

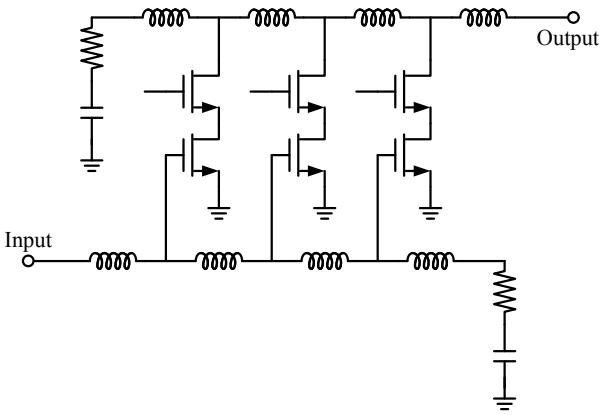
圖七、24-GHz 雙向放大器量測之(a) 增益與回返損耗，(b) 雜訊指數。



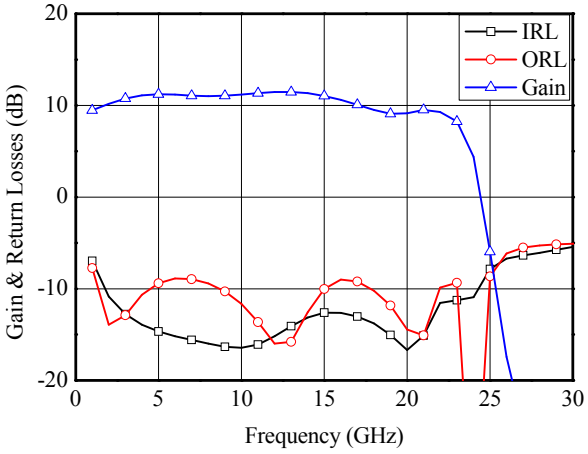
圖八、寬頻雙向放大器方塊圖。



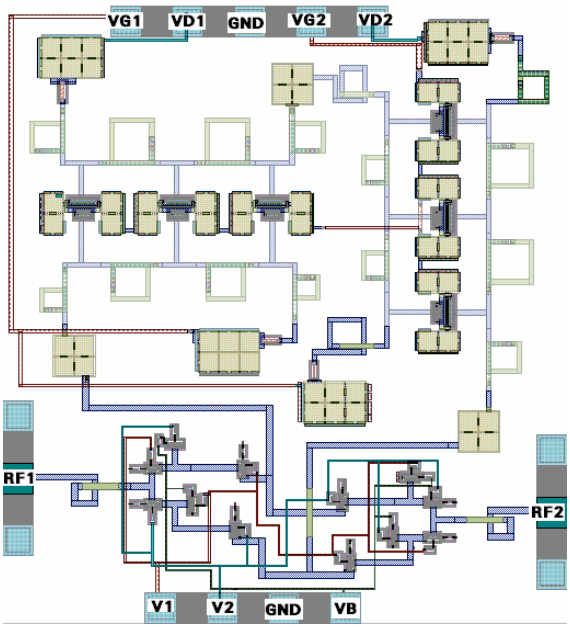
圖九、寬頻切換器電路圖。



圖十、寬頻分佈式放大器電路圖。



圖十一、2 ~ 20 GHz 寬頻雙向放大器之模擬增益與輸入輸出回返損耗。



圖十二、2～20 GHz 寬頻雙向放大器之電路佈局。

表一、雙向放大器特性比較表。

Ref.	Process	Topology	Frequency (GHz)	Gain (dB)	NF (dB)	Chip size (mm^2)
[6]	GaAs HEMT	Two stage CG	42	6	-	7.48
[8]	GaAs HEMT	Two stage CS	35	17	4	1.3
[8]	GaAs HEMT	Two stage CG	35	13	3.5	2.6
This work	0.18-μm CMOS	Two stage CS	24	8.7	4.5	0.29
This work (Sim.)	0.18-μm CMOS	Distributed amp. + switch	2～20	13	6.5～8	0.9

出席國際學術會議心得報告

計畫編號	NSC 95－2218－E－002－057
計畫名稱	單晶微波/毫米波雙向放大器之研製
出國人員姓名 服務機關及職稱	林坤佑, 台灣大學電信工程學研究所, 助理教授
會議時間地點	2007/6/3～2007/6/8, 美國夏威夷
會議名稱	國際微波會議
發表論文題目	1. A 35-50 GHz IQ-demodulator in 0.13-μm CMOS technology 2. A 10.8-GHz CMOS low-noise amplifier using parallel-resonant inductor

一、參加會議經過

2007 年國際微波週（International Microwave Week）於 6 月 3 日至 8 日在美國夏威夷舉行。國際微波週活動期間包括三個研討會：國際微波會議（International Microwave Symposium, IMS），射頻積體電路會議（Radio Frequency Integrated Circuit symposium, RFIC），以及自動化射頻量測會議（Automatic RF Testing Group Meeting）內容相當豐富。本人於此次會議中共有二篇論文發表，同時也出席了 RFIC 及 IMS 的各項議程，了解目前最新的研究成果。

此外會場中還有許多廠商的展出，包括高頻量測儀器設備、半導體代工製程、微波電路設計軟體、全波電磁分析模擬軟體及各種微波元件等廠商。

二、與會心得

國際微波會議是微波界最重要也是規模最大的研討會及展覽，會中除了有各國研究人員報告最新的研究成果外，各國微波元件、設備廠商也都參展，總數多達數百家廠商，參加會議及參展人數近萬人。也同時會見了許多在各領域的學者專家，分享研究成果及經驗。

三、建議

參與國際學術會議對於國內研究人員有相當大的助益，可以提昇自身的視野，了解目前國際上最新的技術發展現況，並提高我國在國際上學術界與工業界的能見度。應鼓勵國內研究人員積極參與大型國際學術會議。

四、攜回資料名稱及內容

大會所提供之論文集光碟片，內容包括 2007 International Microwave Symposium 的所有論文。此外也帶回一些參展廠商所提供之最新電路設計、電磁分析軟體與高頻量測元件與儀器的產品資訊。

A 35-50 GHz IQ-Demodulator in 0.13-μm CMOS Technology

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***Abstract* — A broadband millimeter-wave (MMW) IQ demodulator is presented in this paper using standard 1P8M 0.13-μm CMOS technology. This IQ demodulator consists of two Gilbert-cell mixers, one 90° broadside coupler, and one Wilkinson power divider. This IQ demodulator has a conversion loss better than 3 dB from 35 to 50 GHz. The magnitude imbalance and image-signal rejection ratio are smaller than 1 dB and greater than 25 dBc, respectively. The 16-QAM baseband signals with 1 MHz symbol rate are used to test the digital demodulation performance. The 16-QAM baseband signals can be demodulated with an EVM of 6.3%. The chip area of this IQ demodulator is 0.9 × 1 mm^2 including all testing pads.**

***Index Terms* — CMOS, demodulator, Gilbert cell, microwave monolithic integrated circuit (MMIC), mixer**

I. Introduction

Recently, complementary metal oxide semiconductor (CMOS) technology demonstrates the potential for wireless applications in millimeter-wave frequencies, such as gigabits point-to-point links, local area networks with extraordinary capacity in 60 GHz, and vehicular radar at nearby frequencies due to advantages of highly-integrated capability and potential low cost for mass production. CMOS integrated circuits have been reported in several millimeter-wave frequency bands, such as a 60-GHz low-noise amplifier [1], a 51-GHz VCO [2], a 60-GHz push-push VCO [3], and a 60-GHz receiver front-end [4]. All show that CMOS technology has high potential for MMW frequency applications.

IQ-demodulator is an important component in RF receiver with digital modulated baseband signals. It is usually placed between RF LNA and baseband circuits. It is advantageous to integrate a system on single chip in CMOS. In millimeter-wave frequency, only CMOS mixers have been reported, but lack of IQ demodulation function [5]-[8]. GaAs-based and SiGe HBT IQ demodulators in millimeter-wave frequency range are reported in 60-GHz receivers [9]-[11] with several GHz bandwidths.

This paper presents a 35-50 GHz IQ demodulator in standard bulk MS/RF 1P8M 0.13-μm CMOS process. This IQ demodulator has a conversion loss less than 3 dB from 35 to 50 GHz. The magnitude imbalance and image-signal rejection ratio are smaller than 1 dB and greater than 25 dBc, respectively. The 16-QAM baseband signals with 1 MHz symbol rate are used to test the digital demodulation performance. The 16-QAM baseband signals can be well demodulated with an EVM of 6.3%. The total dc power consumption is 178 mW. The chip area of this IQ demodulator is 0.9 × 1 mm^2 including all testing pads.

II. Circuit Design

The MMIC process is a standard bulk MS/RF 1P8M 0.13-μm CMOS process provided by Taiwan Semiconductor Manufacturing Company (TSMC). Eight copper metal layers are available for interconnection. The top metal is thickened to 3.3 μm to decrease the metal loss. A metal-insulator-metal (MIM) capacitor of 1 fF/μm^2 has been developed using oxide inter-metal dielectric. Poly resistors and spiral inductors are also available in this process. Additional deep N-well is used to isolate NMOS from lossy substrate. The 18-fingers NMOS device with finger width of 2 μm has a dc transconductance (G_m) of 23 mS biased at 0.7-V V_{DS} and 0.65-V V_{GS}. The device can achieve an f_{max} of 90 GHz and an f_T of 76 GHz.

The circuit schematic of this broadband IQ demodulator is shown in Fig. 1. It consists of two mixers, one 90° coupler, and one Wilkinson power divider. The circuit topology of the mixers is Gilbert-cell mixer [8]. The RF transistors are biased in saturation region to provide higher gain for RF input signal. The LO transistors are biased at near pinch-off region to act as switches. A current source is used under the differential pair to control the total bias current of this Gilbert-cell core and the charge injection technique is also employed in this circuit. Two resistors are chosen as the load of this circuit for very low IF frequencies. In order to match the input impedance of the next stage, two common drain buffer stages are added to achieve the impedance matching. Two Marchand baluns are used to convert the LO and RF signals from single-ended signals to differential signals.

Thin film microstrip lines are employed in this design, including the Wilkinson power divider. The bottom metal (metal 1) is used as the ground plane and the top metal (metal 8) is selected as the signal line of the thin film microstrip line. The port impedances for the three ports are all 50 Ω. The quarter-wave-length lines in the power divider are meandered to reduce the chip area.

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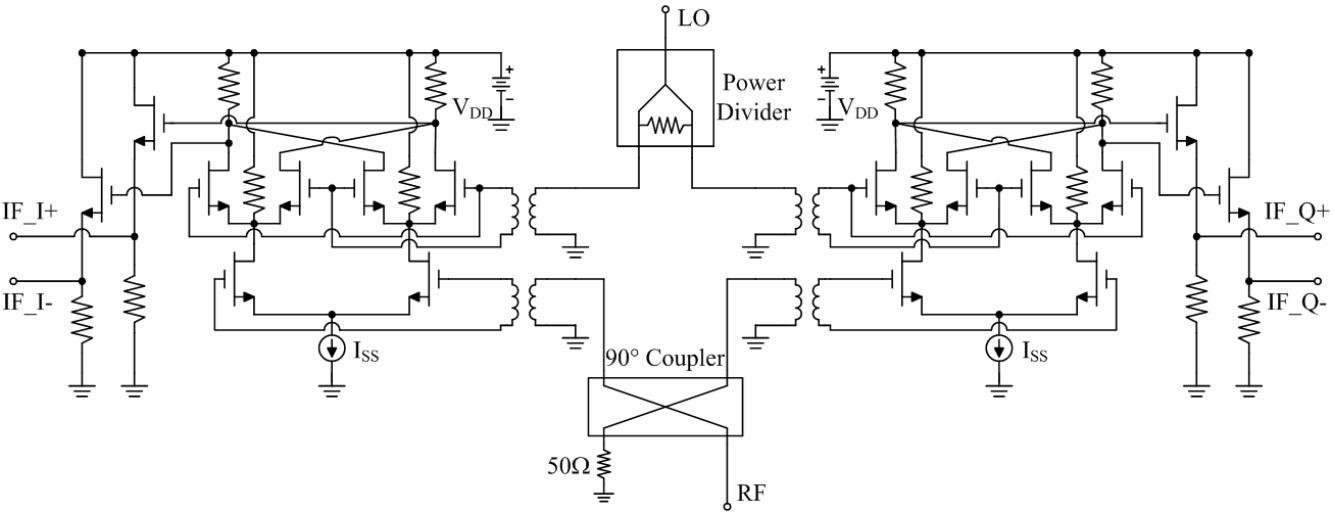

Fig. 1. Circuit schematic of this IQ demodulator, which consists of two Gilbert-cell mixers, one broadside coupler, and one Wilkinson power divider.

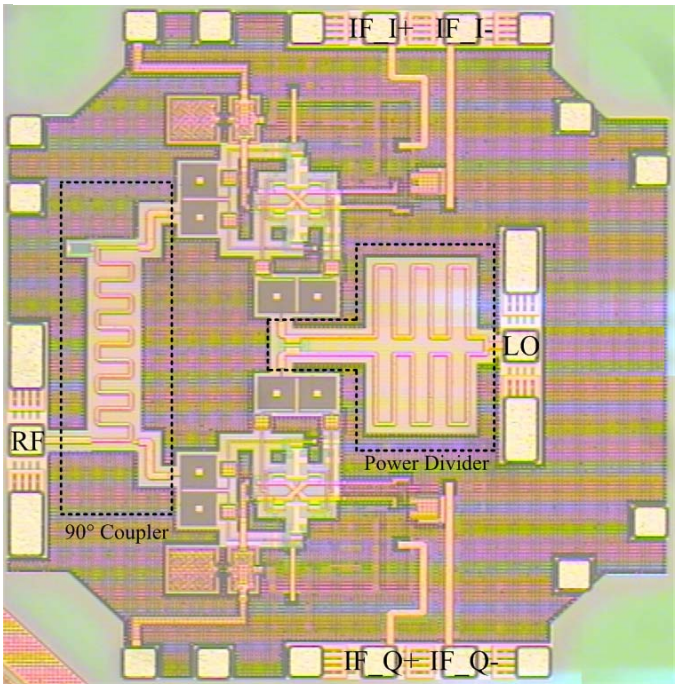

Fig. 2. Microphotograph of this IQ demodulator with a chip area of 0.9×1 mm^2.

The 90° coupler at RF port is implemented using broadside-coupled lines. The broadside-coupled lines are implemented using the top two metal layers (metal 8 and metal 7). This broadside-coupled coupler is also meandered to save the chip area.

Fig. 2 shows the microphotograph of this IQ demodulator with a chip area of 0.9×1 mm^2 including all testing pads. The RF and LO ports are on the left and right sides of this chip, respectively. The IF-ports of the I- and Q-channels are placed symmetrically on the top and bottom sides of the chip. To avoid the mismatch, all components and metal connections are placed as symmetrical as possible. The total dc power consumption is 178 mW with a dc supply voltage of 3.3 V.

III. Experimental Results

This circuit is measured via on-wafer probing for RF and LO ports through ground-signal-ground probes. IF ports are connected to PCB with bonding wires as output ports. Four dc blocking capacitors are used to block the dc current to the output ports.

To measure the conversion loss performance, the Agilent E8257D and Agilent 83650L signal generators are used for LO and RF sources, respectively. The measured conversion loss swept over LO power saturates at LO power of 8 dBm at RF frequency of 40 GHz with 10 MHz IF frequency. Therefore, 8-dBm LO power is used to drive this IQ demodulator over the entire RF-frequency range. Fig. 3 shows the single-ended conversion gain of the IQ demodulator. The single-ended conversion gains of I- and Q-channels are better than -3 dB from 35 to 50 GHz. The magnitude imbalance between I- and Q-channels is lower than 1 dB from 35 to 50 GHz. The high magnitude imbalance below 30 GHz is due to the insertion loss difference between the through and coupled ports of the broadside coupler, but it will not affect 35-50 GHz circuit performance. Fig. 4 shows the image signal rejection ratio of this IQ demodulator. The image-signal rejection ratio is better than 25 dBc from 35 to 50 GHz.

To measure the demodulation quality, an Agilent E8257D signal generator is used for LO source. The baseband signals are generated by using an Agilent E4438C vector signal

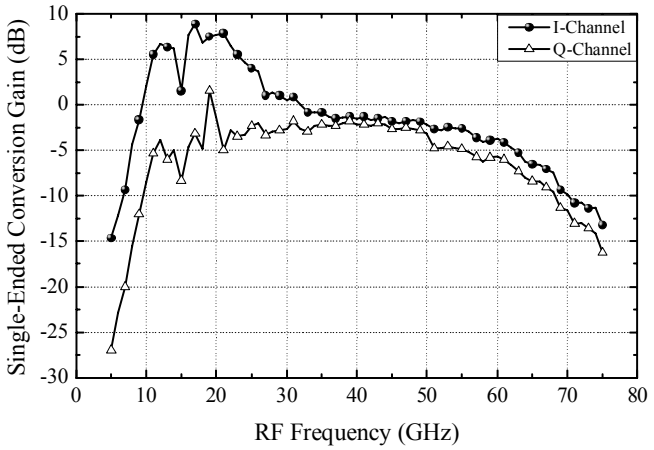

Fig. 3. Single-ended conversion gain for I- and Q-channels.

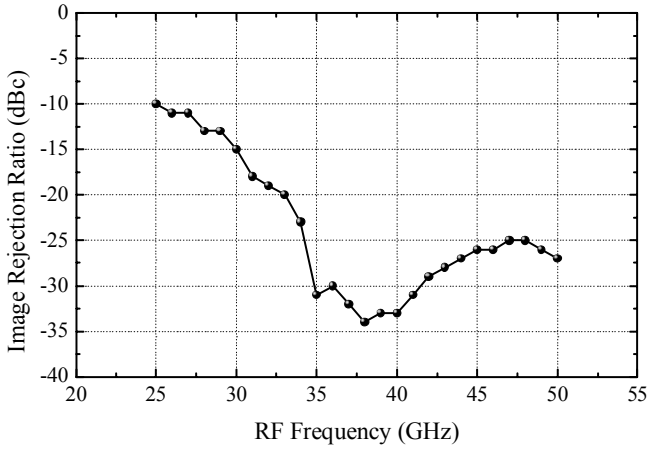

Fig. 4. Image signal rejection ratio of this IQ demodulator.

generator, which is coded with a pseudorandom bit stream. Then the baseband signals are connected to an Agilent E8247C signal generator to up-convert to millimeter-wave frequencies and feed into RF port. The output IF signals are connected to Agilent infiniium 54833D oscillation scope to calculate the demodulated results. The 16-QAM baseband signal is modulated with symbol rate of 1 MHz, and then up-converted to 46 GHz to feed into RF port. The constellation of the demodulated 16-QAM signals are shown in Fig. 5. The eye diagrams of the I- and Q-channels are shown in Fig. 6. The output spectrum of this IQ demodulator is shown in Fig. 7. The measured EVM of this circuit is 6.3%. Therefore, it is verified that this demodulator is suitable for broadband digital demodulation applications.

IV. Conclusions

A broadband IQ demodulator using 0.13-µm CMOS process has been demonstrated. This circuit has good amplitude balance and image signal rejection ratio over wide bandwidth. The measured results show that digital modulated signals can be demodulated well. From this demonstration, it is observed that the CMOS technology has high potentials for low cost MMW components.

Acknowledgement

The authors would like to thank Jeng-Han Tsai and Chi-Hsueh Wang for their helpful suggestions. This chip is fabricated by TSMC through Chip Implementation Center (CIC), Taiwan, R.O.C. This work was supported in part by the National Science Council of Taiwan, R.O.C. (NSC 95-2752-E-002-003-PAE, NSC 95-2219-E-002-006, and NSC 95-2219-E-002-009).

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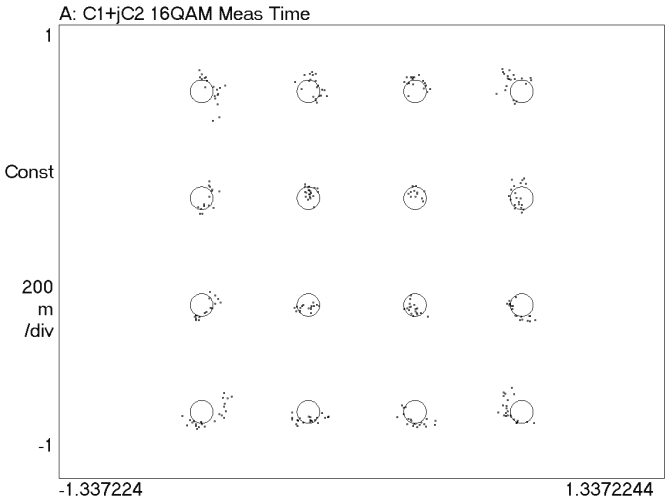
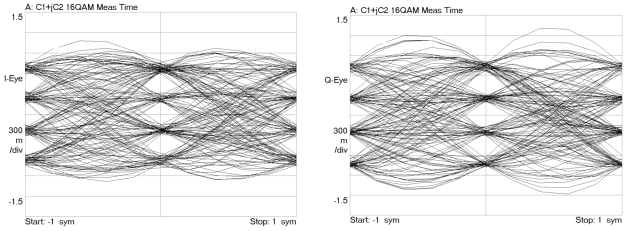


Fig. 5. The constellation of 16-QAM demodulated signals. The symbol rate is 1 MHz.



(a) (b)

Fig. 6. The eye diagram of the 16-QAM demodulated signals (a) I-channel (b) Q-channel.

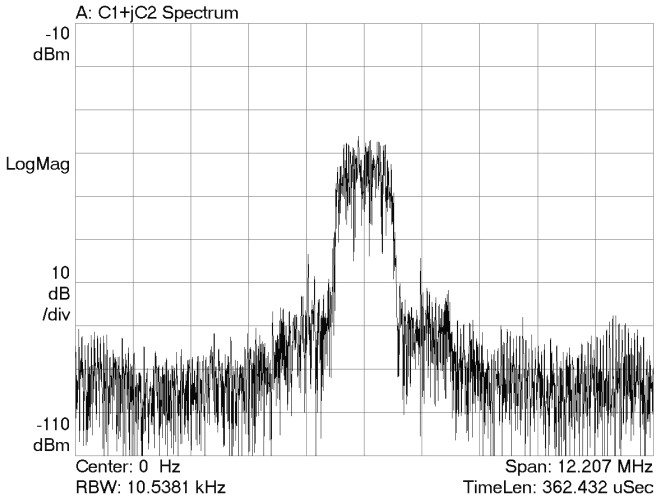


Fig. 7. The output spectrum of the 16-QAM demodulated signals.

A 10.8-GHz CMOS Low-Noise Amplifier Using Parallel-Resonant Inductor

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***Abstract* — A noise-reduction design method using parallel-resonant technique is demonstrated to improve the noise performance of a 10-GHz CMOS cascode low-noise amplifier, which is designed and implemented in a standard mixed-signal/RF bulk 0.18-µm CMOS technology. Measurements show a power gain of 10 dB with noise figure of 2.5 dB at 10.8 GHz, which is believed to be the lowest NF among the LNAs using bulk 0.18 µm CMOS at this frequency.**

***Index Terms* —CMOS, low-noise amplifier (LNA).**

I. Introduction

CMOS low-noise amplifiers (LNAs) have been extensively investigated for possible low-cost integration. Around 10 GHz, many implementations have demonstrated significant results, such as a folded-cascode variable gain LNA centered at 8-9 GHz with only 1-V power supply [1], a cascode LNA centered at 7 GHz by using dual-gate MOSFET and shielded pads in 0.25-µm CMOS process [2] and a cascode LNA centered at 13 GHz by using patterned-ground shield and helical inductors [3].

Since the low-noise characteristics of a cascode LNA will be compromised at higher frequencies, a parallel-resonant technique was proposed to mitigate the noise contribution from the cascode device, therefore improves the noise performance of a cascode amplifier at 5 GHz [4].

In this paper, the analysis of a noise-reduction design method using parallel-resonant technique based on [4] is demonstrated. This methodology is implemented to further improve the reported 10-GHz CMOS cascode LNA, which was designed with improved device-size selection method, and achieved a noise figure of 2.9 dB [5]. With the parallel-resonant technique, the noise figure has been reduced to 2.5 dB, which is believed to be the lowest one among the previously reported LNAs using bulk CMOS process at this frequency.

II. Noise Analysis

It can be shown that, based on a similar analysis as [4], the noise figure of a cascode amplifier in Fig. 1 is

$$F = F_1 + F_2\big|_{input\ referred}$$

$$= 1 + \frac{\overline{v_{n1}^2}}{4kTR_s} + \frac{\overline{i_{n1}^2}R_s^2}{4kTR_s} + 4R_s\gamma_2 g_{d02}\left(\frac{\omega_o}{\omega_{T1}}\right)^2\left(\frac{\omega_o^2 C_x^2}{g_{m2}^2}\right) \quad (1),$$

where R_s is the source resistance, γ_2 is a bias-dependent parameter for the second transistor M_2, g_{d02} is the zero-bias drain conductance of M_2, gm_2 is the transconductance of M_2, C_x is the parasitic capacitance presents at the node X between M_1 and M_2, and v_{n1} and i_{n1} are the input-referred noise voltage and current for the first stage, respectively. Equation (1) shows the parasitic capacitance (C_x) indeed has an important impact on the noise figure of a cascode amplifier. If channel length modulation in the input stage of the cascode amplifier (M_1) is neglected, the drain noise of the cascode device (M_2) contributes almost no noise especially at low frequencies. At high frequencies, however, the total capacitance, including parasitic capacitance C_x at node X between M_1 and M_2, as illustrated in Fig. 1, causes the drain noise of the cascode device (M_2) to contribute to the output noise, thus increase the noise figure.

To reduce this noise contribution from the cascode device (M2), a parallel-resonant inductor (Lp) placed at the node X between M1 and M2, can be used to resonate the Cx, as shown in Fig. 2.

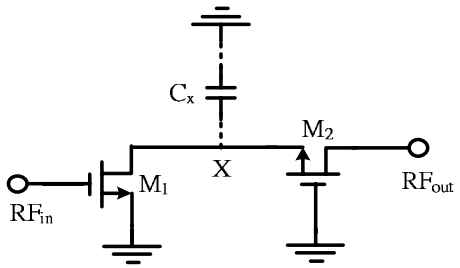

Fig. 1. Schematic for a cascode amplifier with parasitic capacitance (C_x) presents.

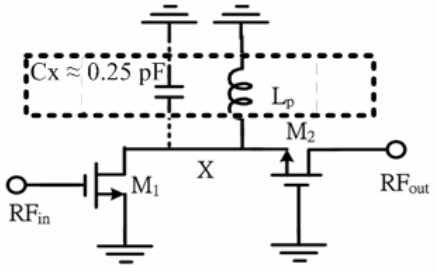

Fig. 2. Schematic for a cascode amplifier with parasitic capacitance (C_x) and associated L_p used to resonate it.

In this paper, the noise figure of a cascode amplifier using parallel-resonant technique is

$$F' = 1 + \frac{\overline{v_{n1}^2}}{4kTR_s} + \frac{\overline{i_{n1}^2}R_s^2}{4kTR_s}^2 + 4R_sC_x\omega_o Q_{L_p}\left(\frac{g_{m2}^2 + \omega_o^2 C_x^2}{(g_{m2} + \omega_o C_x Q_{L_p})^2}\right)\left(\frac{\omega_o}{\omega_{T1}}\right)^2 \quad (2),$$

where Q_{Lp} is the Q-factor of the on-chip parallel-resonant inductor (L_p) and $\omega_0 = 1/\sqrt{L_P C_X}$.

In (1) and (2) C_x is evaluated to be 0.246 pF and Q_{Lp} is estimated to be 10. Since the process, device size, biasing point and frequency of this LNA is equal to those of the LNA in [5]. The noise of the LNA using parallel-resonant technique is evaluated to be 1.54 dB by (2) which is 0.7 dB better than the 2.24 dB noise figure without parallel resonant technique evaluated by (1).

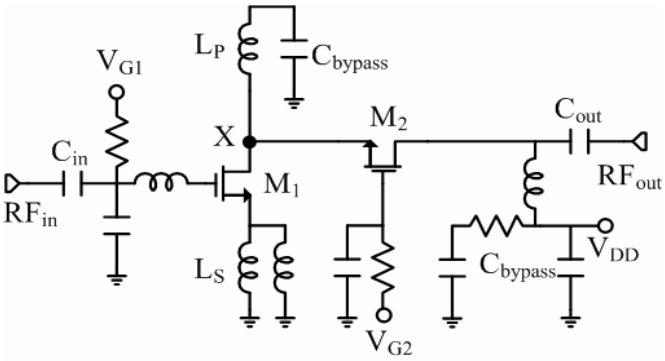

Fig. 3. Schematic of the 10-GHz CMOS LNA using the parallel-resonant technique.

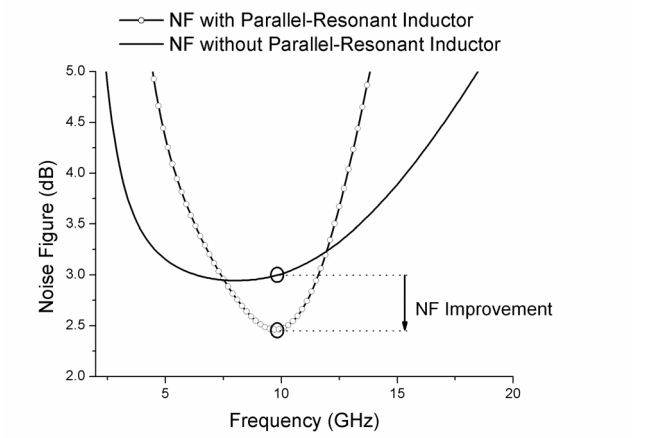

Fig. 4. Simulated noise improvement of the 10-GHz CMOS LNA using parallel-resonant technique.

III. Circuit Design

This 10.8-GHz LNA is implemented in a commercial standard 0.18-μm mixed-signal/RF CMOS technology which provides one poly layer for the gate of the MOS and six metal layers for inter-connection [5].

To demonstrate the parallel-resonant technique at higher than 5 GHz, the proposed 10.8-GHz LNA using parallel-resonant technique was designed and implemented. This methodology is implemented to further improve the reported 10-GHz CMOS cascode LNA, which was designed with improved device-size selection method, and achieved a noise figure of 2.9 dB [5] (the device widths were both 160 μm with 0.18-μm gate length). The inductor L_p at the node X between M_1 and M_2 is used to resonate out C_x. The output matching is accomplished with an LC impedance transformation network. C_{out} is 112 fF and was implemented with two 224-fF capacitors in series to desensitize the process variation. Parasitic capacitances of input and output RF pads are also included in the circuit simulation. Fig. 3 presents the complete schematic diagram of the 10.8-GHz CMOS LNA using the parallel-resonant technique. A 1.5-nH inductance L_p is used to achieve a noise figure improvement of 0.4 dB over the repeated 10 GHz LNA [5] as shown in Fig. 4.

The circuit simulation is performed in the software ADS [7], and the inductors and MIM capacitors are all simulated by the full-wave EM simulator, Sonnet [8]. Figure 5 presents the chip photo of the 10.8-GHz CMOS LNA, with a chip size of 0.65×0.71 mm^2.

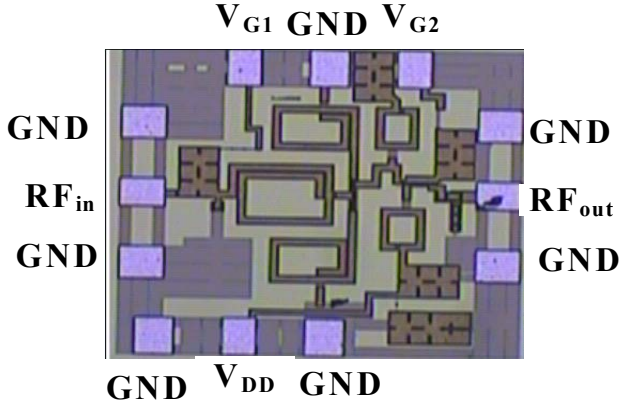

Fig. 5. Chip photo of the 10-GHz CMOS LNA using parallel-resonant technique with a chip size of 0.65×0.71 mm^2.

IV. Measurement Results

The LNA was measured via on-wafer probing. The measured and simulated gain and input/output return losses from 0.045 to 20 GHz are shown in Fig. 6. The measured LNA performs 10-dB peak gain at 11.4 GHz. The measured and simulated noise figures from 9 to 13 GHz are illustrated in Fig. 7, which shows a noise figure of 2.5 dB at 10.8 GHz. The measured 1-dB compression point (P_{1dB}) is +2.5 dBm and the measured two-tone input-referred third-order intercept point (IIP3) is +4.1 dBm. The total current consumption for this LNA is 11 mA from a 1.6-V power supply.

TABLE I
PREVIOUSLY REPORTED CMOS LNAS OPERATED AROUND 10 GHZ

References	Process	Architecture	Frequency (GHz)	Gain (dB)	Noise Figure (dB)	IIP3/P_{1dB} (dBm)	DC Power (mW)	Chip Size (mm^2)
[2]	CMOS (0.25μm)	Cascode	7	6.2	3.3	+8.4/NA	13.8	0.86×0.61
[1]	CMOS (0.18μm)	Folded Cascode	8	13.7	3.2	NA/-13.2	22.4	1×0.9
[1]	CMOS (0.18μm)	Folded Cascode	9	12.2	3.7	NA/-8.7	19.8	1×0.9
[3]	CMOS (0.18μm)	Cascode	13	4.9	4.67	+8.5/NA	9.7	0.31×0.33
[5]	CMOS (0.18μm)	Cascode	10	11.25	2.9	NA/NA	17.6	0.74×0.65
This Work	CMOS (0.18μm)	Cascode, parallel resonant technique	10.8	9dB (10 dB @ 11.4 GHz)	2.5	+4.1/+2.5	17.6	0.65×0.71

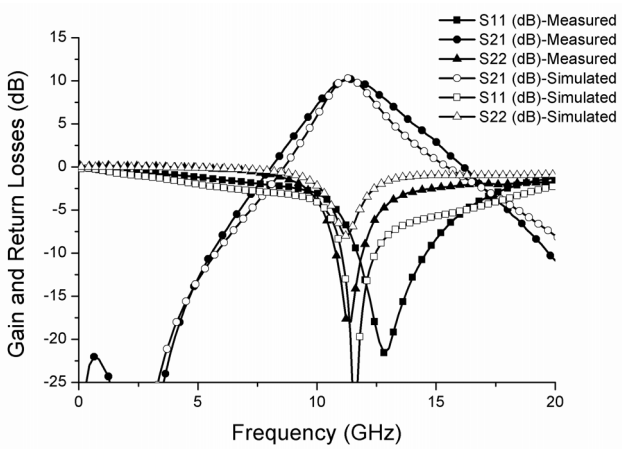

Fig. 6. Measured gain and input/output return losses of the 10-GHz CMOS LNA using parallel-resonant technique.

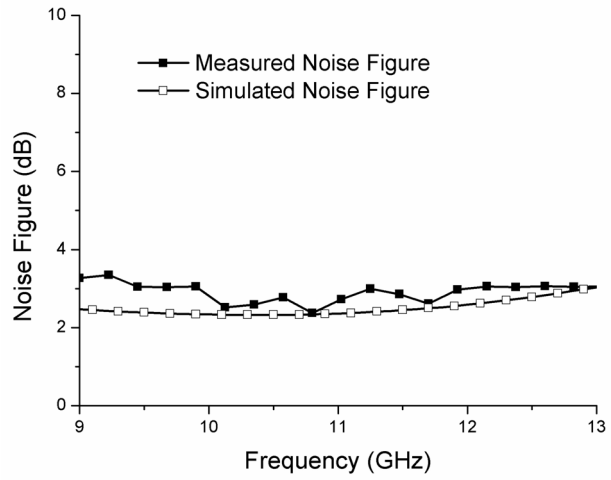

Fig. 7. Measured noise figure of the 10-GHz CMOS LNA using parallel-resonant technique.

Table I summarizes the performance comparisons among the related references. It reveals that our LNA has the lowest noise figure compared with the previously reported LNAs using bulk CMOS processes operating around 10 GHz.

V. CONCLUSION

A 10-GHz LNA using the parallel-resonant technique is successfully implemented in a standard 0.18-μm CMOS technology. This LNA shows a measured gain of 9 dB with a measured noise figure of 2.5 dB at 10.8 GHz and demonstrates lowest noise figure among the previously reported LNAs using bulk CMOS process around this operating frequency.

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