AAIC 2006 Homework 1

Due Fri. Mar. 17, 2006

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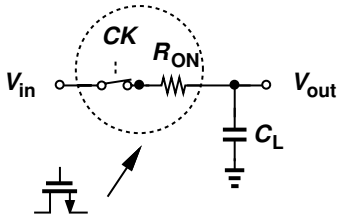
These problems are from "Design of Analog CMOS Integrated Circuits," by Razavi , McGraw-Hill, 2001

1. Problem 12.10

2. Problem 12.15

3. For the following sampling circuit, where R_{on}=1$k\Omega$, and C_H =2 pF. The circuit has been designed for a 12-bit system.

(a) Suppose $V_{out}(t = 0) = 0$ and V_{in} is a constant, 1 V. How long does it take for the output to



reach within 0.5 LSB of V_{in}?

(b) Now the switch is replaced by a MOS with R_{on} can be estimated as $1/\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_{th})$, where $\mu_n C_{ox} W/L$= $0.33mA/V^2$. Assume V_{CK}=3 V, V_{th} = $0.7V$ and v_{in}=1+sin(ωt). Write a C or MATLAB program to simulate total harmonic distortion (THD) for the input frequency from 5 MHz to 5 GHz. Note that body effect can be neglected in this problem.

(c) Now, let's neglect the RC phase shift problem in part (b). However, the finite fall time of clock (t_f) does degrade the performance. If ω= 100 MHz, obtain the signal-to-distortion ratio for t_f=100 ps, 300 ps, 1 ns and 2 ns. For this problem, you need to derive the "actual sampling signal" and then use MATLAB FFT to obtain the answer. Verify Eq.(2.13) in the textbook.