JAPANESE JOURNAL OF APPLIED PHYSICS
VOL. 29, NO. 7, JULY, 1990, pp. 1243-1247

Oxide Resistance Characterization in MOS Structures by the Voltage Decay Method

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(Received January 26, 1990; accepted for publication April 21, 1990)

The resistances of the gate oxides in MOS structures are determined based on the voltage decay method proposed in this work. This method provides nondestructive measurement of the oxide. The oxide resistance obtained by this method can be as high as 10^{14} ohms. Also, the unreliability of the data obtained by the conventional method, i.e., by dividing the applied voltage by the measured current, is compared. It is found that samples having the same initial C-V behavior can show significant differences in their oxide resistances. The one having a high oxide resistance can sustain a higher breakdown voltage than that having a low oxide resistance. A possible mechanism of the oxide resistance and the usability of the voltage decay method are also discussed.

KEYWORDS: MOS structure, gate oxide, resistance

§1. Introduction

There are several ways of characterizing the properties of gate oxides, *e.g.*, dielectric breakdown,[1,2] defect density,[1] stress measurement,[3] and hot-electron injection.[4] Some measurements cause degradation to the oxide properties either at the SiO_2/Si interface or in the bulk of SiO_2. For a practical metal oxide semiconductor (MOS) device which is still of use after testing, the harmful characterization techniques are of less interest. Therefore, a nondestructive characterization method of the oxide properties is worth noting.

Recently, we have found that the resistance-capacitance (RC) time constant for a general oxide is quite large.[5,6] Therefore, if an MOS device is charged to a certain value first, and the charging source is subsequently removed from the device, the charges on the metal gate will not be lost quickly. The slowly decreasing behavior of the residual charges left behind the gate can be detected in the voltage read by an electrometer in parallel with the MOS device. Since the voltage decay speed is mainly related to the leakage path through the oxide, the oxide resistance R_{ox} can then be analyzed from the voltage reading. Detailed analysis will be given in this paper. After obtaining the R_{ox} of an MOS device by the voltage decay method, it was found that the high- and low-frequency capacitance-voltage (*C-V*) curves before and after tests are almost the same. Therefore, this measurement does not introduce any damage to the oxide. An example of the application of the voltage decay method in examining the properties of oxides with indistinguishable *C-V* behavior is also given.

§2. Sample Preparation

P-type (100) silicon wafers with a resistivity of 7 Ω·cm were used as the substrates of MOS devices. After standard cleaning, the wafers were dry-oxidized at a temperature of 1000°C for several minutes. Oxides with thicknesses d_{ox} of 150, 250, and 400 Å were obtained in this study. Aluminum was then evaporated onto the oxide. Gate electrodes with diameters of 0.4 and 1 mm were formed by a standard etching process. In this experiment, the used samples with thicknesses of 150 and 250 Å have a gate diameter of 0.4 mm while the ones with a thickness of 400 Å have a gate diameter of 1 mm. Aluminum was also evaporated onto the back side of the wafer after the oxide was etched away. Finally, all the samples were postmetallization-annealed in N_2 at 400°C for about 10 mim.

§3. Breakdown Characterization

Breakdown voltage V_B is one of the important parameters in characterizing the oxide property. According to the existing literature, the V_B can be tested by applying a negative staircase voltage on the MOS device and measuring the leakage current as a function of applied bias until 1 $\mu A/cm^2$ is reached.[1] The negative polarity with respect to p-type substrates forces the device into

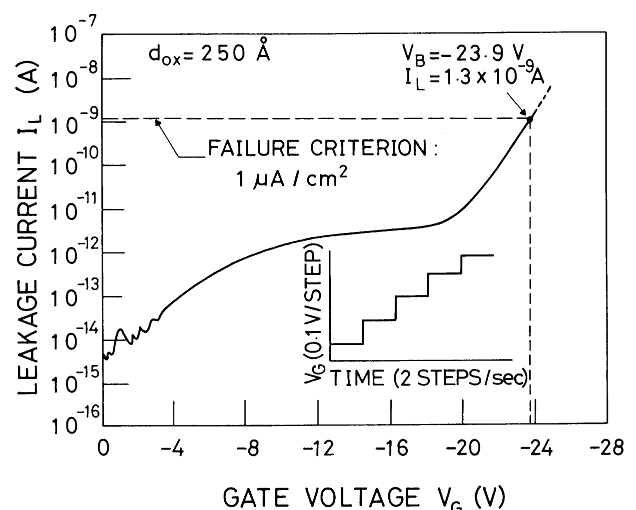

Fig. 1. Breakdown voltage and leakage current measurements of an MOS device with an oxide thickness d_{ox} of 250 Å. The failure criterion is defined as 1 $\mu A/cm^2$. The applied voltage is also shown in the insert of this figure.

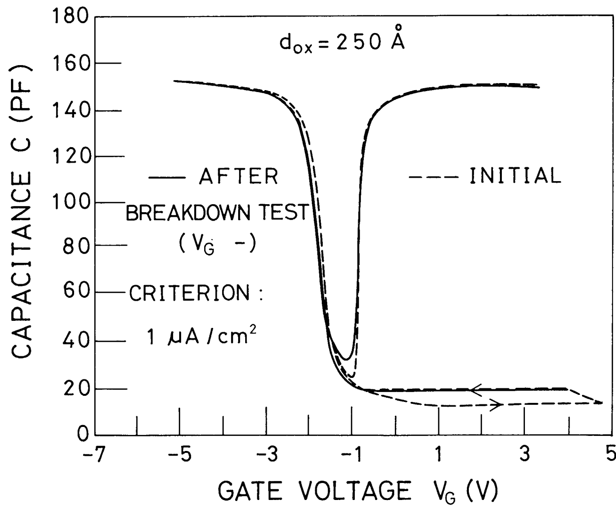

Fig. 2. High- and low-frequency *C-V* curves of the sample indicated in Fig. 1 before and after breakdown tests.

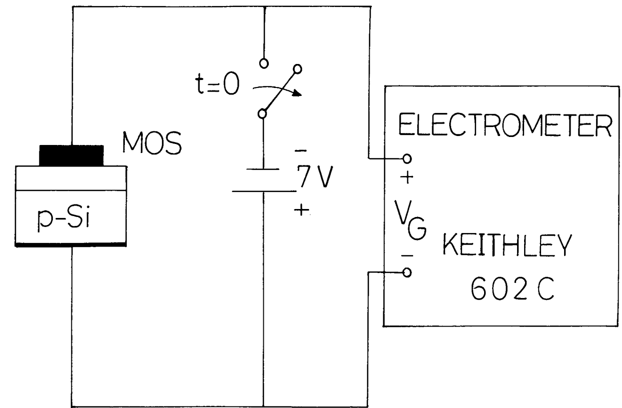

Fig. 3. Schematic diagram of the voltage decay measurement system.

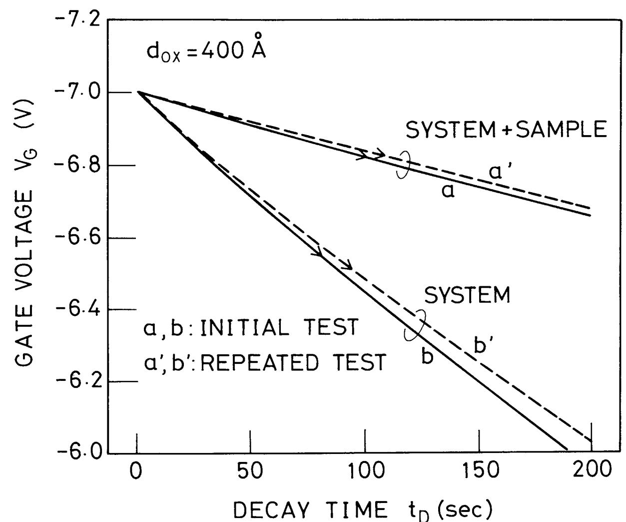

Fig. 4. Voltage decay behavior of an MOS device with an oxide thickness d_{ox} of 400 Å. The decays of the system with and without samples are both shown. Curves a and b are for the initial test and curves a′ and b′ are for the repeated tests.

accumulation, thus minimizing surface depletion and voltage loss in the silicon regions.[7] Note that the staircase voltage, *e.g.*, 2 steps/s and 0.1 V/step, is generated by an HP 4140B. Figure 1 shows the leakage current I_L versus gate voltage V_G for a sample with a d_{ox} of 250 Å. The applied staircase voltage is also shown in the insert of this figure for comparison. From this figure, one can obtain a V_B of 23.9 V under a failure criterion of 1 μA/cm^2.

Unfortunately, the V_B test causes some destructive damage to the oxide. This can be seen from the *C-V* curves before and after breakdown tests, as shown in Fig. 2. As can be seen from this figure, the breakdown test introduces the generation of interface states since the low-frequency *C-V* curve after the test is higher than that before the test. Also, some positive oxide charges were introduced during negative field stressing since the high-frequency *C-V* curve after the test shifts toward negative V_G. Therefore, the breakdown test of oxide is a destructive measurement.

§4. Voltage Decay Method

In order to describe the details of the voltage decay method proposed in this paper, a schematic diagram of the voltage decay measurement system is presented in Fig. 3. To start with, an electrometer is shunted with the test probes. With the MOS device placed on the test platform, the system, including the sample, is first charged with a certain voltage, *e.g.*, −7 V in this case. Then, the charging source is removed. This is indicated by an opened switch when $t=0$, as shown in Fig. 3. The voltage read by the electrometer decays slowly according to the RC time constant of the system with the sample. The measured V_G versus decay time t_D for the initial test of an MOS device with a d_{ox} of 400 Å is shown by curve a in Fig. 4. After this test, the MOS device is removed from the system. That is to say, the system is left floating without a sample. Then the same procedure as described above is performed again. Now the measured voltage decays according to the RC time constant of the system without a sample, and is shown by curve b in Fig. 4. Clearly, the RC time constant for the system without a sample is smaller than that for the system with a sample. This is mainly due to the significant increase of capacitance when the sample is added in parallel, although the total resistance is suitably reduced.

The measurement of a high resistance, such as the oxide resistance described in this paper, is very sensitive to some uncontrollable parameters. For example, a different position of the wafer on the test platform will cause a slight change in the RC time constant found. In order to show the reproducibility of the voltage decay method, the results of a repeated test are also compared following the same procedures as described above. The second set of measured voltage decay behaviors for the system with and without a sample are shown by curves a′ and b′, respectively, in Fig. 4. It is observed that curve a′ (b′) deviates slightly from curve a (b). Therefore, there are some limitations in the resolution of R_{ox} obtained by this voltage decay method. However, it is not important when samples with significant differences of R_{ox} are com-

pared. An example will be given in a later section.

Before determining the R_{ox}, the system capacitance C_s and the oxide capacitance C_{ox} are found to be 130 pF and 600 pF, respectively, by HP 4140B within the voltage decay range, i.e., from -7 to -6 V in this case. Note that C_{ox} is nearly constant within this voltage decay range since the MOS device is biased in the accumulation region. The C_s is also constant in this case. When the sample is absent, the system resistance R_s can be found from the simple RC decay equation expressed by

$$V_G(t_D) = -7 \cdot \exp\left(-\frac{t_D}{R_s C_s}\right). \quad (1)$$

The R_s's found from eq. (1) according to curves b and b′ in Fig. 4 are shown by the solid curve (initial test) and the dotted curve (repeated test) in Fig. 5(a), respectively. They are almost of the same value, i.e., about 1×10^{14} Ω, through the whole decay range.

When the sample is shunted, the RC time constant is changed. The total resistance R can be expressed by

$$\frac{1}{R} = \frac{1}{R_{ox}} + \frac{1}{R_s}, \quad (2)$$

and the total capacitance C can be expressed by

$$C = C_{ox} + C_s. \quad (3)$$

Similarly, under the simple assumption that R_{ox} is nearly constant, the simple RC decay equation is also valid. Note that the R_s and C_s in eq. (1) are changed to R and C, respectively, in this case. According to the voltage decay behavior as shown by curves a and a′ in Fig. 4, the obtained R_{ox}'s for the initial and the repeated tests are about 1.2×10^{14} and 1.4×10^{14} Ω, respectively. They are shown by the solid and the dotted curves in Fig. 5(b), respectively. Note that the deviation between them is small, i.e., 0.2×10^{14} Ω, and can be regarded as the resolution of the R_{ox} determined by the voltage decay method. Since the voltage decay rate of the system with the sample is lower than that without the sample, as observed in Fig. 4, the range of V_G in examining the R_{ox}, i.e., from -7 to -6.6 V, is smaller than that in examining the R_s, i.e., from -7 to -6 V, as shown in Fig. 5. Nevertheless, the determined R_{ox}'s, as shown in Fig. 5(b), are almost constantly distributed within the decayed V_G range. This is consistent with the simple assumption made earier.

§5. Discussion and Example

The R_{ox} determined in this investigation can be regarded as a measurement of the seriousness of the existing leakage path. The micropores grown during oxidation are responsible for the leakage path through SiO_2,[1] and may differ from sample to sample due to different oxidation processes or nonuniformities. In the voltage decay measurement, the flow of the leakage current through the micropore-related leakage path does not introduce further damage to the oxide properties. Figure 6(a) shows the voltage decay behavior of an MOS device

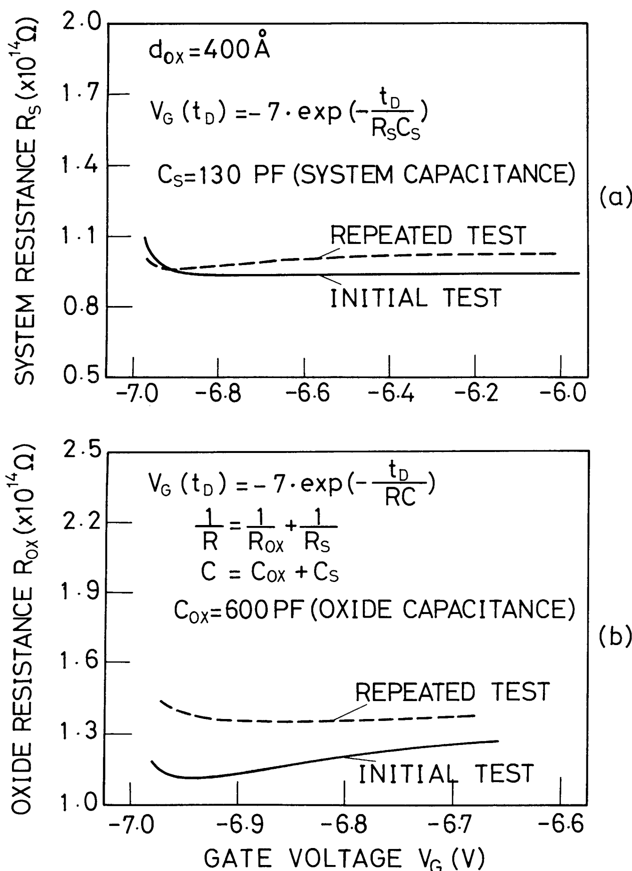

Fig. 5. (a) System resistance R_s and (b) oxide resistance R_{ox} versus gate voltage V_G for the sample shown in Fig. 4.

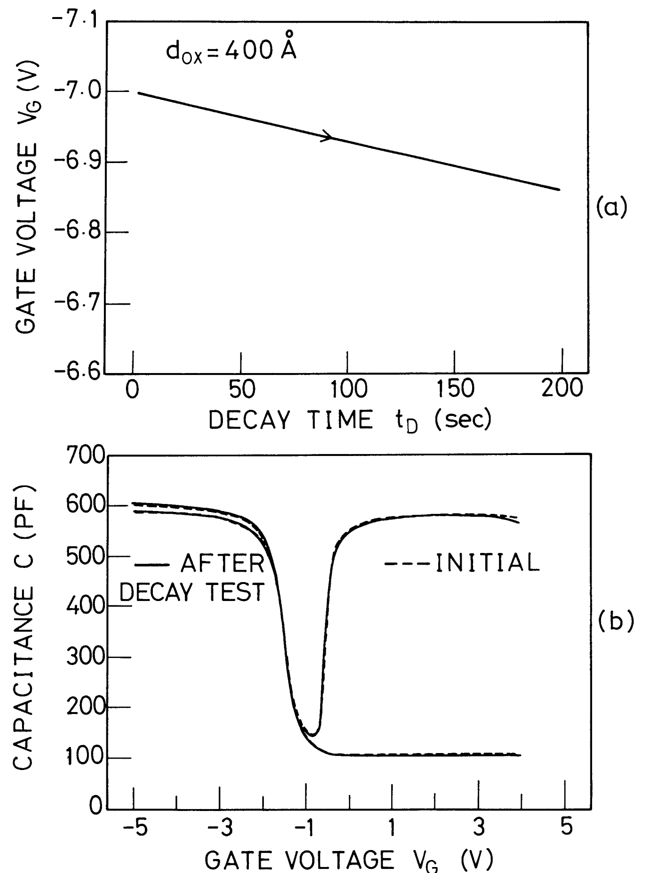

Fig. 6. (a) Voltage decay behavior of an MOS device with an oxide thickness d_{ox} of 400 Å. (b) High- and low-frequency C-V curves of this sample before and after decay tests.

with a d_{ox} of 400 Å. The high- and low-frequency *C-V* curves before and after decay tests are shown in Fig. 6(b). They are coincident with each other. Hence, the oxide properties after testing are as good as those before testing.

If the R_{ox} is obtained by dividing the applied voltage by the measured current instead of using the voltage decay method, unreliable fluctuation of data occurs due to unstable measurement errors. Figure 7(a) shows the measured current I versus V_G for an MOS device with a d_{ox} of 250 Å by HP 4140B. The solid circles are obtained under a holding time of 60 s, while the open circles are 20 s. The holding time is defined as the period of the applied V_G when the current is measured. Clearly, both the solid and the open data are unreliable. Figure 7(b) shows the R_{ox}'s calculated by V_G/I according to the data shown in Fig. 7(a). The data obtained by the voltage decay method are also shown for comparison. It is obvious that the fluctuation of R_{ox} obtained by the voltage decay method is much smaller than that by the division method.

It is noted that since the samples used in this study do not receive any passivation after sample preparations, the measured R_{ox} should account for both the surface and the bulk oxide leakage currents. Therefore, the oxide resistances determined in this investigation, i.e., about 1×10^{14} Ω, are smaller than those of gate dielectrics used in industrial erasable programmable read-only memories (EPROM's), i.e., about 1×10^{16} Ω. The passivation process is not examined for this investigation. But, it is worth investigating in this study. However, no matter how the surface leakage current may be reduced, the voltage decay method is still of use in evaluating the total oxide resistance.

Finally, an example is given to show the use of the voltage decay method. Five MOS devices, i.e., samples A, B, C, D, and E, with a d_{ox} of 150 Å are compared. They are fabricated by the same procedure and their initial *C-V* curves are all the same. Their R_{ox}'s before breakdown tests are obtained by the voltage decay method proposed in this work. The voltage decay behaviors for these samples are shown in Fig. 8, and the R_{ox}'s are found to be 5.2×10^{14}, 7.3×10^{13}, 1.3×10^{13}, 6.6×10^{12}, and 8.3×10^{11} Ω, for samples A, B. C, D, and E, respectively. It is noted that R_{ox} varies from sample to sample. These variations result from the nonuniformities of oxide properties, *e.g.*, oxide thickness or defect distribution. Therefore, there is no special relationship between the R_{ox}'s of two randomly chosen samples, such as those shown in Figs. 7 and 8. However, from the R_{ox} data shown in Fig. 8, it is expected that the sample with the smallest value of R_{ox}, i.e., sample E, should have the worst appearance in breakdown behavior. To show this relationship, the breakdown tests as described above are also performed on these samples for comparison. The corresponding V_B's for samples A, B, C, D, and D are −11.7, −11.3, −11.2, −9.6, and −8.3 V, respectively. These V_B's show a consistent relationship with R_{ox} wherein a smaller R_{ox} appears with lower V_B. Similar relationships between the oxide resistance and breakdown behavior are reproducibly observed in samples with different oxide thicknesses. Therefore, one can determine how good the prepared oxide is by the voltage decay method without the destructive measurement of V_B.

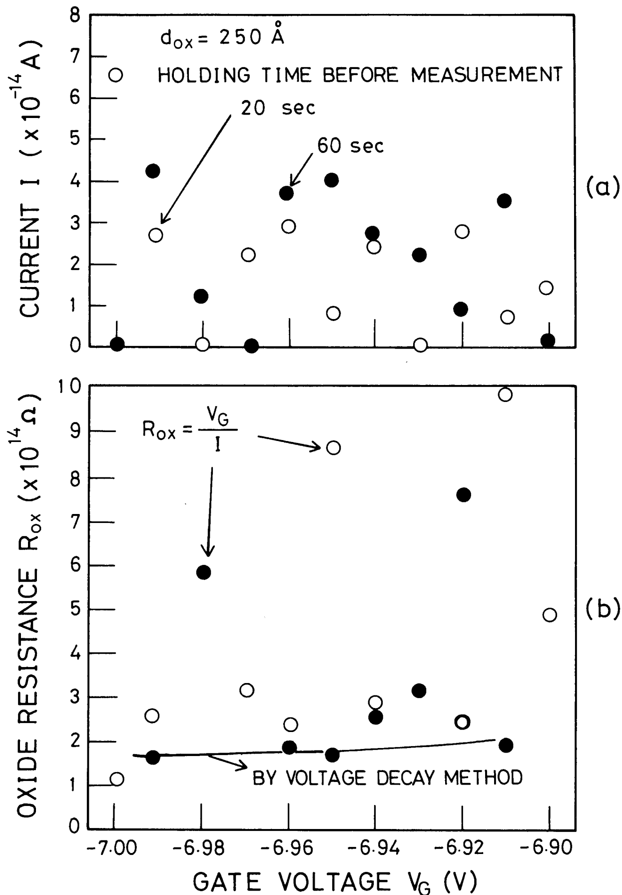

Fig. 7. (a) The measured current I and (b) the calculated oxide resistance R_{ox} versus gate voltage V_G of an MOS device with an oxide thickness d_{ox} of 250 Å. The data obtained by voltage decay method are also shown for comparison.

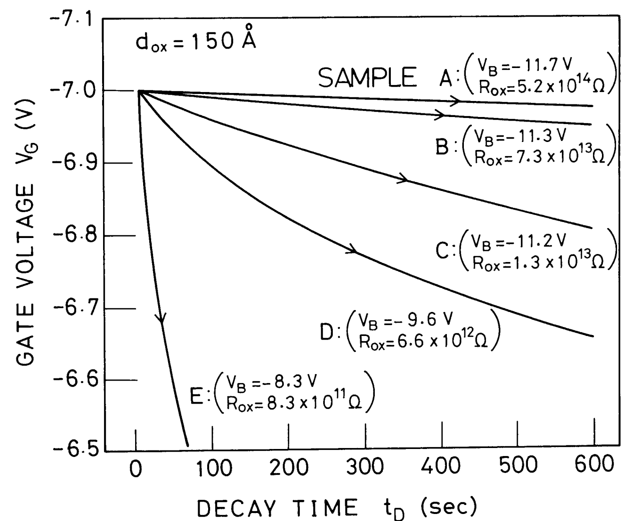

Fig. 8. Voltage decay behaviors of five MOS devices with different oxide resistances. The oxide thickness for all these samples is 150 Å. The breakdown voltages are also shown for comparison.

§6. Conclusions

The resistance of oxide in MOS structures has been found by the voltage decay method. The oxide after voltage decay measurement retains the same property as that before measurement. From the oxide resistance, one can determine how good the oxide properties are. The advantage of the voltage decay method due to nondestructive measurement is useful in some device characterizations.

Acknowledgement

The authors would like to thank the National Science Council of the Republic of China for supporting this work under Contract No. NSC78-0404-E002-51.

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