DESIGN OF AN OFDM RECEIVER FOR HIGH-SPEED WIRELESS LAN

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ABSTRACT

In this paper, we propose a baseband OFDM receiver for high-speed wireless local area network defined in IEEE 802.11a physical layer. Algorithms for channel estimation/equalization, timing recovery, carrier frequency acquisition/tracking, and sampling clock tracking are individually designed and later integrated into a receiver architecture. Simulation results show that the proposed OFDM receiver architecture is capable of high-rate data transmission in indoor multi-path fading channels.

1. INTRODUCTION

With a rapidly growing demand for wireless communication, there have been many research efforts on providing efficient and reliable high-data-rate wireless services. IEEE 802.11 standard for wireless LAN is first established in 1997, and it supports data rates of 1 Mbps and 2 Mbps in indoor wireless environments. Comparing with a wired network, such as 100-Mbps Ethernet, 2-Mbps data rate is relatively slow and is not sufficient for most multimedia applications. Recently, the IEEE 802.11 WLAN standard group finalized the IEEE Standard 802.11a, which is an orthogonal frequency division multiplexing (OFDM) physical layer for indoor wireless data communications [1]. The data rates of IEEE 802.11a range from 6 up to 54 Mbps and therefore this new standard is capable of providing almost all multimedia communication services in indoor wireless environments.

The paper first introduces the basic idea of OFDM and some important parameters defined in the IEEE 802.11a standard. Next, demodulation algorithms designed for IEEE 802.11a packet format and the entire receiver architecture will be described. All the impairments in typical indoor wireless channels are properly dealt with to minimize the degradation they may bring to system performance. A system made up of a standard-compatible transmitter model, an indoor channel model, and the proposed receiver model is designed and simulated. Whole system performance is evaluated by packet error rate (PER), as specified in the standard.

2. OFDM OVERVIEW

Recently, OFDM has received a great deal of attention and has been adopted in many new-generation wideband data communication systems, such as digital audio broadcasting (DAB), digital video broadcasting (DVB), high-speed wireless LAN, and digital subscribe lines (DSL). The basic principle of OFDM is to split the transmission binary data into several parallel data streams and transmit each of them on a separate subchannel. By making all subchannels narrowband, each subchannel experiences almost flat fading, which makes equalization manageably simple. Besides, an OFDM symbol usually lasts longer than channel RMS delay spread, therefore inter-symbol interference (ISI) can be dealt with by inserting a guard interval between two consecutive OFDM symbols.

Figure 1 shows a discrete-time baseband model of an OFDM communication system, where the inverse DFT and the DFT are used in the transmitter and the receiver, respectively [2]. In real implementation, the DFT is always replaced by a properly-sized FFT to reduce computation complexity. A mathematical model of the discrete-time OFDM system without channel distortion can be written as

$$\hat{\mathbf{X}}_n = \mathrm{DFT}(\mathrm{IDFT}(\mathbf{X}_n)). \quad (1)$$

where $\mathbf{X}_n$ are the N transmitted complex signals that encode the bit stream in the nth symbol and $\hat{\mathbf{X}}_n$ are the N received complex signals. With perfect channel, $\hat{\mathbf{X}}_n$ can be mapped to the original bit stream. In reality, channel impairments make more signal processing necessary in both the transmitter and the receiver.

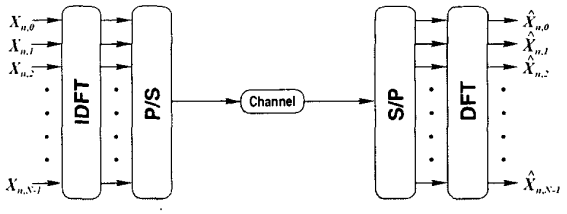

Figure 1: Simplified discrete-time OFDM system model.

Table 1 lists several key parameters in the IEEE 802.11a standard. Figure 2 shows the fundamental frame format of an IEEE 802.11a packet [1]. The guard interval duration is 800 ns, which is long enough to cover ISI in any indoor environment. In the beginning of each packet, there are short preamble and long preamble. The receiver exploits these predetermined sequences to conduct channel estimation and achieve proper initialization of several receiver blocks. Among the 52 used subchannels, there are 4 pilot subchannels used to assist timing/carrier tracking tasks during data symbols after the two preambles.

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Table 1: Parameters in the IEEE 802.11a standard.

Information data rate	6, 9, 12, 24, 36, 48, and 54 Mbps
Modulation	BPSK-OFDM QPSK-OFDM 16-QAM-OFDM 64-QAM-OFDM
Code rate	1/2, 2/3, 3/4
Number of subchannels	52
Number of pilot subchannels	4
OFDM symbol duration	4.0 μs
Guard interval	0.8 μs
Signal Bandwidth	16.6 MHz

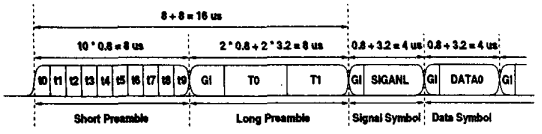

Figure 2: Structure of the IEEE 802.11a packet.

3. RECEIVER DESIGN

In an OFDM receiver, in addition to FFT for transforming signals from time domain to frequency domain, channel impairments caused by wireless multi-path fading channels must also be estimated and removed or compensated. In the following, several such signal processing techniques used in the proposed receiver will be described.

3.1. Packet Detection

Since a packet starts with the short preamble consisting of 10 identical symbols, a correlator is employed to detect the presence of a packet. This correlator correlates the received signal with itself delayed by 0.8 μs, the length of a short-preamble symbol. This correlation is formulated as

$$\gamma(i) = \sum_{l=0}^{L-1} \sum_{n=0}^{N-1} z_{i+n+lN} \; z^*_{i+n+(l+1)N}, \qquad (2)$$

where z_i are the received signal samples, N is the number of samples in 0.8 μs, and L is the number of symbols in the short preamble. Once the correlation value is above a pre-defined threshold for some duration, the receiver announces detection of a packet.

3.2. Coarse Carrier Frequency Acquisition

The carrier frequency offset estimation is again achieved during the short preamble and it is based on a maximum-likelihood estimation [3]. The estimated phase drift in a symbol is

$$\Delta\hat{k}(i) = \frac{1}{L} \sum_{l=0}^{L-1} \angle \left(\sum_{n=0}^{N-1} z_{i+n+lN} \; z^*_{i+n+(l+1)N} \right). \qquad (3)$$

3.3. Timing Recovery

The IEEE 802.11a short preamble has the characteristic of a PN sequence, so timing recovery can be achieved using a matched filter [4]. However, unlike a direct sequence spread spectrum (DSSS) signal, the optimum timing boundary is not where the matched filter output has its maximum. If the timing boundary is chosen at the position of the maximum peak as shown in Figure 3, an OFDM symbol will suffer from ISI introduced by the succeeding symbol. Therefore, for an OFDM symbol with a cyclic prefix, the optimal timing is the interval maximizing the SIR (signal to interference (ISI+ICI) ratio) that is given by [2]

$$\text{SIR} = \frac{S_u}{S_t - S_u}, \qquad (4)$$

where

$$\begin{aligned} S_u &= \int_{T_0}^{T_g} |h(t)|^2 dt, \\ S_t &= \int_{-\infty}^{\infty} |h(t)|^2 dt, \end{aligned} \qquad (5)$$

$h(t)$ is the channel impulse response; $T_0 + T_g$ is the chosen starting point of the signal interval for FFT; and T_g is the length of the guard interval. However, this method requires a sliding integrator with a maximum-finding circuit after the matched filter, thus a sub-optimal timing location algorithm is proposed. In this algorithm, the largest three peaks of the matched filter outputs are found and the earliest peak is identified. Then, T_0 is set to the point that precedes this earliest peak by a pre-defined number of samples. Simulation results show that the simplified method recovers the correct timing in most cases.

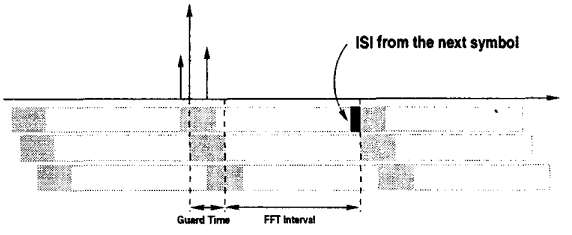

Figure 3: Illustration of ISI from the next symbol when the symbol boundary is set to the maximum peak. The three bars in the bottom illustrates three multi-path signals with different arrival times.

3.4. Channel Estimation

One of the advantages of OFDM is that it is not necessary to use a complicated equalizer to compensate fading caused by the channel. Instead of performing equalization in the time domain, an OFDM receiver usually compensates the channel response in the frequency domain, which requires less computation.

In an IEEE 802.11a packet, long preamble carries BPSK modulated signals on the 52 subchannels, which can be used for estimating the channel frequency response. Channel estimation and correction can be modeled as [5]

$$Y_{\text{Long},\,k} = H_k \cdot X_{\text{Long},\,k} + W_k, \qquad (6)$$

where $X_{\text{Long},\,k}$ is the known kth subchannel signal of the long preamble; $Y_{\text{Long},\,k}$ is the received kth subchannel signal during the long preamble. H_k is the channel frequency response on the

kth subchannel; and W_k is AWGN noise on the kth subchannel. Then, the channel frequency response estimation on subchannel k is given by

$$\hat{H}_k = \frac{Y_{\text{Long},\,k}}{X_{\text{Long},\,k}}. \tag{7}$$

In an indoor channel, since the channel impulse response is assumed stationary throughout a packet, channel estimation derived in the long preamble can be used to correct the following data symbols in the same packet, i.e.,

$$\hat{Y}_{n,k} = \frac{Y_{n,k}}{\hat{H}_k}, \tag{8}$$

where $Y_{n,k}$ and $\hat{Y}_{n,k}$ are the receiver signals before and after channel correction, respectively.

3.5. Tracking

After initial carrier/timing synchronization using preambles, there are still two tasks left: to track the remaining carrier frequency drift and sampling clock drift. Figure 4 shows the block diagram of tracking processing in the proposed receiver.

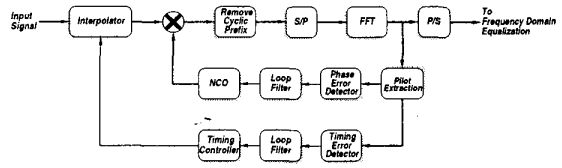

Figure 4: Block diagram of tracking processing.

3.5.1. *Carrier Frequency Tracking*

There are four pilot subchannels containing known signals. These pilots can provide information about the phase drift caused by the carrier frequency offset. Since the initial carrier frequency offset has already been acquired during the short preamble, inter-channel interference (ICI) can be neglected. Thus, complex-valued signals on a pilot subchannel rotate with an angular velocity equal to the remaining carrier frequency offset. The pilot subchannel signal phase difference between two consecutive symbols can be used to estimate the carrier frequency offset. The estimated phase error is given by

$$e_f(n) = \sum_k \angle\hat{X}_{n,\,k} - \angle\hat{X}_{n-1,\,k}, \tag{9}$$

where $k = -21,\ -7,\ 7,$ and 21. The phase error $e_f(n)$ is then fed to a phase-locked loop, which consists of four components: a phase-error detector, a loop filter, a numerically controlled oscillator (NCO), and a complex multiplier for phase de-rotation.

3.5.2. *Sampling Clock Tracking*

Both carrier frequency offset and sampling clock offset result in phase shift of subchannel signals. Although the phase shift caused by the sampling clock offset is tiny, its influence can not be neglected, especially for long packets, high-center-frequency subchannels, or high-order QAM modulation.

To recover sampling clock offset, interpolation based timing recovery is adopted in the proposed receiver and the timing error is estimated by [6]

$$e_t(n) = \sum_{k,\,l\ \ k\neq l} (\angle\hat{X}_{n,\,k} - \angle\hat{X}_{n,\,l}) - (\angle\hat{X}_{n-1,\,k} - \angle\hat{X}_{n-1,\,l}), \tag{10}$$

where $k,\ l = -21,\ -7,\ 7,$ and 21. With four pilot subchannels, there exists on the total six terms in the summation. The timing tracking is again performed by a phase-locked loop with a timing-error detector, a loop filter, a timing controller, and a digital interpolator.

3.5.3. *Tracking Consideration*

The frequency response of the indoor channel is not always flat. The tracking mechanism has to guarantee that the receiver can cope with drifts in carrier frequency and sampling clock. So the loop parameters in the two tracking phase-locked loops need to be tuned carefully. Moreover, it is likely that pilot subchannels are faded severely by the channel frequency response, especially in channels with long delay spread. In this case, robustness of the pilot subchannels becomes crucial. Fortunately, the channel estimation results derived during the long preamble can tell whether a pilot subchannel is robust or not. So, we use the magnitude of a pilot subchannel as a robustness indicator when phase/timing errors are calculated.

4. SIMULATION RESULTS

A system made up of an IEEE 802.11a transmitter model, an indoor channel model, and the receiver model is built. Whole system performance is evaluated by packet error rate (PER) under different noise levels and multi-path fading channels with two different delay spreads. Figure 5 shows the complete receiver block diagram and Figure 6 illustrates the simulation model. Note that both carrier frequency offset and sampling clock offset are set at 20 ppm of the RF frequency and the sampling clock frequency, respectively. The impulse response of the wireless indoor channel model is composed of complex samples whose phase is uniformly distributed and whose magnitude is Rayleigh distributed with exponentially-decaying means [2, 7].

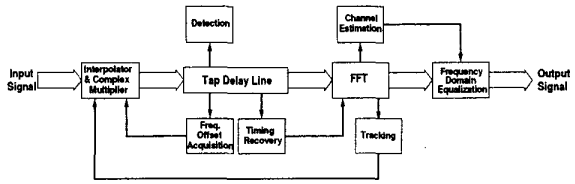

Figure 5: Block diagram of the proposed receiver.

Each transmitted packet consists of 1000 bytes, and the maximum allowable PER specified in the IEEE 802.11a standard is 10%. Figure 7 and 8 show the packet error rates versus E_b/N_0 using four data transmission rates and the delay spread of the channel is set to 100 and 150 ns, respectively. The convolutional code used in all cases has a code rate of $1/2$. Note that in a typical office environment, the channel delay spread is less than 100 ns. In this case, the proposed receiver can reliably communicate with a

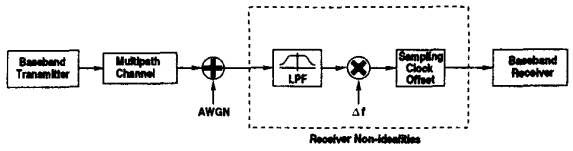

Figure 6: Model used in functional simulation.

bit rate up to 36 Mbps (64-QAM). In a larger indoor environment, such as factories, the receiver works best at a bit rate up to 12 Mbps (QPSK).

Note that for all modulations, the performance is sensitive to the channel delay spread. This is due to the following two reasons: First, larger delay spread entails more variations in the channel frequency response and more frequency bands with degradation beyond error correction. Secondly, ISI increases as the channel delay spread grows, and therefore, it is more likely that the guard interval can not cover the multi-path interference. In addition, for the higher-order QAM, more signal energy is needed to achieve the same PER as the channel delay spread increases. In other words, the higher-order QAM is more vulnerable to the increase in channel delay spread.

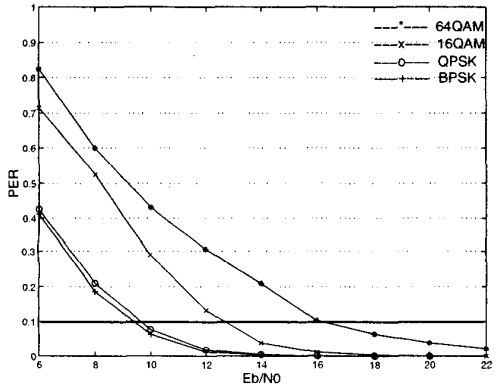

Figure 7: PER performance of the proposed receiver. The channel delay spread is 100 ns.

5. CIRCUIT DESIGN

Digital circuit for the proposed baseband receiver is currently being designed. At first, all processing must be converted to fixed-point arithmetic operations. To minimize the hardware complexity, minimum word length for all signals must be adopted. However, reducing the number of bits used to represent a signal adds quantization noise and degrades receiver performance. Therefore, a tradeoff must be made to ensure that the fixed-point-arithmetic receiver architecture causes acceptable PER degradation. With the architecture converted, we must then address the speed and power issues of the receiver circuit.

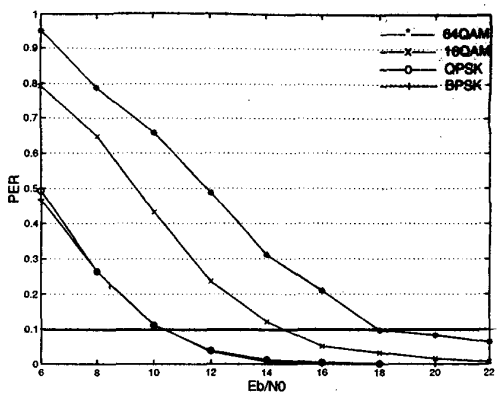

Figure 8: PER performance of the proposed receiver. The channel delay spread is 150 ns.

6. CONCLUSION

In this paper, an OFDM receiver architecture for high-speed wireless LAN is proposed. Many techniques, such as channel coding, channel estimation, interpolation, and carrier/timing recovery, are adopted to ensure functionality of the proposed receiver in various indoor environments. The system performance is verified and meet the PER specification in the IEEE 802.11a standard using reasonable signal power levels. Future ASIC implementation of IEEE 802.11a compatible WLAN baseband receivers can be based on the work proposed in this paper.

7. REFERENCES

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