Short-Channel Effects of SOI Partially-Depleted (PD) Dynamic-Threshold MOS (DTMOS) Devices

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Abstract

This paper presents short-channel effects of SOI partially-depleted (PD) dynamic-threshold MOS (DTMOS) devices using a compact model derived from a quasi-2D approach and MEDICI 2D simulation. Based on the analytical model, as verified by the 2D simulation results, the DTMOS device has less short channel effects including drain-induced-barrier-lowering (DIBL)-induced short channel effects.

Summary

For the SOI PD DTMOS device as shown in Fig.1, by dividing the thin-film into three regions---I) the left fully-depleted region near the source (0<y<l_1), (II) the top fully-depleted region near the surface (l_2<y<L), and (III) the right fully-depleted region near the drain (0<x<w_d) excluding the bottom neutral region, and using a quasi-2D approach, solving 2D Poisson's equation with the boundary conditions derived from V_G,V_D, and V_S, the surface electrostatic potential distribution has been obtained. From the surface electrostatic potential distribution, the threshold voltage of the SOI PD DTMOS device, which is defined as the gate voltage when the minimum surface electrostatic potential is equal to thin-film Fermi voltage, has been obtained.

In order to verify the validity of the compact short-channel effect model for the SOI PD DTMOS device, the analytical model results have been compared with the MEDICI 2D simulation results. Fig. 2 shows the threshold voltage vs channel length of the n-channel SOI PD DTMOS device with a gate oxide of 64A, a p-type thin-film doped with a density of 1.5~6x$10^{17}$$cm^{-3}$, a channel width of 1um, biased at V_{DS}=0.1V and V_{BS}=0V, 0.6V. As shown in the figure, with a more heavily doped thin-film, its short channel effects are less noticeable. Note that the V_{BS}=0 case can be regarded as the conventional device without the DTMOS structure (V_{GS}=0V). Compared to the case without the DTMOS structure (V_{BS}=0V), the DTMOS one has smaller short channel effects. As shown in the figure, the analytical model results predict well of the short channel effect behavior as verified by the 2D simulation results. Fig. 3 shows the threshold voltage vs channel length of the n-channel SOI PD DTMOS device with a gate oxide of 64A, a p-type thin-film doped with a density of 3x$10^{17}$$cm^{-3}$, and a channel width of 1um, biased at V_{DS}=0.1V and V_{BS}=0 ~ 0.6V. As shown in the figure, at a higher V_{BS} (V_{GS}), short channel effects are smaller. Compared to the case without the DTMOS structure (V_{BS}=0), the DTMOS one has smaller short channel effects. Fig. 4 shows the threshold voltage vs channel length of the n-channel SOI PD DTMOS device with a gate oxide of 64A, a p-type thin-film doped with a density of 3x$10^{17}$$cm^{-3}$, and a channel width of 1um, biased at V_{DS}=0.1V, 0.6V and V_{BS}=0V ~ 0.6V. As shown in the figure, at a larger V_{DS}, the short channel effects due to drain induced barrier lowering (DIBL) are more noticeable. Compared to the case without the DTMOS configuration (V_{BS}=0), the DTMOS device shows less DIBL-induced short channel effects.

References

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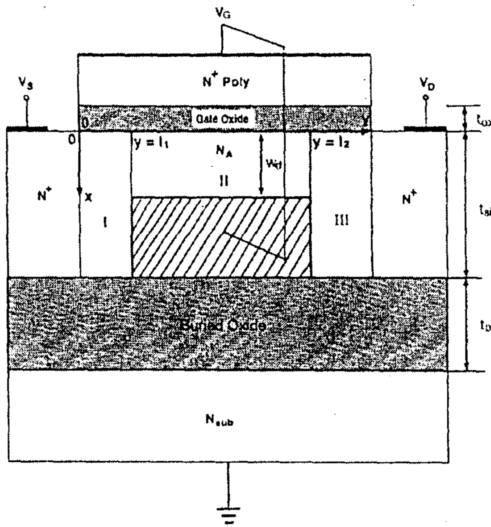

Fig. 1: Cross section of the SOI partially-depleted (PD) dynamic-threshold MOS (DTMOS) device under study.

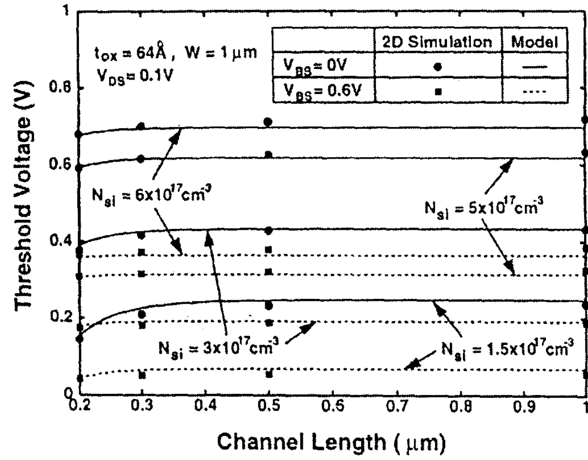

Fig. 2: Threshold voltage vs. channel length of the n-channel SOI PD DTMOS device with various p-type thin-film doping densities.

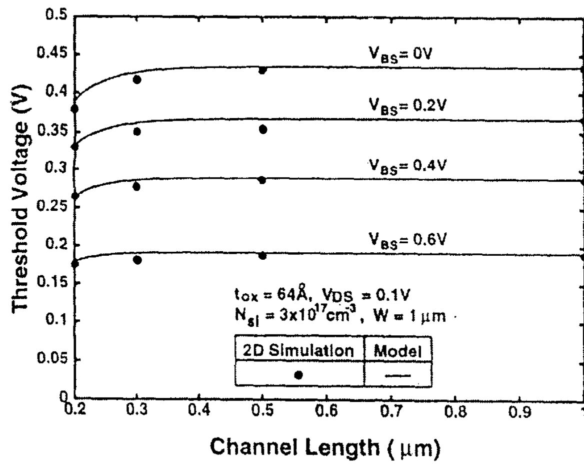

Fig. 3: Threshold voltage vs. channel length of the n-channel SOI PD DTMOS device biased at various body voltages.

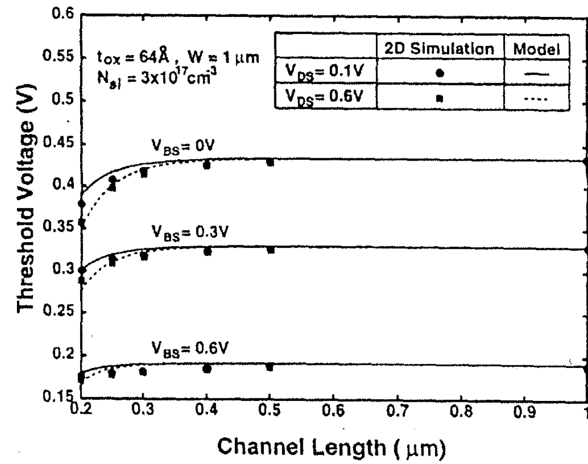

Fig. 4: Threshold voltage vs. channel length of the n-channel SOI PD DTMOS device biased at various drain voltages and body voltages.