Minimizing Coupling Jitter by Buffer Resizing for Coupled Clock Networks

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Abstract

Crosstalk noise is a crucial factor affecting chip performance in deep submicron technologies. Among all possible crosstalk noise sources, clock is the most common aggressor as well as victim. Crosstalk on clock nets can increase clock jitter, which may degrade significantly the system performance. It is therefore imperative to design clock buffers to reduce the coupling effects. In this paper, we address the crosstalk effect on clock networks. We propose an algorithm to size clock buffers for given buffered clock trees such that the induced clock jitter is minimized. Our experimental results show a significant reduction of clock jitter by sizing the clock buffers without increasing the total area of buffer.

1. Introduction

With the recent advances in VLSI technology, the device sizes have shrunk below 0.1um. The shrinking geometries have brought two new major concerns for signal integrity. One is the power and ground levels fluctuations caused by simultaneous switching circuits. The other problem is the increasing aspect ratio of wires and the decreasing of interconnect spacing which have made coupling capacitance larger than self-capacitance. The ratio of coupling capacitance is reported to be as high as 70%-80% of the total capacitance. For high speed circuits, it has become very important issue to avoid the impact of coupling effect.

Clock synthesis has been an important step in chip design for more than ten years. Synchronous designs have been the most popular as they are robust and easy to migrate. However, the chip performance of synchronous designs highly rely on the quality of clock tree. With the increasing coupling effect on clock trees, the clock jitter caused by coupling is becoming more and more significant. Therefore, it is now very important to design clock networks such that the coupling effect can be minimized [5][6].

Clocks distributed throughout the chip toggle in every cycle with the highest frequencies; therefore improper clock design could easily introduce too much crosstalk noise and cause chip failure. Coupling can be accumulated over large portions of a clock tree and hence may be very significant. Fig. 1 shows a typical clock signal propagating through a series of clock buffers. In each stage, crosstalk increases the timing uncertainty, or jitter. The clock jitter increases and accumulates throughout the tree. Thus at the last stages, it can be very significant. Experiments show that for a ten stage clock signal, the jitter can grow from 0 at the input to 290ps [1] at the leafs in worst case. For two coupled interconnects driven by different buffers, the coupling capacitance, the arrival time, size of aggressor and victim can determine the jitter caused by cross coupling (Fig. 2). Gate sizing is a commonly used technique to improve circuit performance [4]. Existing buffer insertion or gate sizing algorithms only try to eliminate the noise effect instead of delay change induced by crosstalk [2][8]. But for a coupled clock network, the clock buffers should be inserted and sized in a way such that both skew and jitter are both minimized.

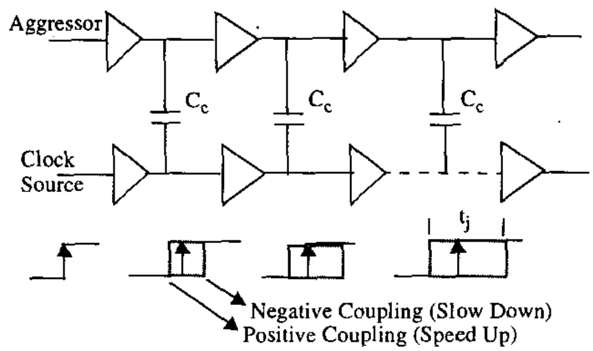

Fig. 1: Crosstalk effect on a multi-stage clock signal. The timing uncertainty is magnified at every stage. t_j is the clock timing uncertainty (jitter).

In this paper, we propose a buffer sizing algorithm to minimize clock jitter for a coupled clock network. The problem formulation is given in Section 2, followed by the modeling and algorithm in Section 3, 4. Section 5 gives the experimental results and Section 6 for the conclusion and summary.

2. Problem Formulation

Given two coupled transmission line as shown in Fig. 2, with C_c minimized, the transition of aggressor can change the delay of victim. It speed up the victim when it goes in the same direction of victim, and slow down the victim when it goes in the opposite direction. Analytical methods have been established to capture the effect [3][7]. The effect of jitter is determined by three major factors, the buffer size of aggressor, the buffer size of victim, and the coupling capacitance. Since we assume that C_c is already minimized in the routing

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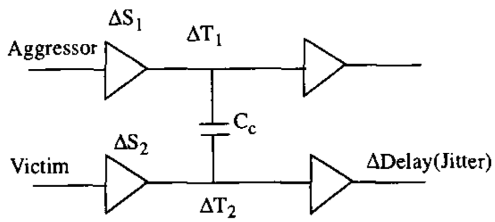

Fig. 2: A coupled transmissin line

phase, to minimize the jitter (ΔDelay) of victim, we can only size the buffer of the aggressor and victim.

Fig. 3 shows how the timing of aggressor and victim affect the delay change. One can observe that the jitter rises to peak when the aggressor's arrival time is close to the victim's. Therefore, by sizing the aggressor's and victim's buffer size, we can separate the timing window and hence minimize the jitter effect caused by coupling.

Given a set of buffered clock trees, T_1, T_2, ...,T_n the problem is to minimize the effect of jitter by sizing the clock buffers while in the mean time maintain the zero skew property.

*Problem 1:*Clock Buffer Sizing Problem

Given a set of buffered clock trees, T_1, T_2,..., T_n with buffer size S_{ij}, the problem is to find the size change ΔS_{ij} such that the clock jitter on all clock paths are minimized, and subject to the constraints that all the path delays from root to sinks are maintained.

The jitter in terms of size change is given in Section 3.

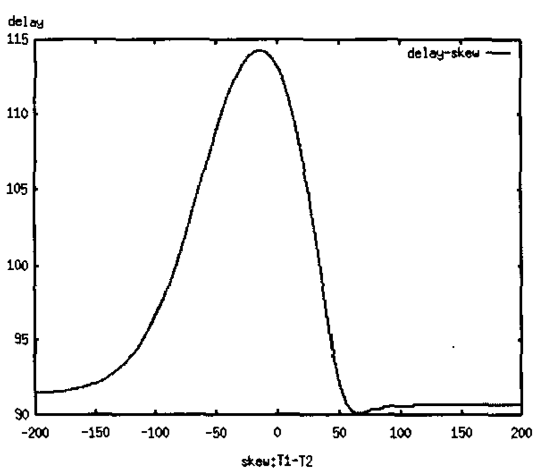

Fig. 3: The victim's delay v.s. skew (Skew = T_1-T_2), unit in ps.

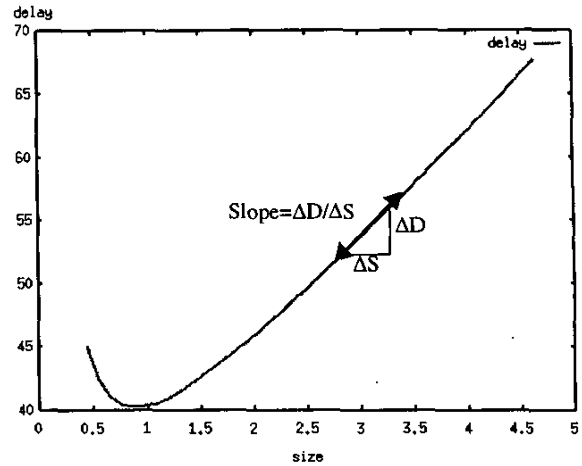

Fig. 4: Delay and size relation

3. Modeling

3.1 Timing Constraint

As described in problem 1, the constraint for the problem is to maintain the path delay from root to all sinks constant. Since the delay of a buffer can be changed by sizing the buffer, and the output loading is constant, the gate delay change ΔD can be represented as ΔD=F(ΔS). Fig. 4 is the typical relation of delay and buffer size for a given loading. If we limit the search range ΔS to a small range, the slope can be approximated as a linear function. That is, ΔD=a*ΔS, where a is the slope of the current size. Now all the gate delay change can be represented $\Delta D_i = a_i * \Delta S_i$.

For all the clock paths from root to sinks, the change of path delay can be expressed by the gate delay change ΔD_i on its path, $P_i = \sum_j \Delta D_{ij} = \sum a_{ij} \times \Delta S_{ij}$, to maintain the timing, we set P_i=0 for all the clock paths. By limiting the search range, we can obtain a linear equation on the path delays from root to sinks. Besides the timing constraints, a set of bounds on ΔS_{ij} can also be implemented to control the slew rate of buffers. $SizeLowerBound \le \Delta S_{ij} \le SizeUpperBound$

3.2 Objective Function

For a pair of aggressor and victim, the coupling effect is mutual. That is, aggressor is also victim at the same time. For two coupled buffers with size S_a, S_v and a coupling capacitance C_C, the jitter effect is captured in Fig. 3. The jitter can be ignored when the rising time of aggressor and victim is far enough, and reaches to peak when the rising of aggressor and victim is aligned. Since the effect is mutual, there should be a symmetric curve on the other direction. That is, the aggressor becomes victim. It is demonstrated in Fig. 5. There are three curves in Fig. 5. The forward curve is the same as Fig. 3. Another curve backward is symmetric to forward at skew=0. One can observe that when the skew is less than 0, the jitter effect is dominated by forward curve, and when the skew is greater than 0, the effect is dominated by backward curve. The forward and backward curves are symmetric. We use a quadratic function $J_i = K_i \times Skew^2 + K_{i0}$, where $Skew = T_1 - T_2$ to fit the jitter effect.

Once the jitter for an individual coupling capacitance has been modeled. The cost function is the summation of all jitters. $Cost = \sum_i J_i = \sum_i K_i \times (T_m - T_n)^2 + K_{i0}$.

An example is given in Fig. 6. There are two coupling capacitances (C_{c1}, C_{c2}) in this example, so there are two terms in the objective functions to minimize

$$K_1 \times (T_3 - T_4)^2 + K_2 \times (T_5 - T_6)^2 ,$$

subject to

$$a_1 \times \Delta S_1 + a_2 \times \Delta S_2 = 0$$

$$a_1 \times \Delta S_1 + a_3 \times \Delta S_3 = 0$$

$$a_4 \times \Delta S_4 + a_5 \times \Delta S_5 = 0$$

$$a_4 \times \Delta S_4 + a_6 \times \Delta S_6 = 0$$

where

$$T_3 = T_{3,0} + a_1 \times \Delta S_1$$

$$T_4 = T_{4,0} + a_4 \times \Delta S_4$$

$$T_5 = T_{5,0} + a_1 \times \Delta S_1 + a_3 \times \Delta S_3$$

$T_6 = T_{6,0} + a_4 \times \Delta S_4 + a_5 \times \Delta S_5$. $T_{n,0}$ is the current path delay from root to node *n*.

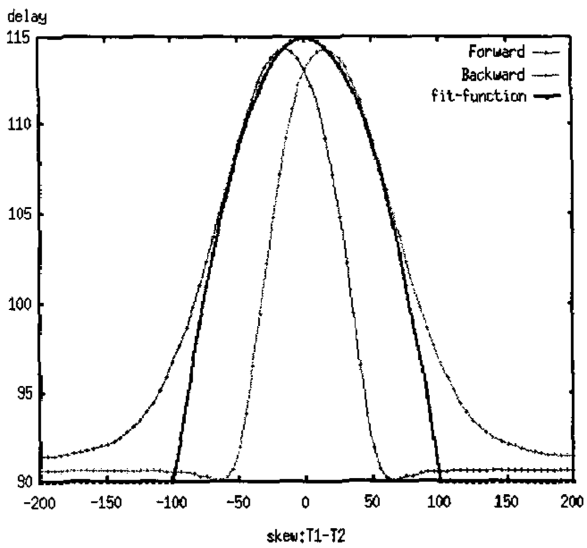

Fig. 5: Curve fitting for jitter effect, unit in ps

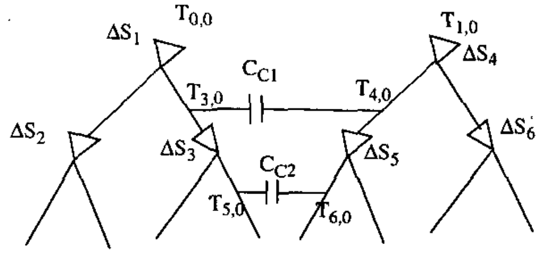

Fig. 6: Example of two coupling trees

4. Algorithm

To obtain the curve fit function, a set of possible combinations of S_a, S_v, and C_C was characterized before the optimization process. We use lookup table and interpolation to get K_i for a particular combination of S_a, S_v and C_{Ci} during the optimization process. The algorithm is based on an incremental process. In each iteration, we optimize

$J(S) = s^T P s + Q s + R$, where s= (Δs_1, Δs_2, Δs_3,..., Δs_n)

subject to $As = 0, s \le B$, where B is the bound for Δs_n.

Only small amount of buffer size Δs is allowed to change. We minimize the quadratic objective function based on the linear constraint in each iteration. The new state is updated and forms another objective function. The process stops when all the ΔS_i equal to zero or the number of iteration exceeds the limitation.

Procedure Buffer Sizing
Input:
Buffered Clock Trees, and Coupling Capacitance
Output:
Clock Buffers with Adjusted Size
Begin
Calculate Internal Node Delay
While Not Converge
    Calculate a_i for all C_{Ci}
    Do Qudratic Optimization on Current Trees
    Update the Size of Buffers Based on Optimization Result
    Re-Calculate Internal Node Delay
End While

5. Experimental Results

We have implemented the algorithm using GNU C++ running under Linux operating system. Since there were no benchmarks for this problem. We use the five test cases in [1][5]. These test cases tackle a specific version of this problem. There are two clock tress in each case, and the clock trees couple with each other. There are no explicit timing relationship between the clock trees. To get the timing relationship, we first fix the timing of tree 1, and scan the timing of tree2 to locate the worst timing where the maximum jitter occurs. Then we use the worst timing relationship as the input to our algorithm to see if the algorithm can reduce the maximum jitter on the given timing relationship. We use LINGO as our solver for the quadratic optimization. Table 1 shows the details of these test cases. In all the five cases, C_c have already been minimized. Table 2 shows the experimental results. We can see that for all the test cases, our algorithm can reduce the maximum clock jitter by average 50% on all the test cases for a given timing.

6. Conclusion

In this paper we have described an effective algorithm for the coupled clock network buffer sizing problem. We have formulated the problem as an incremental quadratic optimization problem. A quadratic cost function is used to capture the jitter for a coupled and buffered transmission line. Our experimental results indicate that our algorithm reduces the clock jitter by 50% on the average for the five test cases.

TABLE 1. Test Cases

	# Sink Node	C_C (FF)
Ex 1024	1024x2	385.51
Ex 512	512x2	62.10
Ex 256	256x2	107.18
Ex 128	128x2	22.67
Ex 64	64x2	23.82

TABLE 2. Experimental Results

	Initial Jitter (Positive/ Negative)/ps	Initial Total Jitter/ps	Optimized Jitter (Positive /Negative)/ps	Optimized Total Jitter/ps	ΔSize %	Jitter Dec.%
Ex 1024	46.86/-32.77	79.63	23.12/-18.34	41.46	+1.2%	-47.93%
Ex 512	27.84/-14.16	42.00	12.81/-10.59	23.40	-7.7%	-44.28%
Ex 256	15.84/-11.85	27.69	10.56/-3.50	14.06	-6.7%	-49.22%
Ex 128	7.41/-8.36	15.77	3.70/-2.58	6.28	-7.7%	-60.18%
Ex 64	15.9/-12.75	28.65	4.25/-2.10	6.35	+4.3%	-77.84%

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