Extrinsic Elements Extraction of DGMESFET

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Abstract

A procedure for the extraction of extrinsic elements of dual-gate MESFET (DGMESFET) is described in this paper. It is the first time to accurately extract the extrinsic elements of series resistance by considering the distributed channel resistance under the regions of two gates with the use of "end resistance measurement" method. The extrinsic elements of capacitance and inductance are extracted by three-port Y-matrix and Z-matrix calculation from cold measurements. The developed procedure is useful for the characterization of DGMESFET.

Introduction

To design a microwave circuit using DGMESFET, an equivalent circuit at operational bias condition is required. The small-signal models [1]-[3] and large-signal model [4] have been proposed by many authors. In those papers, the equivalent circuit of DGMESFET is basically composed by cascoding two single gate MESFETs (SGMESFET) embedded by extrinsic parasitic elements. Fig.1 shows a typical small-signal equivalent circuit of a coplanar DGMESFET. Since the connection between two intrinsic FETs can not be directly measured from probes, it is not easy to find the analytical formula to extract the intrinsic and extrinsic elements as in the SGMESFET case [5]. In this paper, we will describe the developed extraction procedure for the extrinsic elements of DGMESFET.

For a DGMESFET, the values of extrinsic series resistance can be estimated from physical modeling [1],[6] or derived by empirical formula with the distributed channel resistance under the regions of two gates to be neglected [2],[3]. In this paper, a circuit model of cold DGMESFET is proposed to consider the distributed channel resistance. The precise values of extrinsic series resistance can then be extracted by using the "end resistance measurement" method [7]. The extrinsic elements of capacitance and inductance are extracted using three-port Y-parameter and Z-parameter calculation from the cold measurements with DGMESFET at forward bias and reverse bias accordingly.

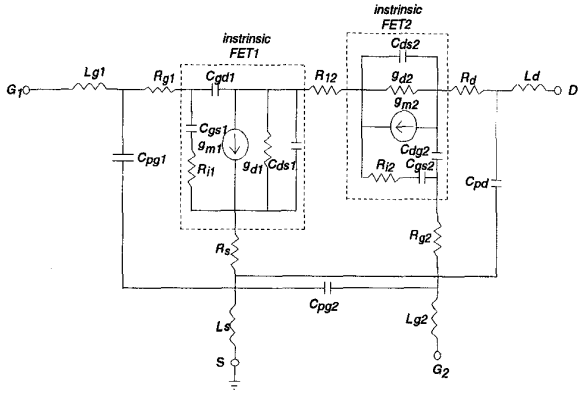

Fig.1 A small-signal equivalent circuit of DGMESFET.

Series Extrinsic Resistance Extraction

The schematic diagram to describe the DC behavior of a cold DGMESFET under forward bias is shown in Fig.2. Five independent equations with seven unknowns can be acquired from the "end resistance measurement" method as follows

$$\frac{\Delta V_{g1s}}{\Delta I_{g1s}}|_{Drain floating} = R_{g1} + \frac{n_1 V_T}{I_{g1s}} + \frac{R_{c1}}{3} + R_s, \quad (1)$$

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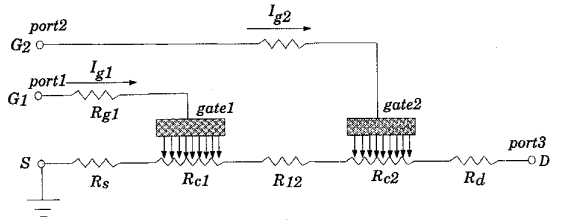

Fig. 2 Schematic diagram of a DGMESFET for "end resistance measurement" method. R_{g1}, R_{g2}, R_s and R_d are gate1 , gate2 , source, and drain resistances. R_{c1}, R_{c2} are the distributed channel resitance under the regions of gate1 and gate, respectively. R_{12} is the bulk resitance between gate1 and gate2.

$$\frac{\triangle V_{g2s}}{\triangle I_{g2s}}|_{Drain floating} = R_{g2} + \frac{n_2 V_T}{I_{g2s}} + \frac{R_{c2}}{3} + R_{12} + R_{c1} + R_d, \quad (2)$$

$$\frac{\triangle V_{g2d}}{\triangle I_{g2d}}|_{Source floating} = R_{g2} + \frac{n_2 V_T}{I_{g2d}} + \frac{R_{c2}}{3} + R_d, \quad (3)$$

$$\frac{\triangle V_{g1d}}{\triangle I_{g1d}}|_{Source floating} = R_{g1} + \frac{n_1 V_T}{I_{g1d}} + \frac{R_{c1}}{3} + R_{12} + R_{c2} + R_d, \quad (4)$$

$$\frac{V_{ds}}{I_{g1s}}|_{Drain floating} = R_{c1} + R_s. \quad (5)$$

Equation 1 shows a straight line for $V_{g1s} - I_{g1s}$ characteristics with $n_1 V_T$ as the slope and $R_{g1} + \frac{R_{c1}}{3} + R_s$ as the intercept point. Therefore from a set of measurements of current I_{g1s} and voltage V_{g1s} with floating drain terminal, the mean values of $\frac{\triangle V_{g1s}}{\triangle I_{g1s}}$ can be calculated to solve $n_1 V_T$ and $R_{g1} + \frac{R_{c1}}{3} + R_s$ by a least square error method. By using the same process, (1)-(4) become the following three-port Z-parameter expression

$$R_{11} = R_{g1} + \frac{R_{c1}}{3} + R_g, \quad (6)$$

$$R_{22} = R_{g2} + \frac{R_{c2}}{3} + R_{12} + R_{c1} + R_d, \quad (7)$$

$$R_{32} = R_{g2} + \frac{R_{c2}}{3} + R_d, \quad (8)$$

$$R_{31} = R_{g1} + \frac{R_{c1}}{3} + R_{12} + R_{c2} + R_d, \quad (9)$$

and (5) can be rewritten as

$$R_x = \frac{R_{c1}}{2} + R_s. \quad (10)$$

Two additional equations for solving seven extrinsic elements of series resistance can be selected from the following approaches

1 the relation of R_{c1} and R_{c2}, $R_{c1} = mR_{c2}$ provided the gate1 and gate2 channel length ratio m is known.

2 the value of $R_s + R_{12} + R_{c2} + R_d$ obtained from Hower and Bechte method [8] by floating gate2 terminal.

3 the values of R_{g1} and R_{g2} acquired from dummy pad resistance measurement.

4 the values of R_s and R_d of SGMESFET [5] provided the same device structure and processing in DGMESFET for source and drain terminals.

Extrinsic Capacitance Extraction

Figure 3 shows the equivalent circuit of a cold coplanar DGMESFET in which FET1 is reverse biased in pinched-off region and FET2 is forward biased in linear region. The imaginary part of the three-port Y-parameter, with frequency below a few gigaherhz, can be written as

$$Im(Y_{11}) = j\omega(C_{pg1} + 2C_{b1}), \quad (11)$$

$$Im(Y_{13}) = -j\omega(Cb1), \quad (12)$$

$$Im(Y_{22}) = j\omega(2C_{g2d} + 2C_{pg2}), \quad (13)$$

$$Im(Y_{23}) = -j\omega(2C_{g2d}), \quad (14)$$

$$Im(Y_{33}) = j\omega(C_{pd} + 2C_{g2d} + Cb1). \quad (15)$$

One can then solve the values of extrinsic capacitance C_{pg1}, C_{pg2}, C_{pd} and C_{g2d}.

Extrinsic Inductance Extraction

Figure 4 shows the equivalent circuit of a coplanar cold DGMESFET with FET1 and FET2 both at forward bias. The real part of the three-port Z-parameter, with frequency below a few gigahertz, can be written as

$$Re(Z_{11}) = j\omega(L_{g1} + L_s), \quad (16)$$

$$Re(Z_{22}) = j\omega(L_{g2} + L_s), \quad (17)$$

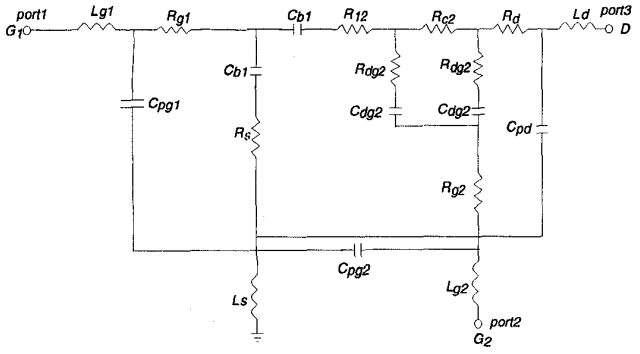

Fig. 3 An equivalent circuit of coplanar cold DGMESFET with FET1 reverse biased and FET2 forward biased.

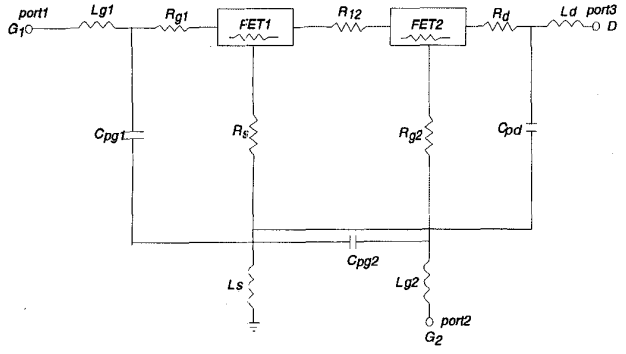

Fig. 4 An equivalent circuit of coplanar cold DGMESFET with FET1 and FET2 forward biased.

$$Re(Z_{33}) = j\omega(L_d + L_s), \tag{18}$$

$$Re(Z_{21}) = j\omega L_s. \tag{19}$$

One can then solve the values of extrinsic inductance L_{g1}, L_{g2}, L_s and L_d.

Measurement Results

A coplanar DGMESFET with $L_{g1}, L_{g2} = 1\mu m$ and $W_{g1}, W_{g2} = 4 \times 75\mu m$ fabricated by HEXAWAVE Co., is measured to extract the extrinsic elements. The three-port scattering matrix of DGMESFET is measured on wafer using an automated three-port network analyzer with associated calibration method developed in our laboratory. Figure 5 shows the measured results of $\frac{\Delta V_{g1s}}{\Delta I_{g1s}}$, $\frac{\Delta V_{g1d}}{\Delta I_{g1d}}$, $\frac{\Delta V_{g2s}}{\Delta I_{g2s}}$ and $\frac{\Delta V_{g2d}}{\Delta I_{g2d}}$ with floating drain terminal or source terminal, respectively. The three-port Y-parameter at biases $V_{g1s} < V_{th}, I_{g2} =$

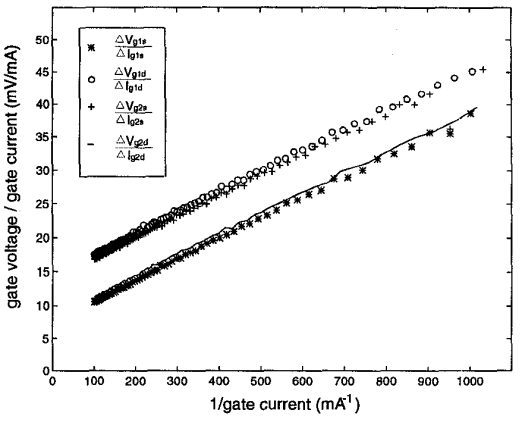

Fig. 5 Measured results of $\frac{\Delta V_{g1s}}{\Delta I_{g1s}}$, $\frac{\Delta V_{g1d}}{\Delta I_{g1d}}$, $\frac{\Delta V_{g2s}}{\Delta I_{g2s}}$, and $\frac{\Delta V_{g2d}}{\Delta I_{g2d}}$ at forward bias with floating drain terminal or source terminal, respectively.

$0.2mA$ and $V_{ds} = 0V$ are calculated from the on-wafer measurement of S-parameter. The results of $Im(Y_{11}), Im(Y_{22}), Im(Y_{21})$ and $Im(Y_{33})$ are shown in Fig. 6. Values of C_{pg1}, C_{pg2}, C_{pd} and C_b calculated from (11)-(15) are shown in Fig.7, and values of extrinsic inductance L_s and L_d are shown in Fig. 8. Table 1 summaries the extraction results of extrinsic elements of DGMESFET and the associated bias conditions.

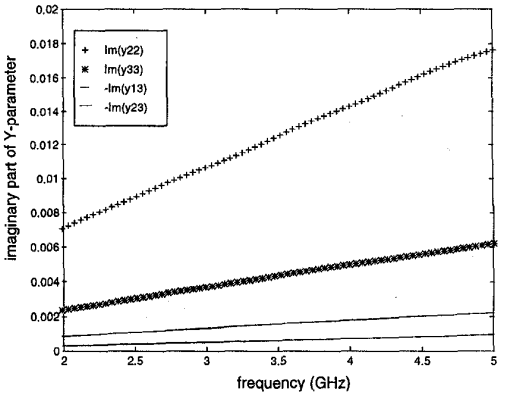

Fig. 6 Measured results of the imaginary part of three-ort Y-parameter , $V_{ds} = 0V, V_{g1s} = V_{th}$, and $I_{g2s} = 0.2mA$.

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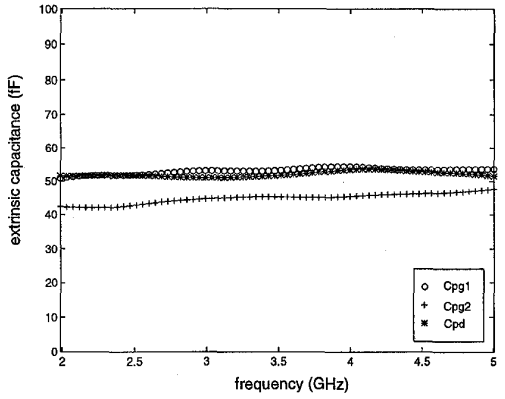

Fig. 7 Measured results of extrinsic elements of capacitance.

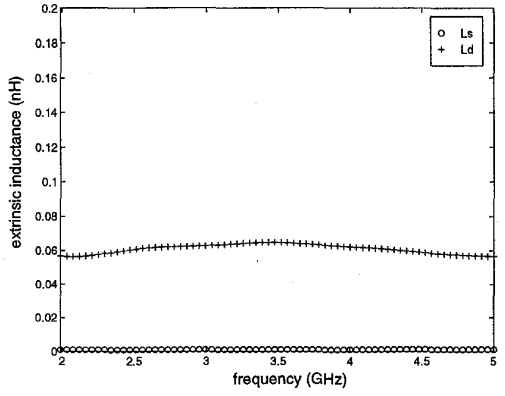

Fig. 8 Measured results of extrinsic elements of inductance.

cold measurement (Vds = 0V)		
Extrinsic Resistance (ohm)	*Extrinsic Capacitance (fF)*	*Extrinsic Inductance (nH)*
FET1: forward bias I g1=1-10mA *FET2: forward bias I g1=1-10mA* *with floating drain or source*	*FET1: reverse bias V g1s< Vth* *FET2: forward bias I g1=0.2mA*	*FET1: forward bias I g1 = 0.2mA* *FET2: forward bias I g1=0.2mA*
Rg1 = 1.59 *Rg2 = 1.52* *Rs = 3.68* *Rd = 3.59* *R12 = 3.1* *Rc1 = 3.05* *Rc2 = 3.05*	*Cpg1 = 53* *Cpg2 = 44* *Cpd = 52*	*Ls = 0.003* *Ld = 0.065* *Lg1 = 0.002* *Lg2 = 0.002*

Table 1 Values of extrinsic elements of DGMESFET and measured bias condition.

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