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A Novel 0.7V Two-Port 6T SRAM Memory Cell Structure with Single-Bit-Line Simultaneous Read-and-Write Access (SBLSRWA) Capability using Partially-Depleted SOI CMOS Dynamic-Threshold Technique

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Abstract

This paper reports a novel low-voltage two-port 6T SRAM memory cell structure with single-bit-line simultaneous read-and-write access capability using partially-depleted SOI CMOS dynamic-threshold technique. With an innovative approach by connecting the body terminal of an NMOS device in the latch and the write access pass transistor to the write word line, this 6T memory cell can be used to provide SBLSRWA capability for 0.7V two-port SOI CMOS VLSI SRAM as verified by MEDICI results.

Summary

For standard two-port SRAMs with simultaneous read and write capability, two more pass transistors and an extra pair of bit lines in addition to the conventional 6T SRAM memory cell are needed. Techniques with single-bit-line read and write have been studied for reducing the size of the two-port SRAM memory cell[1]. However, for the 6T SRAM memory cell with the single-bit-line write structure, write logic-1 operation via the single bit line is difficult due to the the ratioed logic structure involved. This problem is especially serious for the low-voltage environment. Recently, SOI CMOS dynamic threshold technique has been reported for its advantages in low-voltage logic circuits [2][3]. In this paper, by using the dynamic threshold technique in connecting the body terminal of an NMOS device in the latch and the write access pass transistor to the write word line, a 6T memory cell with the single-bit-line simultaneous read-and-write access for 0.7V two-port SOI CMOS VLSI SRAM is described.

Fig. 1 shows the 0.7V two-port 6T SRAM memory cell structure with single-bit-line simultaneous read-and-write access (SBLSRWA) capability using partially-depleted SOI CMOS dynamic-threshold technique. As shown in the figure, the body terminal of the NMOS device M_{N4} in the latch is connected to the write word line (WWL) instead of floating as in the conventional SOI CMOS SRAM memory cell. In the SBLSRWA memory cell, the left side is connected to the write bit line (WBL) via the pass transistor M_{N1}, which is controlled by write word line (WWL) and with its body tied to WWL. The right side of the SBLSRWA SRAM memory cell is connected to the read bit line (RBL) via the pass transistor M_{N2}, which is controlled by the read word line (RWL). By this arrangement, simultaneous read and write accesses of the SBLSRWA SRAM memory cell can be facilitated. Consider the write-logic-1 operation with logic-0 stored at node n1 initially and WBL is high at 0.7V. During the single-bit-line write-logic-1 operation, when WWL becomes high, the body of the NMOS devices M_{N1} and M_{N4} is tied to high at 0.7V. Due to the DTMOS effect, the threshold voltage of M_{N4} and M_{N1} is lowered such that both M_{N4} and M_{N1} turn on faster. As a result, M_{N3} turns off faster and node n1 is pulled to 0.7V more easily. When the write access is over, WWL becomes low at 0V, the threshold voltage of M_{N4} and M_{N1} goes back to its original value. In order to investigate the effectiveness of the new 2-port SRAM memory cell, transients during the write access of this SBLSRWA SRAM memory cell at 0.7V have been studied. In the SBLSRWA SRAM memory cell under study, all six transistors have an aspect ratio of $0.3\mu m/0.2\mu m$. Two parasitic capacitances of $0.1pF$ are placed at WBL and RBL. Fig. 2 shows the transient waveforms during the write access of this SBLSRWA 6T SRAM memory cell at V_{dd} of 0.7V from MEDICI simulation results based on a $0.2\mu m$ partially-depleted SOI CMOS technology. As shown in the figure, at V_{dd} of 0.7V, for the four cases of the write access—(1) logic-0→ logic-0 (logic-0 is written into the storage node n1, which is stored with logic-0 initially), (2) logic-0→ logic-1, (3) logic-1→ logic-1, and (4) logic-1→ logic-0, write operations can be done for this two-port SBLSRWA 6T SRAM memory cell using this innovative structure. Without using this innovative structure, single-bit-line write-logic-1 operation of the two-port 6T SRAM cell at V_{dd} of 0.7V is not possible.

References

[1] K. Sasaki, et al, "A 16-Mb CMOS SRAM with a $2.3\mu m^2$ Single-Bit-Line Memory Cell," *IEEE J. Solid-St. Ckts*, Vol. 28, pp. 1125-1130, Nov. 1993.

[2] J. B. Kuo and K. W. Su, "CMOS VLSI Engineering: Silicon-on-Insulator (SOI)," *Kluwer: Dordrecht*, 1998.

[3] F. Assaderaghi, et al, "A Dynamic Threshold voltage MOSFET (DTMOS) for Very Low Voltage Operation," 1994.

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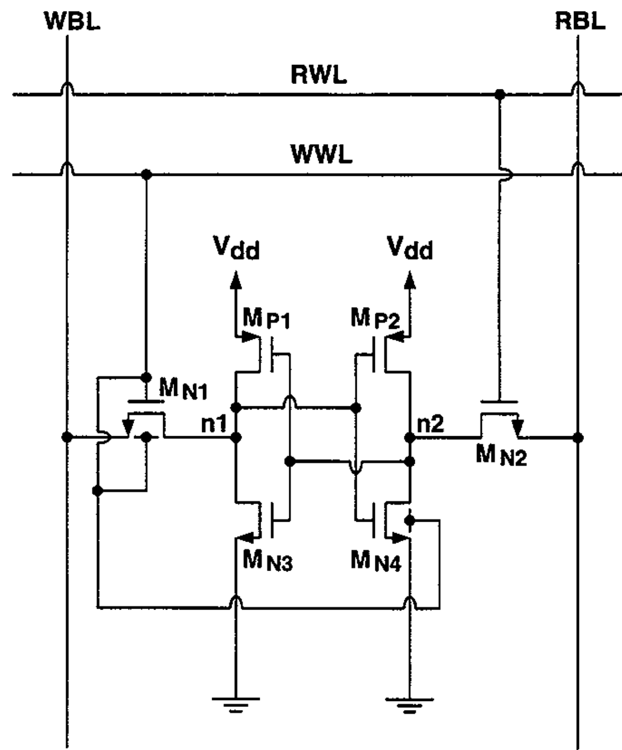

Fig.1 0.7V two-port 6T SRAM memory cell structure with single-bit-line simultaneous read-and-write access (SBLSRWA) capability using partially-depleted SOI CMOS dynamic-threshold technique.

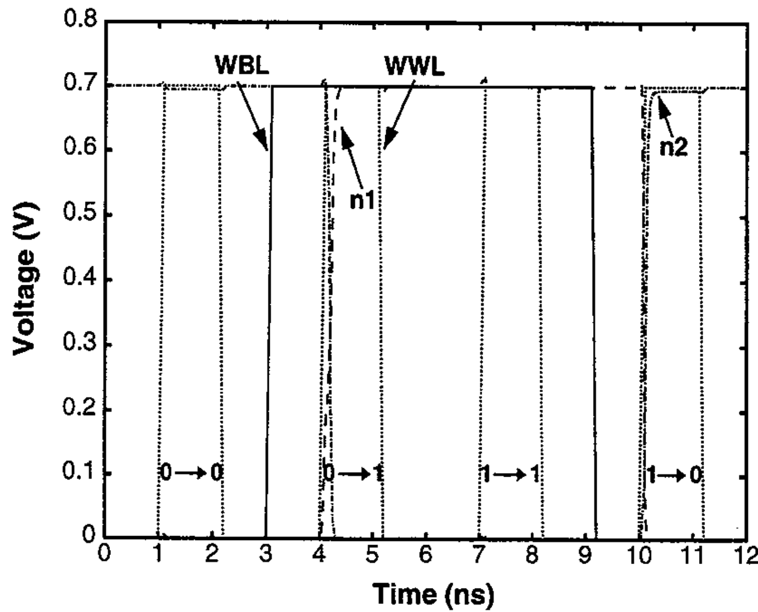

Fig.2 Transients during the write access of the 0.7V partially-depleted SOI CMOS two-port 6T SBLSRWA SRAM memory cell.