

# Simple analytical model for short-channel MOS devices

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**Abstract:** A simple analytical model derived from a quasi-two-dimensional analysis with a non-vanishing  $E$ -field derivative at the pinchoff point and a continuous output conductance at the transition point for short-channel MOSFETs is presented. This model also covers mobility reduction, carrier velocity saturation, body, channel-length modulation, source-drain series resistance and short-channel effects for an accurate determination of the pinchoff point location without internal numerical iterations as compared to other models. This model can be used to describe the channel-length modulation effects more accurately in circuit simulation with short-channel MOSFETs.

## 1 Introduction

The growing applications of MOS analogue and digital circuits for VLSI systems have triggered a strong demand in accurate circuit simulation, which depends on accurate and efficient MOS device models. The existing MOS device models intensively used are based on a quasi-two-dimensional analysis (QTDA) [1], which has been used to estimate the lateral electric field near the drain region successfully by assuming a negligible field derivative at the pinchoff point [2]. However, the derived output conductance is discontinuous at the transition point. As a result, for a large gate voltage the accuracy of the predicted drain current is not sufficient for accurate circuit simulation. Despite a proposed modified model [3], substantial internal iterations are required to solve for the drain saturation voltage and the length of the post-velocity-saturation region. Although another better analytical model was developed to improve the QTDA model [4], the source-drain series resistance and short-channel effects were not considered.

In this paper, a simple analytical MOS transistor model suitable for circuit simulation, including mobility reduction, carrier velocity saturation, body, channel-length modulation, source-drain series resistance and short-channel effects, is presented. The model is based on a two-section approach; i.e. the channel region is divided into two sections. In the source section, gradual channel approximation (GCA) is used [5], whereas in the drain

section QTDA is applied accounting for the two-dimensional field distribution. Instead of assuming a zero  $E$ -field derivative at the pinchoff point, as in the unified model [2], the proposed model assumes that the  $E$ -field derivative at the pinchoff point is nonvanishing and the output conductance is continuous at the transition point by introducing a source-drain series resistance dependent scaling factor. Furthermore, owing to the inclusion of the source-drain series resistance and short-channel effects, the location of the pinchoff point is more accurately determined as compared to the other model [4], especially for large gate and drain voltages.

## 2 Simple model

### 2.1 Linear region

For an MOS transistor biased in the linear region, the drift drain current is

$$I_{DL} = W(Q_m(y))v_y(y) \quad (1)$$

where  $y$  is the direction along the channel;  $W$  is the channel width;  $v_y(y)$  is the electron drift velocity; and  $Q_m(y)$  is the inversion layer charge density per unit surface area. To include the source-drain series resistance, we insert both the source resistance,  $R_s$ , and the drain resistance,  $R_d$ , in series with the source and the drain terminals, respectively. In this model,  $R_s = R_d = R$  is assumed for simplicity. By modifying Reference 3,  $Q_m(y)$  is given below

$$Q_m(y) = C_{ox}(V'_{GS} - V_T - 2a_0 V_y(y)) \quad (2)$$

where

$$V'_{GS} = V_{GS} - I_{DL} R \quad (3)$$

$$2a_0 = 1 + \frac{\gamma F d}{2\sqrt{(2\phi_f + V_{SB})}} \quad (4)$$

$$V_T = 2\phi_f + V_{FB} + \gamma F \sqrt{(2\phi_f + V_{SB})} \quad (5)$$

and

$$\gamma = \frac{\sqrt{(2\epsilon_s q N_A)}}{C_{ox}} \quad (6)$$

where  $V_y(y)$  is the channel potential;  $F$  is a geometrical factor accounting for short-channel effects [6];  $d$  is introduced as a correction factor compensating for the Taylor series expansion error [14]; and the other symbols have their conventional meanings.

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As for  $v_y(y)$ , a simple two-region piecewise empirical velocity-field model is used [7]:

$$v_y(y) = \frac{\mu_{eff} E_y(y)}{1 + \frac{E_y(y)}{E_c}} \quad E_y(y) \leq E_c \quad (7)$$

$$= v_{sat} \quad E_y(y) > E_c \quad (8)$$

where  $E_y(y)$  is the lateral electric field;  $E_c$  is the critical field;  $v_{sat}$  is the saturated velocity; and  $\mu_{eff}$  is the effective mobility given by the following expression which satisfies both simplicity and accuracy:

$$\mu_{eff} = \frac{\mu_0}{1 + \theta_A(V_G - V_T) + \theta_B V_{SB}} \quad (9)$$

where  $\mu_0$  is the low field mobility;  $\theta_A$  is the mobility reduction factor due to the transverse field [8]; and  $\theta_B$  represents the substrate bias effect [15].

Assuming no velocity saturation in channel, and integrating the drift drain current equation over the whole channel length  $L$  with the source-drain series resistance effect, the drain current in the linear region is expressed as

$$I_{DL} = \frac{-A_2 + \sqrt{(A_2^2 + 4A_1 I_{D0})}}{2A_1} \quad (10)$$

where

$$A_1 = \left( 2W\mu_{eff} C_{ox} R^2 (2a_0 - 1) - \frac{2R}{E_c} \right) \left( L + \frac{V_{DS}}{E_c} \right) \quad (11)$$

$$A_2 = \frac{2RI_{DD}}{V_{DS}} - \frac{W\mu_{eff} C_{ox} V_{DS} R (2a_0 - 1)}{L + \frac{V_{DS}}{E_c}} + 1 \quad (12)$$

and

$$I_{D0} = W\mu_{eff} C_{ox} \frac{(V_{GS} - V_T - a_0 V_{DS}) V_{DS}}{L \left( 1 + \frac{V_{DS}}{LE_c} \right)} \quad (13)$$

## 2.2 Drain saturation voltage

As the internal drain voltage (the applied terminal voltage less the voltage drops across the source and the drain resistances) is increased, the lateral electric field in the channel close to drain will reach the critical field  $E_c$  and the carriers will travel with the saturated velocity. Using a similar approach to that of Reference 9, the internal drain saturation voltage,  $V_{dsat}$ , which is defined as the channel potential where carriers reach the saturated velocity, can be obtained:

$$V_{dsat} = \frac{-A_4 + \sqrt{(A_4^2 + 4A_3 A_5)}}{2A_3} \quad (14)$$

where

$$A_3 = a_0 W\mu_{eff} C_{ox} R E_c \quad (15)$$

$$A_4 = V_{GS} - V_T + 2a_0 L E_c \quad (16)$$

and

$$A_5 = L E_c (V_{GS} - V_T) \quad (17)$$

For the external drain saturation voltage,  $V_{DSAT}$ , it is given by the relation below:

$$V_{DSAT} = V_{dsat} + 2RI_{DS} \quad (18)$$

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where  $I_{DS}$  is the drain current at the onset of saturation. As compared to the other saturation voltage model [9], the new model has included the source-drain series resistance and short-channel effects.

## 2.3 Saturation region

For an MOS transistor biased in the saturation region, the channel region can be divided into the source and the drain sections, where GCA and QTDA have applied, respectively. Accounting for the channel-length modulation effect, the drain current,  $I_{DSAT}$ , in the saturation region is now organised as

$$I_{DSAT} = \frac{I_{DS}}{1 - \frac{s \cdot L_{SAT}}{L_{eq}}} \quad (19)$$

where  $L_{eq}$ , the equivalent channel length, is defined as

$$L_{eq} = L \left( 1 + \frac{V_{dsat}}{L E_c} \right) + W\mu_{eff} C_{ox} V_{dsat} R \quad (20)$$

and  $(s \cdot L_{SAT})$  is treated as the actual channel-shortening length in this simple model.  $s$  is a source-drain series resistance dependent scaling factor introduced to ensure both the continuity of the drain current and the output conductance at the transition point from linear to saturation. Its value is determined by equating both the output conductance in the linear region and in the saturation region at the onset of saturation as given in the Appendix. The saturation region length,  $L_{SAT}$ , is the length of channel near the drain section where carriers travel with the saturated velocity. Note that  $L_{SAT}$  becomes zero at the onset of saturation, ensuring the continuity of the output conductance at the pinchoff point by introducing  $s$ .

To compute  $L_{SAT}$  as shown in Fig. 1, we apply QTDA to the drain region with a selected Gaussian box of width  $X_j/\eta$  enclosing the mobile and the bulk charges.  $X_j$  is the drain junction depth and  $\eta$  is a fitting parameter [2, 10]. Applying Gauss's law to the rectangular box area with four boundary conditions, and differentiating the resulting equation with respect to the lateral dimension  $y$ , we can obtain a differential equation in terms of  $E_y$  at the surface as given below [11]:

$$\frac{X_j}{\eta} \frac{dE_y(y)}{dy} = \frac{\epsilon_{ox}}{\epsilon_s} E_{ox}(y) - \frac{1}{\epsilon_s} (qN_A X_j + Q_m(y)) \quad (21)$$

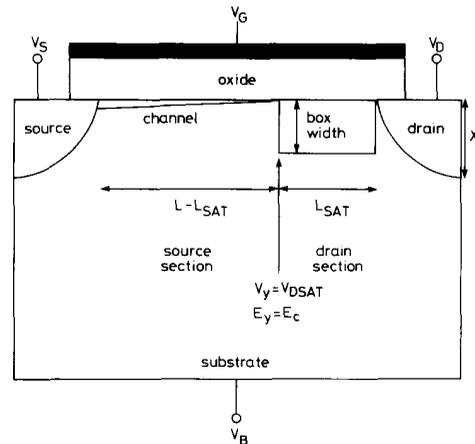


Fig. 1 Definition of the drain region

where  $\epsilon_{ox}$  is the oxide permittivity. Based on GCA,  $Q_m(y)$  at the pinchoff point is given by

$$Q_m(-L_{SAT}) = C_{ox}(V'_{GS} - V_T - 2a_0 V_{dsat}) \quad (22)$$

After rearrangement,  $Q_m(-L_{SAT})$  is expressed as

$$Q_m(-L_{SAT}) = \frac{C_{ox}(V_{GS} - V_T - 2a_0 V_{dsat})}{1 + 0.5\mu_{eff}WC_{ox}RE_c} \quad (23)$$

Using  $dE_y(y)/dy = -d^2V_y(y)/dy^2$  and eqn. 23, eqn. 21 can be rearranged as

$$\frac{d^2V_y(y)}{dy^2} = \frac{V_y(y) - V_{dsat}^*}{l^2} + \frac{q\eta N_A}{\epsilon_s} \quad (24)$$

where

$$V_{dsat}^* = V_G - V_{FB} - 2\phi_f - \frac{(V_G - V_T - 2a_0 V_{dsat})}{1 + 0.5\mu_{eff}WC_{ox}RE_c} \quad (25)$$

and

$$l^2 = \frac{\epsilon_s X_i}{\eta C_{ox}} \quad (26)$$

Note that the field derivative at the pinchoff point is nonvanishing. Solving eqn. 24 subject to the boundary conditions  $V_y(-L_{SAT}) = V_{DSAT}$  and  $|E_y(-L_{SAT})| = E_c$ , we obtain

$$\begin{aligned} V_y(y) - V_{dsat}^* &= lE_c \sinh\left(\frac{y + L_{SAT}}{l}\right) \\ &+ \left(V'_{dsat} - V_{dsat}^* + \frac{q\eta N_A l^2}{\epsilon_s}\right) \\ &\times \cosh\left(\frac{y + L_{SAT}}{l}\right) - \frac{q\eta N_A l^2}{\epsilon_s} \end{aligned} \quad (27)$$

and

$$\begin{aligned} |E_y(y)| &= E_c \cosh\left(\frac{y + L_{SAT}}{l}\right) \\ &+ \left(\frac{V_{DSAT} - V_{dsat}^* + (q\eta N_A l^2/\epsilon_s)}{l}\right) \\ &\times \sinh\left(\frac{y + L_{SAT}}{l}\right) \end{aligned} \quad (28)$$

With the drain voltage  $V_y(0) = V_D$ ,  $L_{SAT}$  is given as

$$L_{SAT} = l \ln\left(\frac{c + \sqrt{(c^2 - k_2^2 + k_1^2)}}{k_1 + k_2}\right) \quad (29)$$

where

$$c = V_D - V_{dsat}^* + \frac{q\eta N_A l^2}{\epsilon_s} \quad (30)$$

$$k_1 = lE_c \quad (31)$$

and

$$k_2 = V_{DSAT} - V_{dsat}^* + \frac{q\eta N_A l^2}{\epsilon_s} \quad (32)$$

From the above analysis, an analytical solution for  $L_{SAT}$ , the drain region length, has been obtained. Consequently, the drain current can be computed directly from the terminal voltages; no iterations are required as they are in other models [3, 12].

### 3 Comparisons with experimental data

In this section, the DC performance of two nMOS devices with parameters listed in Table 1 [2, 13] is analysed using the simple analytical model. The  $I_D$  against  $V_{DS}$  characteristics of the two devices with channel lengths of  $L = 1.09 \mu\text{m}$  and  $1.45 \mu\text{m}$  are shown in Figs. 2 and 3. A good agreement (within 3.5% average error for device A and 1.6% for device B) between the model results and the experimental data [2, 13] has been observed over the whole range of applied gate and drain voltages. This accuracy is attributed to the accurate estimate of the pinchoff point location resulting from the inclusion of short-channel effects and the nonvanishing E-field derivative at the pinchoff point, as well as the source-drain series resistance effect.

Table 1: Device parameters

Parameters	Device A	Device B	Units
Type	nMOS	nMOS	
Substrate doping ( $N_A$ )	6.63E15	2E15	$\text{cm}^{-3}$
Gate-oxide thickness ( $t_{ox}$ )	358	300	Å
Channel length ( $L$ )	1.09	1.45	$\mu\text{m}$
Channel width ( $W$ )	100	10	$\mu\text{m}$

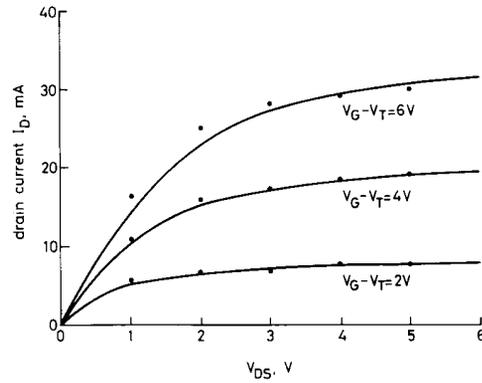


Fig. 2 The I-V characteristics of the nMOS device with a channel length of  $1.09 \mu\text{m}$  and a channel width of  $100 \mu\text{m}$   
 ●●● experimental data [2]  
 — model predictions

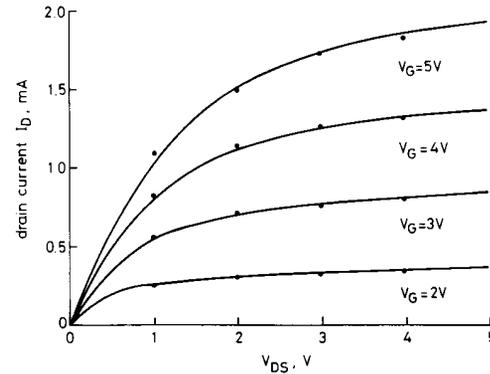


Fig. 3 The I-V characteristics of the nMOS transistor with a channel length of  $1.45 \mu\text{m}$  and a channel width of  $10 \mu\text{m}$   
 ●●● experimental data [13]  
 — model predictions

Fig. 4 shows the saturation voltage,  $V_{DSAT}$ , based on the simple model and other model [9] for the device with a channel length of  $1.09 \mu\text{m}$ . The  $V_{DSAT}$  derived from the simple model will substantially deviate from the other model as the source-drain series resistance increases. In fact, as the effective channel length shrinks down to the submicrometre range, the source-drain series resistance becomes significant. Therefore, to obtain more accurate circuit simulation results, its effect on both the drain saturation voltage and the current-voltage characteristics should be considered.

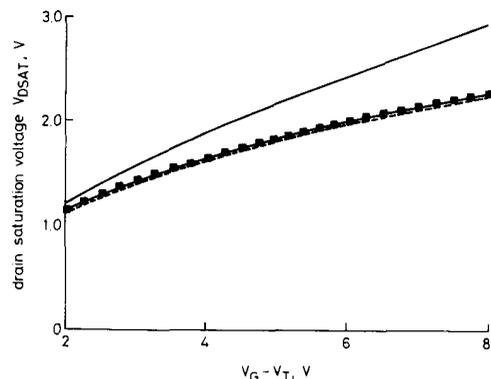


Fig. 4 The saturation voltage,  $V_{DSAT}$ , for the nMOS device with a channel length of  $1.09 \mu\text{m}$

—■— see Reference 9  
 - - -  $R = 0.01 \Omega$   
 —  $R = 10 \Omega$

The output conductance estimated by the simple analytical model for the device with a  $1.45 \mu\text{m}$  channel length is compared with the experimental data in Fig. 5 [13]. Note that the continuity of the output conductance is maintained by introducing  $s$ . Fig. 6 shows the channel-shortening length derived from the proposed model and the other existing model [4] without an LDD structure for the nMOS device with a gate-oxide thickness of  $358 \text{ \AA}$  and a channel length of  $1.09 \mu\text{m}$ . The magnitude of  $(s \cdot L_{SAT})$  derived from this model shows a significant difference from Huang's results. As the gate-source voltage increases, the voltage drop across the source-drain series

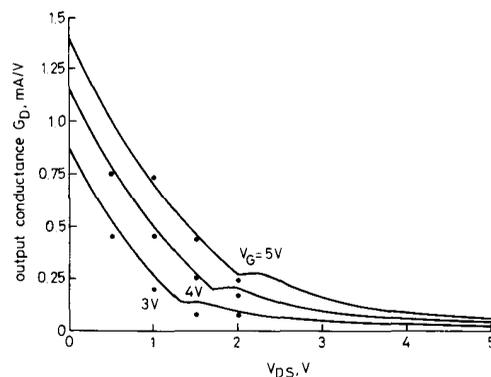


Fig. 5 The output conductance of the nMOS device with a channel length of  $1.45 \mu\text{m}$

●●● experimental data [13]  
 — model predictions

resistance becomes larger due to a larger drain current. Consequently, the drain saturation voltage increases and the effective gate-source voltage becomes less when compared to the case without the source-drain series resistance as in Huang's model. The combined effect is that the channel-shortening length calculated by this model is much less than that of Reference 4 which overestimates the drain region length. It is to be noted that to achieve more accurate results the bias-dependent source-drain series resistance has to be considered instead of a constant resistor. The advantages of the simple model can be exploited in very short-channel MOS devices with a small gate-oxide thickness, owing to a large drain current density. As a result, the well modelled channel-length modulation becomes more important for accurate circuit simulation. Therefore, the simple model is favourable for circuit simulation of short-channel MOS devices.

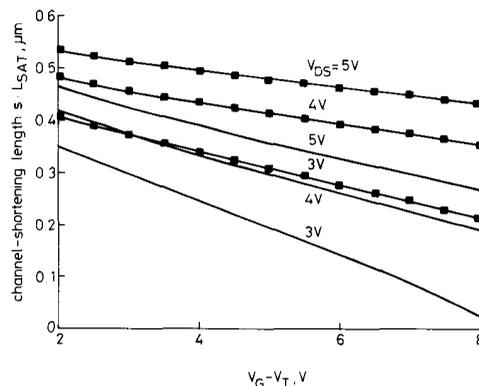


Fig. 6 The channel-shortening length,  $(s \cdot L_{SAT})$ , as defined in Fig. 1, for the nMOS device with a channel length of  $1.09 \mu\text{m}$

—■— see Reference 4  
 — model predictions

#### 4 Conclusion

In this paper we have presented a simple analytical short-channel MOSFET model suitable for circuit simulation. In the proposed model, both a nonvanishing  $E$ -field derivative at the pinch-off point and a continuous output conductance at the transition point hold. Second-order effects, such as mobility reduction, carrier velocity saturation, body, channel-length modulation, source-drain series resistance and short-channel effects, are also included. From comparisons, we have observed that the current-voltage characteristics predicted by this model shows a satisfactory agreement with the reported experimental data over a wide range of applied voltages. Furthermore, it should be mentioned that for these two devices biased in saturation the effective channel length becomes near or less than  $1 \mu\text{m}$ . In addition, the calculated output conductance has been compared with the experimental data, and the source-drain series resistance effect on the drain saturation voltage has been discussed. Finally, we have presented calculated results of the channel-shortening length and reasons for the difference from the other existing model have been given. In conclusion, due to the validity of this model and the fact that no internal numerical iterations are required, accurate and efficient circuit simulation results of short-channel MOSFETs can be obtained if this simple analytical device model is used.

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## 6 Appendix

The source-drain series resistance dependent scaling factor,  $s$ , is determined by equating both the output conductance in the linear region and in the saturation region at the onset of saturation, as given below

$$G_{DL} = \frac{a_1}{2} \left( -\frac{\partial a_2}{\partial V_{DS}} + \frac{a_2}{\partial V_{DS}} + \frac{2}{a_1} \frac{\partial a_3}{\partial V_{DS}} \right) \quad (33)$$

and

$$G_{DS} = \frac{I_{DS} \cdot s}{\left( 1 - \frac{s \cdot L_{SAT}}{L_{eq}} \right)^2 L_{eq} E_y(0)} \quad (34)$$

where  $a_1 = (A_1(L_{eff} + (V_{DS}/E_c)))^{-1}$ ,  $a_2 = A_2(L_{eff} + (V_{DS}/E_c))$  and  $a_3 = I_{D0}(L_{eff} + (V_{DS}/E_c))$ . Therefore,

$$s = \frac{L_{eq} E_c G_{DL} |_{V_{DS} = V_{DSAT}}}{I_{DS}} \quad (35)$$