# Current-mode full-wave rectifier and vector summation circuit

## Cheng-Chieh Chang and Shen-Iuan Liu

A current-mode full-wave rectifier and current-mode vector summation circuit are presented. They are implemented by utilising the square-law characteristics of MOS transistors in saturation. A two-input vector summation circuit using the proposed full-wave rectifier has been fabricated in a 0.8 µm <sup>2</sup> CMOS process. The experimental and simulation results confirm the feasibility of the proposed circuits.

Introduction: Owing to the square-law characteristics of MOS transistors, many squarer and multiplier circuits [1 - 4] have been proposed. Some rectifiers and vector summation circuits [5, 6] have been developed based on the square-law characteristics of MOS transistors. In this Letter, a current-mode rectifier and a vector summation circuit are proposed. A two-input vector summation circuit has also been fabricated in a 0.8µm CMOS process. The experimental and simulation results confirm the feasibility of the proposed current-mode full-wave rectifier and the vector summation circuit.

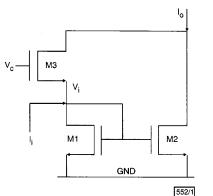
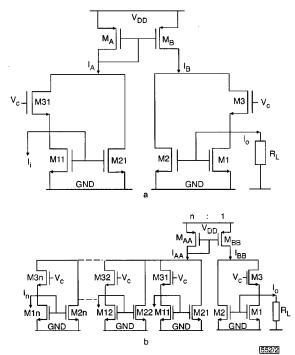


Fig. 1 Building block for proposed rectifier and vector summation circuit



**Fig. 2** Proposed rectifier and vector summation circuit a Proposed current-mode full-wave rectifier b Proposed current-mode vector summation circuit

*Circuit description:* The basic building block for realising the proposed current-mode full-wave rectifier and the vector summation

circuit is shown in Fig. 1 [7]. We neglect the body effect and assume that all the transistors operate in saturation and have the same transconductance parameters, K. The expression between the input current,  $I_i$ , and output current,  $I_o$ , can be given as [7]

$$I_O = \frac{K}{2} (V_C - 2V_T)^2 + \frac{I_i^2}{2K(V_C - 2V_T)^2}$$
(1)

where  $V_C$  is the biased voltage and  $V_T$  is threshold voltage. To keep all the transistors operating in saturation, the condition,  $|I_i| < K(V_C - 2V_T)^2$ , should be satisfied. The circuit in Fig. 1 can be regarded as the compound of a squarer and a DC current source.

Based on the building block of Fig. 1, a current-mode full-wave rectifier and a current-mode vector summation circuit are shown in Figs. 2a and b, respectively. According to eqn. 1, the current,  $I_A$ , in the left part of Fig. 2a can be expressed as

$$I_A = \frac{K}{2} (V_C - 2V_T)^2 + \frac{I_i^2}{2K(V_C - 2V_T)^2}$$
(2)

Since transistors  $M_A$  and  $M_B$  are constructed from a current mirror, we have  $I_B = I_A$ . In the right part of Fig. 2*a*, the output current,  $I_O$ , can be given as

$$I_O = \sqrt{2K(V_C - 2V_T)^2 \left[I_B - \frac{K}{2}(V_C - 2V_T)^2\right]}$$
(3)

Substituting eqn. 2 into eqn. 3, the rectified output current becomes

$$I_O = \sqrt{I_i^2} = |I_i| \tag{4}$$

The vector summation circuit shown in Fig. 2b is similar to the proposed rectifier with multiple input currents. The current,  $I_{AA}$ , is the summation of the output currents for n building blocks, as shown in Fig. 1, and can be expressed as

$$I_{AA} = \frac{K}{2}n(V_C - 2V_T)^2 + \frac{1}{2K(V_C - 2V_T)^2}(I_1^2 + I_2^2 + \dots + I_n^2)$$
(5)

Furthermore, utilising the specific current mirror composed of transistors  $M_{AA}$  and  $M_{BB}$  gives  $I_{AA} = nI_{BB}$ . Therefore, the output current,  $I_O$ , can be given as

$$I_O = \sqrt{2K(V_C - 2V_T)^2} \left[ I_{BB} - \frac{K}{2} (V_C - 2V_T)^2 \right]$$
(6)

Substituting eqn. 5 into eqn. 6, the vector summation circuit becomes

$$I_O = \sqrt{\frac{1}{n}(I_1^2 + I_2^2 + \dots + I_n^2)}$$
(7)

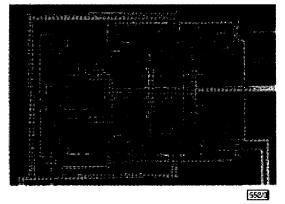


Fig. 3 Layout of two-input vector summation circuit

Simulation and experimental results: The proposed current-mode full-wave rectifier was verified with the  $0.8 \mu m$  CMOS process by HSPICE simulations. The aspect ratios (W/L) were  $5 \mu m/5 \mu m$  for all PMOS and NMOS transistors. The power supply was single

ELECTRONICS LETTERS 14th September 2000 Vol. 36 No. 19

3V and the biased voltage,  $V_C$ , was 1.5V. The simulation results show that when the input currents are set to between 1 and 12.5μA, the error is less than 0.5%. A two-input vector summation circuit was also fabricated in the same CMOS process and its die photograph is shown in Fig. 3. The aspect ratios (*W/L*) were 20μm/1µm and 5µm/5µm for the PMOS and NMOS transistors, respectively. The supply voltages were ±1.5V and the biased voltage was grounded (i.e.  $V_C = 0$ ). The input current signals were generated by AD844s [8] with 1 and 3kHz sinusoidal waves of 0.1V and two 10kΩ resistors. The transient response is shown in Fig. 4. The experimental and simulation results confirm the feasibility of the proposed circuits.

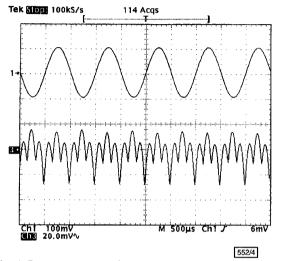


Fig. 4 Transient response of two-input vector summation circuit in Fig. 3

Upper trace: 100mV sinusoidal signal of 1kHz (100mV/div) Lower trace: output voltage (20mV/div) Horizontal scale is 500µs/div

*Conclusions:* Based on the square-law characteristics of MOS transistors, a current-mode full-wave rectifier and a current-mode vector summation circuit have been presented. The proposed two-input vector summation circuit has been fabricated in a  $0.8 \mu m$  CMOS process. The simulated and experimental results confirm the feasibility of the proposed circuits.

© IEE 2000 1 August 2000 Electronics Letters Online No: 20001180 DOI: 10.1049/el:20001180

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#### References

- PENA-FINOL, J., and CONNELLY, J.A.: 'A MOS four-quadrant analog multiplier using the quarter-square technique', *IEEE J. Solid-State Circuits*, 1987, SC-22, pp. 1064–1073
- 2 QIN, S.C., and GEIGER, R.L.: 'A ±5V CMOS analog multiplier', IEEE J. Solid-State Circuits, 1987, SC-22, pp. 1143–1146
- 3 SONG, H.J., and KIM, C.K.: 'An MOS four-quadrant analog multiplier using simple two-input squaring circuits with source followers', *IEEE J. Solid-State Circuits*, 1990, 25, pp. 841–848
- 4 LIU, S.I., and HWANG, Y.S.: 'CMOS four-quadrant multiplier using bias-offset crosscoupled pairs', *Electron. Lett.*, 1993, 29, pp. 1737-1738
- 5 LIU, S.I., and CHANG, C.C.: 'A CMOS square-law vector summation circuit', *IEEE Trans. Circuits Syst. II*, 1996, 43, pp. 520-523
- 6 CHANG, C.C., LIU, S.I., and LEE, J.L.: 'Analogue BiCMOS squarer and its application', *Electron. Lett.*, 1999, **35**, pp. 361-363
- 7 BULT, K., and WALLINGA, H.: 'A class of analog CMOS circuits based on the square-law characteristics of an MOS transistor in saturation', *IEEE J. Solid-State Circuits*, 1987, SC-22, pp. 357–365
- 8 Analog Devices, Norwood, 1992

# Diffracted Gaussian beam analysis of quasioptical multi-reflector systems

### C. Rieckmann, M.R. Rayner and C.G. Parini

A novel approach for analysing quasi-optical multi-reflector systems is described. The proposed analysis method expands an input beam into a set of elementary Gaussian beams that are propagated in a geometrical optics manner. The canonical problem of a 3D Gaussian beam incident upon a Kirchhoff halfscreen complements the reflected beam by a Gaussian beam diffracted field term. The total output field is again expanded into a Gaussian beam expansion to provide a modular technique.

Introduction: Methods for the design verification of quasi-optical (QO) systems are very limited at present. Geometrical optics (GO) does not account for the effects of edge diffraction. In most QO systems the reflectors are oversized to make diffraction negligible, but there is a demand to make QO systems more compact, in which case diffraction becomes important. The geometrical theory of diffraction (GTD) is an extension to GO that includes diffraction effects but fails at caustics. The method cannot be easily applied to multiple diffraction and caustics. Physical optics (PO) is an accurate and modular method for analysing reflector antennas but is very expensive in terms of computation time and storage for electrically large multi-reflector systems.

Gaussian beam expansion: To expand the input field on a plane in terms of elementary Gaussian beams, the so-called windowed Fourier transform is applied. This has been described for the 2D case [1], the signal being represented in a discrete two-dimensional phase-space. The transform is more general than the well-known Gabor expansion [2] and is superior in terms of stability and convergence [3]. The generalisation to three dimensions is straightforward [2]. Each of the two tangential electric field components on the input plane is represented as a linear superposition of Gaussian beam signals shifted spatially (location) and spectrally (direction). The expansion coefficients are calculated very efficiently employing the 2D FFT algorithm, and the choice of the width of each elementary beam and the corresponding beam spreading is staightforward.

*Gaussian beam reflection:* The width and radius of curvature of the elementary beams at each axial position can be described by a complex beam parameter. At the reflector the width of the beam stays the same, while the curvature changes according to the curvature of the reflector. The curvature of the beam and hence the complex beam parameter after reflection is calculated by GO.

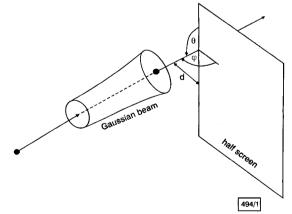


Fig. 1 Canonical problem of 3D Gaussian beam incident upon Kirchhoff half screen

*Gaussian beam diffraction:* In the GTD approach the GO reflected field is complemented by a diffracted field term, which is derived from the canonical problem of a plane wave incident upon a wedge. We take a similar approach. Diffraction of a Gaussian beam normally incident upon a Kirchhoff half-screen is investigated [4] in the forward-scattered region based on the boundary-