

An ATM Traffic Shaper for Delay-Sensitive and Delay-Insensitive VBR Services*

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Abstract

We propose an ATM traffic shaper for shaping multiple delay-sensitive and delay-insensitive VBR cell streams simultaneously, with a shaping mechanism following the definition of GCRA algorithm. By using a feedback mechanism between the regulator and the scheduler, the output streams are strictly conforming. In order to achieve best performance, we employ the Earliest-Due-Date (EDD) discipline to resolve cell emission conflicts. The call admission control condition and the cell delay bound for both classes of VBR traffic are derived. Simulation results demonstrate that the proposed traffic shaper can provide different levels of QoS (delay bound) guarantees for delay-sensitive and delay-insensitive traffic.

1. Introduction

Since the traffic management of ATM networks became an important research area, various traffic shapers or cell spacing devices have been proposed to reduce the burstiness of the VBR traffic [1, 2, 3]. The operation of a typical traffic shaper or cell spacer is to store the input cells in the buffer and then output them at eligible time or theoretical departure time. Traffic shapers can be placed in a terminal with an ATM interface card, in the network edge ATM switch or gateway, or as an independent network device. In [1, 2], traffic shapers or cell spacers are designed according to the so-called Virtual-Scheduling Algorithm (VSA) to reduce the cell delay variation (CDV) due to queueing in multiplexing nodes. In [3], Brochin employs a cell spacing device to prevent any two successive cells from being transmit-

ted within a time shorter than a variable value. In [4], traffic shapers are designed to increase the connection-carrying capacity and provide different QoS guarantees for various traffic types.

In most of these papers, the assumed models include multiple traffic streams passing through separate cell spacing devices and a second-stage multiplexer before output. Since the impact of the multiplexer on the output traffic usually is not taken into account, the output cell streams may be non-conforming due to emission conflicts within the multiplexer, regardless the fact that the cell streams observed at the output of spacing devices are conforming. In other words, such emission conflicts are likely to lead to the unnecessary peak cell rate, sustainable cell rate, or burst tolerance violation when cells are transmitted to the ATM output link. In practice, Generic Cell Rate Algorithm (GCRA) based UPC mechanism may be implemented at the other side of the User-Network Interface (UNI) or Network-Node Interface (NNI). At these UPC devices, non-conforming cells may be tagged as low priority or be discarded and lead to unnecessary cell losses. It reveals that the multiplexer should be modeled as a component of the traffic shaper such that the impact of cell output conflict can be resolved.

Only in [5], the feedback mechanism is employed between the regulator (the cell spacer) and the output scheduler (multiplexier) in the GCRA traffic shaper proposed by Li and Tsai. With such design, the output cell streams were found to be strictly conforming to the GCRA algorithm. Although in the latter approach, we have solved the cell emission conflict problem in traffic shaping, additional issues remain to be resolved. In the previous GCRA traffic shaper model [5], all VBR streams are treated only as the same class traffic, although in certain multimedia high-speed networks, different levels of QoS are designed. For example, voice and video traffic usually are more sensitive to delay or

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delay jitter when transported across the network, while data transfer should be less sensitive for network delay. Obviously, the design of traffic shaper to support multiple levels of QoS remain to be investigated.

Motivated by such challenge, we proposed a GCRA traffic shaper which can shape delay-sensitive and delay-insensitive incoming VBR traffic streams simultaneously, as shown in Fig. 1. The regulator of the shaper is responsible for determining the appropriate cell departure time for all virtual connections, while the scheduler is used to provide differentiated QoS for delay-sensitive and delay-insensitive traffic. Since the shaping delay is related to both the input and output traffic descriptors, we first derive the call admission control condition to guarantee the shaper performance and then analyze the total shaping delay bound later.

The rest of this paper is organized as follows. Section 2 defines the traffic model. Section 3 describes the design of the GCRA traffic shaper. In Section 4, the delay bound of the GCRA traffic shaper is derived. In Section 5, the proposed GCRA traffic shaper is demonstrated by numerical examples. Conclusions are finally made in Section 6.

2. The Traffic Model

The concept of traffic specification in the ATM Forum UNI Specification [6] is used to define the traffic descriptor (X, T, τ) for each virtual connection (VC). Here, X indicates the minimum cell interarrival time, which corresponds to the peak cell rate parameter if CDVT (Cell Delay Variation Tolerance) is zero, and T represents the minimum average cell interarrival time. Note that the inverse of T is equivalent to the sustainable cell rate. The burst tolerance τ is the maximal amount of time that is allowed for the actual cell arrival to be earlier than the cell arrival time theoretically predicted, under the assumption that any two consecutive cells are separated by the interval T . The latter burst tolerance parameter τ is identical to that defined in Forum's GCRA definition [6]. In other words, the traffic descriptor (X, T, τ) indicates the following traffic characteristics of a cell stream: regarding the sustainable cell rate, the cell stream conforms to GCRA (T, τ) ; when the peak cell rate is concerned, the cell interarrival time is strictly larger or equal to X , i.e., conforms to GCRA $(X, 0)$.

Hereafter, the total number of active VBR connections is assumed to be G and the number of active delay-sensitive VBR connections is assumed to be g , where $G \geq g$. The desired output traffic descriptor of VC- j is specified as (X_j, T_j, τ_j) , where VC- j is a delay-sensitive VBR connection if $1 \leq j \leq g$ and it is

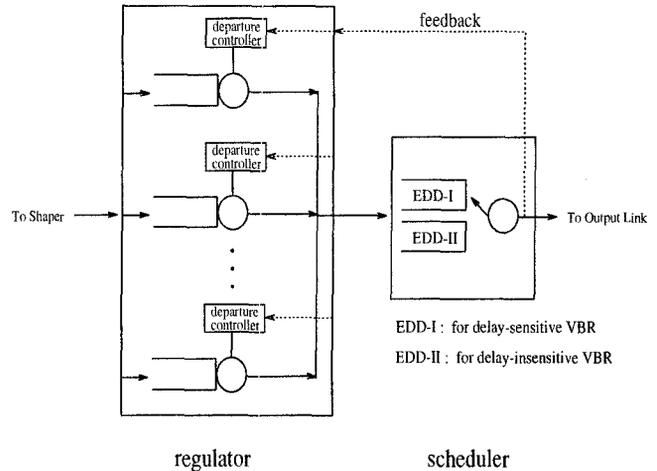


Figure 1: The model of the GCRA traffic shaper.

a delay-insensitive VBR connection if $g + 1 \leq j \leq G$.

3. The GCRA Traffic Shaper

3.1. GCRA Traffic Shaper Model

We extend the traffic shaper model in [5] to support delay-sensitive and delay-insensitive traffic, as shown in Fig. 1. The regulator consists of several departure controllers. Each departure controller regulates the peak cell rate, sustainable cell rate and burst tolerance for one VC according to its individual output traffic descriptor. The operation of the traffic shaper follows a discrete time-axis, on which the normalized cell emission time is called a time slot. If a cell arrives early, the regulator will stop it in the buffer. This cell then enters the scheduler at its eligible time. The scheduler is responsible for resolving the emission conflicts between cells from different VCs and transmits cells to the network. The scheduler consists two EDD queues, EDD-I and EDD-II. EDD-I is for delay-sensitive traffic and EDD-II is for delay-insensitive traffic. The cells in EDD-I has higher priority to be emitted than the cells in EDD-II. While a cell reaches the HOL (Head of Line) position in the EDD queues, it can be transmitted at the beginning of the next slot at the earliest. Hence, the minimum sojourn time at the scheduler for any cell is one slot. In order to prevent the cell emissions from violating the output traffic descriptor, there exists a feedback signal from the scheduler to the GCRA mechanism within the regulator. This assures that the calculation of the eligible time of the next cell emission of the same VC is always done after the receipt of the feedback signal triggered by the current emission. Therefore, there can be at most one cell in the sched-

uler for each VC at any time. The buffer size in the scheduler is thus determined by the maximal number of VCs that the GCRA traffic shaper is designed to support.

3.2. Algorithm of in the Regulator

In order to describe the shaping algorithm in the regulator in detail, some control variables for shaped connections are defined as follows. For VC- j , the k -th cell arrives at the shaper (or regulator) at time $A_j(k)$ and is buffered until the Eligible Time $ET_j(k)$ before it enters the scheduler. It is then given an Initial Due-Date $IDD_j(k)$ when it enters the scheduler. The target time for this cell to leave the scheduler is called the Theoretical Departure Time $TDT_j(k)$. However, the time epoch when it leaves the scheduler could be different. We call such time epoch the Actual Departure Time, and denote it as $ADT_j(k)$. Note that the variables $A_j(k)$, $ET_j(k)$, and $ADT_j(k)$ are integers, while $TDT_j(k)$ and $IDD_j(k)$ may be not. During the operation of the traffic shaper, these variables are calculated by the following iterative forms.

$$TDT_j(k) = \max\{ADT_j(k-1), TDT_j(k-1)\} + T_j, \quad (1)$$

$$ET_j(k) = \max\{ADT_j(k-1) + \lceil X_j \rceil - 1, [TDT_j(k) - \tau_j] - 1, A_j(k)\}, \quad (2)$$

$$IDD_j(k) = \max\{TDT_j(k) - ET_j(k), \delta_j\}, \quad (3)$$

with initial values $TDT_j(1) = A_j(1)$, $ET_j(1) = A_j(1)$, and $IDD_j(1) = \delta_j$, where δ_j is the minimal initial due-date, given by $\delta_j = \min\{T_j - \lceil X_j \rceil + 1, \tau_j\}$.

Consider a specific connection, say VC- j . When the k -th cell arrives at the regulator, $TDT_j(k)$ is not determined until the feedback signal triggered by the departure of the $(k-1)$ -th cell is received. $TDT_j(k)$ is then set to $\max\{ADT_j(k-1), TDT_j(k-1)\} + T_j$ so that it meets the output sustainable cell rate constraint of VBR- j . In order to guarantee that the output cell stream will conform to (X_j, T_j, τ_j) , the k -th cell can not enter the scheduler earlier than either the time epoch $ADT_j(k-1) + \lceil X_j \rceil - 1$ or $[TDT_j(k) - \tau_j] - 1$; otherwise, it might violate the peak cell rate constraint or the burst tolerance constraint, respectively. By taking account of the fact that a cell can never enter the scheduler before it arrives at the regulator, Eligible Time can be expressed as equation (2). Under ideal operation conditions, the maximal throughput of all connections should be maintained with the use of the traffic shaper. This requires that no cell losses occur in the scheduler and all cells are emitted before their Theoretical Departure Times. The first requirement can be easily met by allocating M buffers for cells at the scheduler, where M is the maximal number of connections that the shaper supports. To satisfy the second

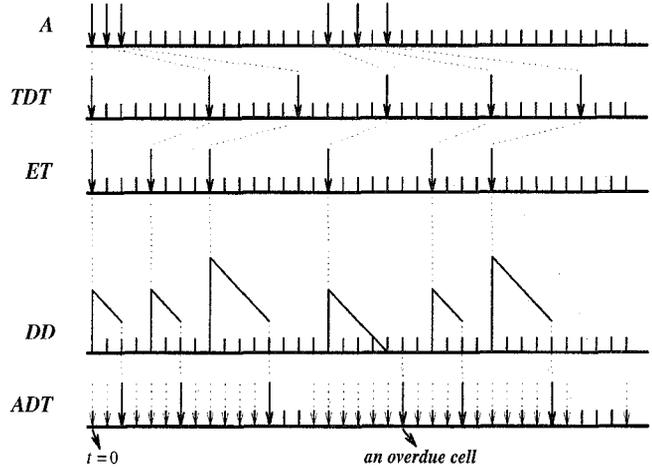


Figure 2: Sample-path of a specific VC with traffic descriptor $(X, T, \tau) = (3, 6, 9)$. The dotted arrows in ADT pattern represent the cell emissions of other VCs.

requirement, appropriate Initial Due-Dates must be assigned. The difference between $TDT_j(k)$ and $ET_j(k)$ is used as the preliminary initial due-date whenever the shaper is nonempty with respect to VBR- j . From (1) and (2), it can be shown that $TDT_j(k) - ET_j(k)$ is never smaller than δ_j unless $ET_j(k) = A_j(k)$. The final initial due-date, as given by equation (3), is set to be the maximum of the preliminary initial due-date $TDT_j(k) - ET_j(k)$ and the minimal initial due-date δ_j . The latter δ_j is used to fairly resolve cell emission conflicts, reduce scheduling delay bounds, and to improve the shaper utilization under the CAC mechanism. We set $\delta_j = \min\{T_j - \lceil X_j \rceil + 1, \tau_j\}$ so that overdue events for other VBR connections caused by immediate emission of cells with $ET_j(k) = A_j(k)$ can be minimized. From (1) to (3), it can be shown that $IDD_j(k)$ satisfies $\tau_j + 1 \geq IDD_j(k) \geq \delta_j$.

3.3. Algorithm in the Scheduler

After the k -th cell of VC- j enters the buffer of the scheduler, its instantaneous due-date at time t , denoted as $DD_j(k, t)$, is defined to be as follows.

$$DD_j(k, ET_j(k)) = IDD_j(k) \quad (4)$$

$$DD_j(k, t+1) = \max\{DD_j(k, t) - 1, 0\}. \quad (5)$$

for $t \geq ET_j(k)$.

In the scheduler, the Earliest-Due-Date (EDD) service discipline is employed to minimize the number of overdue events. (Please refer to [7, 8] for similar designs and [9, 10] for detailed proof of its optimality.) Under the EDD discipline, the cell with the smallest

due-date in the scheduler is emitted first. If multiple cells have equal due-date, they are emitted in FIFO order. In this paper, we say that a cell is *overdue* if its due-date is zero and still resides at the scheduler. Fig. 2 shows one sample-path of the control variables associated with a specific connection, say VC- j , with the output traffic descriptor (3, 6, 9).

4. Performance Analysis

In this section, the delay performance and the call admission control condition for both classes of VBR traffic are derived.

Theorem 1 : Consider a target cell from VC- j , with initial due-date y . Then the delay bound, $d_j(y)$, of the target cell in the scheduler is given as follows.

$$d_j(y) = \max_{\Delta \geq 0} \left\{ N_j(\Delta) + \sum_{i=1, i \neq j}^g N_i(y + \Delta - \delta_i) - \Delta \right\} \quad (6)$$

for delay-sensitive VC, where $1 \leq j \leq g$, and

$$d_j(y) = \max_{\Delta \geq 0} \left\{ \min \left\{ u \mid N_j(\Delta) + \sum_{i=g+1, i \neq j}^G N_i(y + \Delta - \delta_i) + \sum_{i=1}^g N_i(u + \Delta) \leq u + \Delta \right\} \right\} \quad (7)$$

for delay-insensitive VC, where $g+1 \leq j \leq G$, and $N_i(t) = \min\{[1 + \frac{t}{X_i}], [1 + \frac{t+\tau_i}{T_i}]\}$, for $t \geq 0$; $N_i(t) = 0$, otherwise.

Proof : The scheduling delay bound for delay-sensitive VC ($1 \leq j \leq g$) can be directly derived as in [5]. In the following, we only show the scheduling delay bound for delay-insensitive VC ($g+1 \leq j \leq G$). Consider the target cell from VC- j ($g+1 \leq j \leq G$) which enters the scheduler with initial due-date y at time t and departs the scheduler at time $t+u$. Assume the busy period that contains time t started at earlier time ($t-\Delta$). Since delay-sensitive traffic has priority over delay-insensitive traffic, those cells belonging to VC- i , where $1 \leq i \leq g$, enter the scheduler during the interval $[t-\Delta, t+u)$ can be emitted before the target cell. Hence, the number of delay-sensitive cells which can contribute to the scheduling delay of the target cell is bounded by $\sum_{i=1}^g N_i(u + \Delta)$. Furthermore, since the EDD service discipline is employed in the scheduler, the last cell from VC- i ($g+1 \leq i \leq G$, and $i \neq j$) that can delay the target cell must have arrived before time $(t+y-s)$, where s ($s \geq \delta_i$) is the initial due-date of this cell. Hence, between time $(t-\Delta)$ and time $(t+y-s)$ the number of delay-insensitive cells that do not belong to VC- j and will be emitted before the target cell is bounded by

$$\sum_{i=g+1, i \neq j}^G N_i(y + \Delta - s) \leq \sum_{i=g+1, i \neq j}^G N_i(y + \Delta - \delta_i).$$

Moreover, the number of cells which belong to VC- j and enter the scheduler during $[t-\Delta, t]$ is bounded by $N_j(\Delta)$. Since the cells which enter the scheduler during $[t-\Delta, t+u)$ and can be emitted before the target cell all contribute to the busy period $[t-\Delta, t+u)$. The delay of the target cell should not be larger than the minimum u that satisfy

$$N_j(\Delta) + \sum_{i=g+1, i \neq j}^G N_i(y + \Delta - \delta_i) + \sum_{i=1}^g N_i(u + \Delta) \leq u + \Delta.$$

Therefore, we have the delay bound equation (7). \square

The following theorem provides the sufficient condition to avoid cell overdue for both classes of VBR streams. One should note that if a cell is overdue, then its *ADT* is larger than its *TDT*. However, *ADT* > *TDT* does not always imply an overdue event.

Theorem 2 : If $d_j(\delta_j) \leq \delta_j$, then no cell of VC- j will be overdue.

Proof : Consider an arbitrary cell from VC- j and let its initial due-date be y . If $d_j(y) \leq y$, for all $y \geq \delta_j$, this cell shall not experience overdue events. The condition for $1 \leq j \leq g$ is the same as Theorem 2 of [5], since the existence of low priority VBR cells do not affect the behavior of high priority VBR cells. To show the sufficient condition for $g+1 \leq j \leq G$, by equation (7) one can express $d_j(y) - y$ as

$$\begin{aligned} d_j(y) - y &= \max_{\Delta \geq 0} \left\{ \min \left\{ u - y \mid N_j(\Delta) + \sum_{i=g+1, i \neq j}^G N_i(y + \Delta - \delta_i) + \sum_{i=1}^g N_i(u + \Delta) \leq u + \Delta \right\} \right\} \\ &= \max_{\Delta \geq y - \delta_j} \left\{ \min \left\{ u - \delta_j \mid \sum_{i=g+1, i \neq j}^G N_i(\delta_j + \Delta - \delta_i) + N_j(\Delta - y + \delta_j) + \sum_{i=1}^g N_i(u + \Delta) \leq u + \Delta \right\} \right\}. \end{aligned}$$

For $y \geq \delta_j$, one can write

$$\begin{aligned} d_j(y) - y &\leq \max_{\Delta \geq 0} \left\{ \min \left\{ u - \delta_j \mid N_j(\Delta) + \sum_{i=g+1, i \neq j}^G N_i(\delta_j + \Delta - \delta_i) + \sum_{i=1}^g N_i(u + \Delta) \leq u + \Delta \right\} \right\} \\ &= d_j(\delta_j) - \delta_j. \end{aligned}$$

Thus, $d_j(y) \leq y$ for all $y \geq \delta_j$ is implied by $d_j(\delta_j) \leq \delta_j$. We then conclude $d_j(\delta_j) \leq \delta_j$ implies no cell overdue for VC- j . \square

Two possible call admission control procedures can be employed. When we guarantee the delay bound of delay-sensitive VBR and impose call admission control to delay-sensitive traffic only, we call the CAC policy the **Policy 1**. Meanwhile, when both delay-sensitive and delay-insensitive require delay bounds but of different values, the CAC mechanism must be applied to both classes and the corresponding policy is called the **Policy 2**. The detailed CAC procedures are as follows.

Policy 1 : When a new delay-sensitive VC, say VC- n , requests to be supported by the shaper, $d_j(\delta_j)$ is computed for all existing delay-sensitive VCs and VC- n using (6). If all $d_j(\delta_j) \leq \delta_j$ are satisfied for delay-sensitive VCs, the new request is granted. Otherwise, it is rejected. When a new delay-insensitive VC request arrives, it is always admitted unless the traffic is overloaded.

Policy 2 : When a new VC (delay-sensitive or delay-insensitive), say VC- n , requests to be supported by the shaper, $d_j(\delta_j)$ is computed for all existing VCs and VC- n using (6) if the VC is delay-sensitive and (7) otherwise. If all $d_j(\delta_j) \leq \delta_j$ are satisfied for all VCs, the new request is granted. Otherwise, it is rejected.

Although the traffic condition is different from that in [5]. We found the same total delay bound can be employed for both classes of VBR. The proof of the following theorem is thus omitted.

Theorem 3 : Assume the output and input traffic descriptors of VC- j are given by (X_j, T_j, τ_j) and (X'_j, T'_j, τ'_j) , where $T_j \leq T'_j$. If no overdue for VC- j is guaranteed, the cell delay of VC- j within the whole GCRA traffic shaper is bounded by D_j which satisfies

$$D_j \leq \delta_j + \lfloor \frac{\tau'_j}{T'_j - X'_j} \rfloor (T_j - X'_j). \quad (8)$$

If $T_j = T'_j$, then

$$D_j \leq \delta_j + \tau'_j. \quad (9)$$

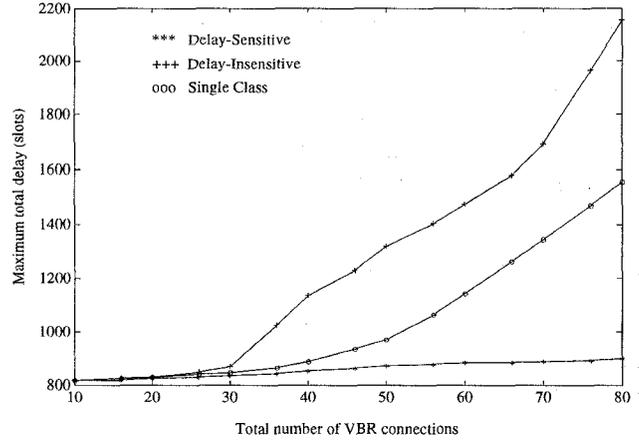


Figure 3: The maximum delay versus the number of all VBR connections. $(X'_i, T'_i, \tau'_i) = (3, 86.2323, 1600)$, $(X_i, T_i, \tau_i) = (20, 86.2323, 800)$, and $r = 0.99$.

5. Numerical Results

Here, we use several examples to illustrate the advantages of the proposed GCRA traffic shaper when delay-sensitive and delay-insensitive VBR traffic are both supported. The ATM link data rate is set to be 149.76 Mbps. During simulation, input cell streams to the regulator are generated by the following rule. The k -th cell arrival is first generated by a pseudo-arrival time $TAT(k) - x$, where $x = \tau'$ (the input jitter or burst tolerance parameter) with probability r and $x = 0$ with probability $1 - r$. The recurrence equation $TAT(k) = TAT(k - 1) + T'$ determines the k -th theoretical arrival time for $k \geq 1$, while $TAT(0)$ can be arbitrarily set. During simulation, the actual cell arrival time, $A(k)$, is determined by

$$A(k) = \max\{[TAT(k) - x], A(k - 1) + [X']\}.$$

Note that $A(k)$ is always an integer. One can observe that the generated input arrival cell stream conforms to the traffic descriptor (X', T', τ') .

In the following examples, multiple homogeneous VBR connections are supported. The input traffic descriptor of each VC is set to be $(X'_i, T'_i, \tau'_i) = (3, 86.2323, 1600)$. Note that the sustainable cell rate of each VC is equivalent to the data rate of a DS1. In the first example, the output traffic descriptor of each VC is set to be $(X_i, T_i, \tau_i) = (20, 86.2323, 800)$. The number of delay-sensitive VCs equals that of delay-insensitive VCs, i.e., $G = 2g$. Fig. 3 shows the curves of the maximum delay versus the number of all connections. One can observe that the maximum delay

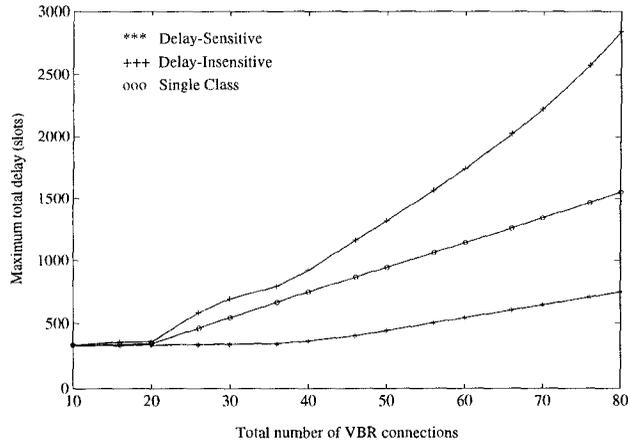


Figure 4: The maximum delay versus the number of all VBR connections. $(X'_i, T'_i, \tau'_i) = (3, 86.2323, 1600)$, $(X_i, T_i, \tau_i) = (20, 86.2323, 1600)$, and $r = 0.99$.

of delay-sensitive VCs is reduced significantly under our proposed shaper model (delay-sensitive VBR traffic has priority over delay-insensitive VBR traffic). The second example employed a different output traffic descriptor $(X_i, T_i, \tau_i) = (20, 86.2323, 1600)$. The maximum delay versus the number of all VCs is illustrated in Fig. 4. Comparing Fig. 3 with Fig. 4, one can conclude that larger burst tolerance leads to smaller shaping delay. This result indicates that the shaping delay of delay-sensitive VBR traffic can be reduced by assigning it higher priority. Last but not least, the traffic descriptor of a VBR stream also affects its shaping delay significantly. If the shaping delay is exceedingly long due to the difference between the input and output traffic descriptors of a delay-sensitive VBR, the priority mechanism does not help to reduce the shaping delay. Only by adjusting the output traffic descriptor or reducing the gap of input and output traffic descriptors can one reduce the shaping delay to an acceptable level.

6. Conclusions

In this paper, a GCRA traffic shaper has been presented and analyzed for supporting delay-sensitive and delay-insensitive ATM traffic. The two main design features have been found to be effective. First, by assigning delay-sensitive VBR traffic higher priority than delay-insensitive VBR traffic in the scheduler, total delay of the former is significantly reduced. Secondly, by using a feedback signal between the regulator and the

scheduler, not only it can guarantee the output cell streams to conform to the output traffic descriptor, call admission control can be derived for QoS guarantee. Numerical examples have also validated the performance improvement than previous design. With such merit shown in this paper, we believe this shaper design should be strongly desirable in support of future QoS-oriented high speed network evolution.

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