A 1-4 GHz DLL Based Low-Jitter Multi-Phase Clock Generator for Low-Band Ultra-Wideband Application

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ABSTRACT

This paper presents the implementation of a low-jitter system clock generator for low-band ultra-wideband (UWB) application based on a wide-range adaptive-bandwidth delay-locked loop (DLL). The false-locking problem commonly along with the wide-range DLL is eliminated by the proposed digital self-correcting loop which also speeds up the lock-in time of the DLL. With self-biased techniques, the proposed DLL adaptively adjusts bandwidth and exhibits optimal jitter transfer characteristic over a wide frequency range and across process, voltage, and temperature (PVT) variations. Fabricated in a 0.18-μm CMOS technology, the design achieves an output multi-phase sampling clock rate of 1 to 4 GHz and exhibits the maximum input tracking jitter of 12.06 ps (rms) and 88.9 ps (pk-pk) over the operating frequency range from 31.25 to 125 MHz. The prototype occupies an active area of 360 × 245 μm^2 and consumes 32 mW from a 1.8-V supply at 125 MHz.

I. INTRODUCTION

The Federal Communications Commission (FCC) has opened the frequency bands for unlicensed ultra-wideband (UWB) wireless systems since February, 2002 [1]. System architectures for pulse-based UWB radio have been recently proposed targeting applications such as positioning system and sensor network. One critical aspect of VLSI implementation of pulse-based UWB radio is the accurate generation of timing signals to support reliable data communications [2].

Phase-locked loops (PLLs) and delay-locked loops (DLLs) have been typically employed to generate high-frequency accurate system clock from a low-frequency, precise, and stable oscillator. Usually, DLLs are easier than PLLs to implement the clock generator. A DLL is unconditionally stable and only needs one capacitor in its first-order loop filter, while a PLL generally requires a higher order filter which usually occupies large areas or needs to be off chip in order to guarantee the stability and performance. Moreover, a DLL offers better jitter performance than a PLL because phase errors induced by supply or substrate noises do not accumulate over many cycles in the voltage-controlled delay line (VCDL) [3]. However, conventional DLLs may suffer from false locking, which is undesirable if multi-phase clocks are needed. The maximum and the minimum delays of the VCDL, $T_{\mathrm{VCDL\cdot max}}$ and $T_{\mathrm{VCDL\cdot min}}$, should satisfy the following inequalities to avoid a false locking [4]:

$$
\begin{aligned}
0.5 \times T_{\mathrm{CLK}} &< T_{\mathrm{VCDL\cdot min}} < T_{\mathrm{CLK}} \\
T_{\mathrm{CLK}} &< T_{\mathrm{VCDL\cdot max}} < 1.5 \times T_{\mathrm{CLK}}
\end{aligned} \qquad (1)
$$

or, equivalently, in terms of T_{CLK}:

$$
\begin{aligned}
\mathrm{Max}\,(\,T_{\mathrm{VCDL\cdot min}},\ 2/3 \times T_{\mathrm{VCDL\cdot max}}\,) &< T_{\mathrm{CLK}} \\
&< \mathrm{Min}\,(\,2 \times T_{\mathrm{VCDL\cdot min}},\ T_{\mathrm{VCDL\cdot max}}\,)
\end{aligned} \qquad (2)
$$

where T_{CLK} is the period of the input reference clock. If the target clock period satisfies the inequality (2), the DLL works and does not posses a false-locking. However, if $T_{\mathrm{VCDL\cdot max}} \geq 3 \times T_{\mathrm{VCDL\cdot min}}$, which is usually the case when process, voltage, and temperature (PVT) variations are taken into consideration, then there is no range of T_{CLK} that satisfies the inequality (2). Therefore, the conventional DLL can only operate over a narrow frequency range if an exotic tedious trimming circuit for correct locking is not employed [4].

This paper proposes a novel DLL architecture without the false-locking problem, which combines two techniques [5], [6] for implementation of a low-jitter wide-range multi-phase clock generator. The output sampling clock rate of the proposed DLL spans from 1 GHz to 4 GHz, which is sufficient for low-band 960 MHz UWB system application [2].

The rest of this paper is organized as follows. Section II describes the proposed DLL architecture followed by the circuit design in Section III. Experiment results are presented in Section IV. Section V concludes this paper.

II. DLL ARCHITECTURE

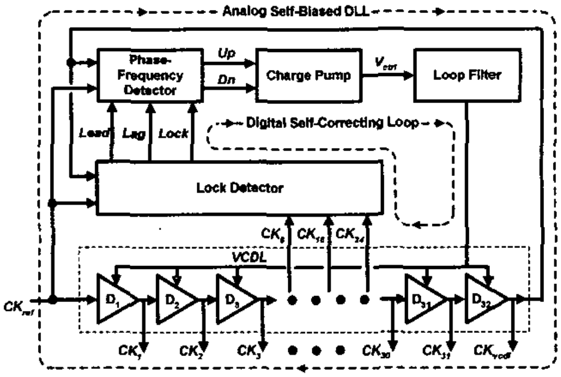

Fig. 1 Block diagram of the proposed DLL architecture.

Fig. 1 shows the architecture of the proposed low-jitter wide-range adaptive bandwidth DLL, which consists of a main *analog self-biased DLL* and an auxiliary *digital self-correcting loop.* The phase-frequency detector (PFD), charge pump, loop filter, and 32-stage VCDL compose the DLL core. The self-biased circuits adjust the DLL loop bandwidth adaptively. Therefore,

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the loop stability and an optimal jitter transfer characteristic can be maintained over a wide frequency range and across PVT variations [6]. The auxiliary digital self-correcting loop consists of the same components of the DLL core except employing a lock detector to replace the PFD. It continuously monitors the DLL acquisition behavior and takes control of the loop if the phenomenon of false locking is detected. The lock detector utilizes three additional delayed clocks, CK_8, CK_{16}, and CK_{24} from VCDL to determine the preset lock-in state. It then generates three digital control signals, namely, *Lead*, *Lag*, and *Lock*. These digital control signals indicate whether the DLL is in false-locking state. That is, when the delay of the VCDL is too small, the *Lead* control signal is activated. The *Lag* control signal is activated to indicate the delay is too large. The lock detector can take over the loop from PFD and directly sense the charge pump to charge or discharge the loop through the *Lead* and the *Lag* control signals. On the other hand, if the delay of the VCDL is within the correct-locking range, the *Lock* control signal is activated and the DLL core restarts to acquire locking as usual. The auxiliary digital self-correcting loop extends correct-locking range of the DLL four times wider than that of the conventional design constrained by the inequality (1).

The critical path timing contributed by gate delays of the digital decision logics in the auxiliary digital self-correcting loop may be so large in high-speed operation that the switching from the auxiliary digital self-correcting loop to the DLL core cannot be accomplished in time. This might result in instability of the loop. The PFD is adopted to effectively increase switching timing margin and mitigate the problem of loop instability because it has a wider capture range of (-2π,$+2\pi$) than the phase detector (PD) used in the previous architecture [5].

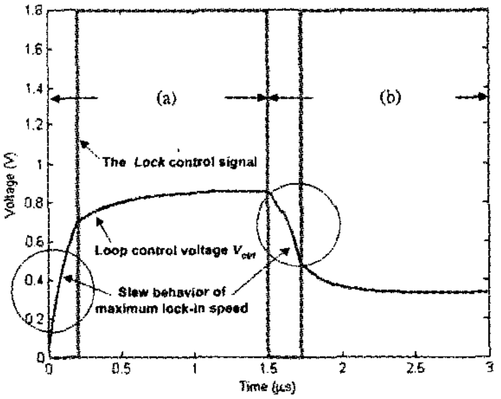


Fig. 2 Simulated loop acquisition behavior of the DLL (a) at 40 MHz and (b) at input clock frequency changed to 100 MHz after 1.5 μs.

Fig. 2 shows the simulated loop control voltage V_{ctrl} and the *Lock* control signal when the DLL starts to acquire locking. In Fig. 2(a), the DLL starts at an input clock frequency 40MHz and the minimum VCDL delay. Once the lock detector detects the DLL core in false-locking state, it immediately disables the *Lock* control signal. Although the DLL core suffers from false locking, the loop can still lock to the right direction and exhibit slew behavior of maximum speed because of the operation of the auxiliary digital self-correcting loop. The *Lock* control signal is activated and the DLL core then regains control of the loop until the delay of the VCDL is within the correct-locking range. When the input clock frequency is suddenly changed to 100 MHz after 1.5 μs, where the conventional DLLs would suffer false-locking problem, the proposed DLL can still react and operate properly, as shown in Fig. 2(b).

III. Circuit Design

A. Lock Detector

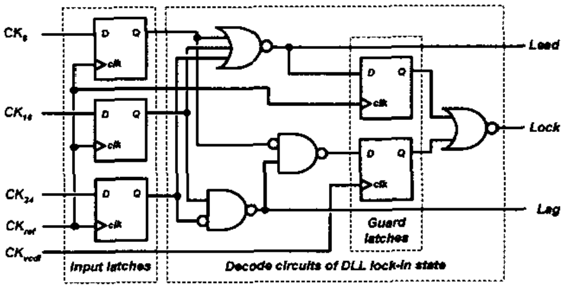


Fig. 3 Schematic of the proposed lock detector.

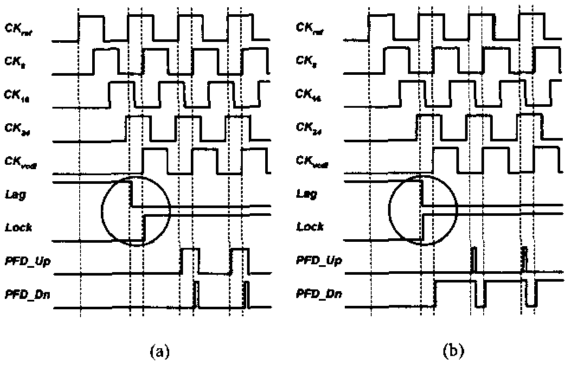


Fig. 4 Timing diagram of the DLL (a) with and (b) without guard latches included in the lock detector.

The schematic of the lock detector is shown in Fig. 3. The three delayed clocks from the VCDL, CK_8, CK_{16}, and CK_{24} are first latched at the rising edge of the input reference clock CK_{ref}. The outputs of these latches are further processed to determine the present lock-in state by decode circuits. Two guard latches, which are trigged respectively by CK_{ref} and the delayed clock from the last stage of the VCDL, CK_{vcdl}, are included in the decode circuits generating *Lock* control signal. Fig. 4 shows the detailed timing diagram of the DLL when the lock-in state of the DLL is changed from the *Lag* state to the *Lock* state. It illustrates the functions of the guard latches. The guard latches ensure the *Lock* control signal can be activated at the right moment so that the PFD can generate proper control signals to keep the DLL core locking to the correct direction when it regains control of the loop from the reset state.

B. Dynamic-Switched Phase-Frequency Detector

Fig. 5 shows the dynamic-switched PFD circuit, which consists of a dynamic logic PFD and digital control logics for lock detector. The *Lead* and *Lag* control signals can bypass the dynamic logic PFD to directly control the following charge-pump stage through these digital control logics. The logics included in the reset path properly reset the PFD when the *Lock* control signal is disabled. The extra gate delays in the reset path also help the PFD periodically produce a chain of short pulses in the locked state which can reduce the dead zone of the PFD effectively. The dynamic logic PFD is adopted here for the capability of higher speed operation in comparison with the static counterpart.

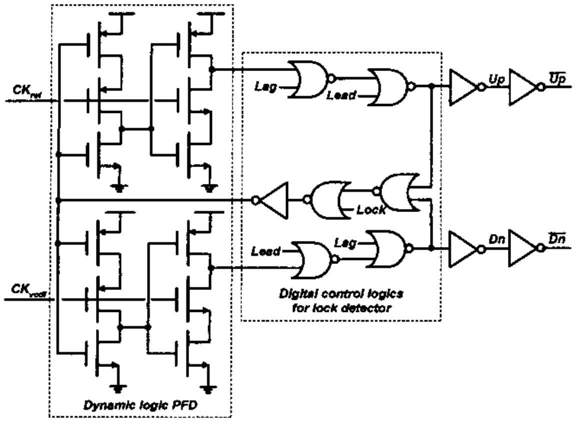
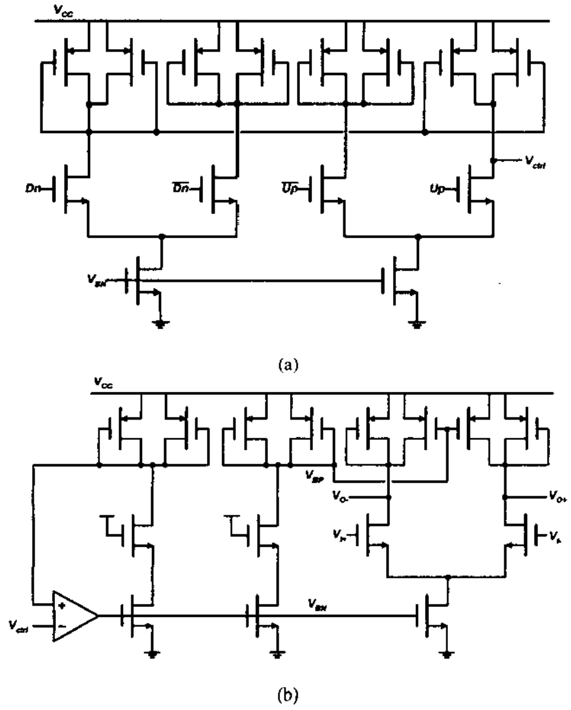


Fig. 5 Schematic of the dynamic-switched PFD circuit

C. Charge Pump and Voltage-Controlled Delay Line



(a)

(b)

Fig. 6 (a) Charge pump (b) delay cell of the VCDL with replica bias [6].

The charge-pump circuit and the delay cell of the VCDL with replica bias are similar to those used in [6], as shown in Fig. 6. These circuits are biased with the VCDL control voltage, and their currents can be scaled with the operating frequency of the DLL consequently.

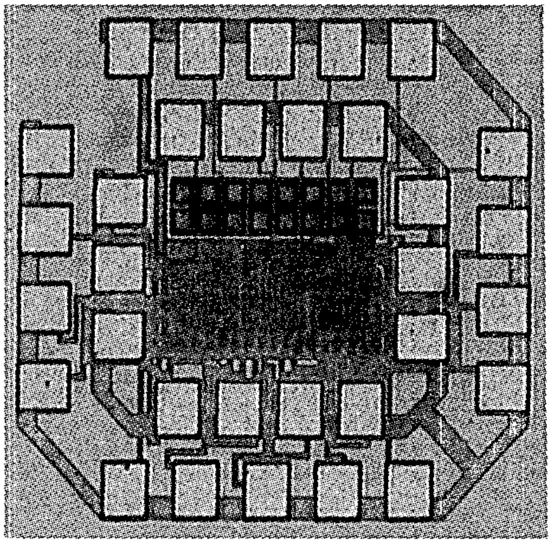


Fig. 7 Die photo of the DLL.

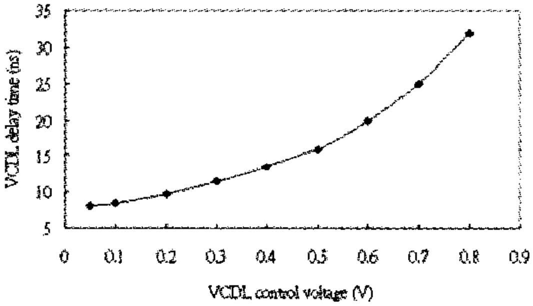
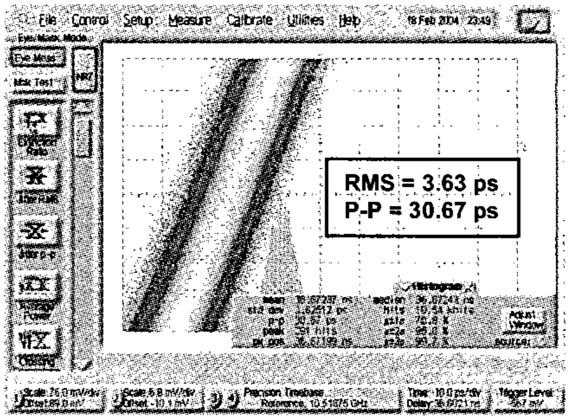


Fig. 8 Measured transfer curve of the VCDL.



RMS = 3.63 ps
P-P = 30.67 ps

Fig. 9 DLL output jitter histogram at 125 MHz.

IV. Experimental Results

The DLL has been designed and fabricated in a 0.18-μm CMOS technology. As shown in the die photo in Fig. 7, the DLL core area is 0.09 mm^2 (360 μm × 245 μm). The experimental results show that the DLL can operate in the frequency range of 31.25 to 125MHz with a 1.8-V supply. Fig. 8 depicts the measured transfer curve of the VCDL. The tracking jitter performance of the DLL output at 125MHz is demonstrated in Fig. 9. The jitter histogram measures 3.63-ps rms and 30.67-ps peak-to-peak jitter characteristics in a quiet supply. Fig. 10 shows the measured rms jitter characteristics of the DLL over different operating frequencies. If a 100 mV Gaussian random noise is injected externally to the supply, the rms jitter and peak-to-peak jitter are increased to 12.23 ps and 90.7 ps respectively when the DLL operates at 125MHz, as demonstrated in Fig. 11. The equivalent jitter supply sensitivity is less than 0.91 ps/mV. Table I summarizes the performance of the proposed DLL.

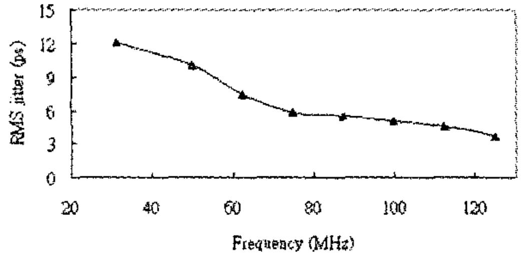
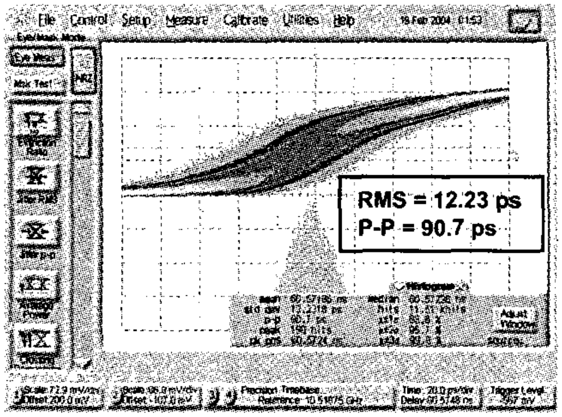


Fig. 10 Measured rms jitter characteristics of the DLL over different operating frequencies.



RMS = 12.23 ps
P-P = 90.7 ps

Fig. 11 DLL output jitter histogram at 125 MHz with 100 mV supply noise injected to the supply.

TABLE I
Performance summary of the proposed DLL

Process	0.18-μm 1P6M TSMC CMOS process
Operating voltage	1.8V
Operating frequency range	31.25 MHz ~ 125 MHz
Output multi-phase clock rate	1 GHz ~ 4 GHz
RMS jitter	12.06 ps @ 31.25 MHz 3.63 ps @ 125 MHz
Peak-to-peak jitter	88.9 ps @ 31.25 MHz 30.67 ps @ 125 MHz
Supply sensitivity	< 0.91 ps/mV
Lock time	~ 54 clock cycles (simulated)
Power dissipation	32 mW @ 125 MHz
Active area	0.09 mm^2

V. Conclusion

A self-biased adaptive bandwidth DLL using an auxiliary digital self-correcting loop is proposed to achieve an optimal jitter transfer characteristic and avoid false-locking problem over a wide frequency range and across PVT variations. Compared with previous wide-range DLLs [4]-[8], the proposed DLL demonstrates smaller area cost, lower power consumption, and better jitter performance. The equivalent sampling clock rate of multi-phase clocks generated from 32 taps of the VCDL can operate up to 4 GHz, which makes this DLL suitable for low-jitter clock generation in low-band UWB application.

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