Improvement in Radiation-Hard CMOS Logic Gates for Noise Margin

S-J Yih, M-L Chang, J-G Hwu, and W-S Feng
Room 244, Department of Electrical Engineering,
National Taiwan University,
Taipei, Taiwan, R. O. C. China

Abstract

A design technique for fundamental CMOS logic gates that are almost insensitive to noise margin is proposed. An auxiliary circuit is added to the conventional CMOS logic gates. All the circuits are simulated by HSPICE. It is observed from simulation results that good radiation hard behavior appears in the improved inverter, NOR and NAND gates for noise margin, especially for the scaling down on supply voltage V_{DD}.

1 Introduction

The performance of MOS circuits in the nuclear and space environments may be degraded due to irradiation [1]. Some approaches have been proposed to improve the radiation hardness in MOS circuits. Generally, the improvement can be obtained either by processing during device fabrication [2], or by circuit design [3], [4]. The circuit design is considered based on normal process technology, and one may use a compensation circuit to achieve the radiation-hardness [4]. The extra circuit is not a burden to the VLSI technology.

Generally, a negative threshold voltage shift was observed for MOSFETs after irradiation. In this work, a negative threshold voltage shift for MOSFETs after irradiation is considered. For an NMOSFET with a positive initial threshold voltage V_{tn} and a PMOSFET with a negative initial threshold voltage V_{tp}, radiation results in the decrease of $|V_{tn}|$ and the increase of $|V_{tp}|$. $\triangle V_{tn}$ is generally much greater than $\triangle V_{tp}$ in normal operating conditions [5]. It is noted that the I-V characteristics of a MOSFET after radiation exposure will change significantly due to V_t shift [5]. In other words, when we investigate the improvement in radiation hardness of MOS circuits using circuit design techniques, we need to consider V_t as the only major controllable variable.

2 Design of Radiation Hard Circuits

CMOS combinational circuits may be constructed by inverters, NOR gates and NAND gates. It is necessary to make these gates radiation hard.

2.1 Inverter

The general noise margins of a CMOS inverter can be found from its voltage transfer characteristic [6]. They are

$$\begin{aligned} NM_L^0 &= V_{IL} - V_{OL} \\ &= \frac{3V_{DD} - 3|V_{tp}^0| + 5V_{tn}^0}{8} \end{aligned} \quad (1)$$

and

$$\begin{aligned} NM_H^0 &= V_{OH} - V_{IH} \\ &= V_{DD} - V_{IH} \\ &= \frac{3V_{DD} + 5|V_{tp}^0| - 3V_{tn}^0}{8} \end{aligned} \quad (2)$$

where NM_L^0 and NM_H^0 are the noise margins of input at 0 state and at 1 state, respectively, before irradiation. V_{IL} and V_{IH} are the highest and lowest input voltages reliably recognized as logic low and high, respectively. V_{OL} and V_{OH} are the nominal logic low and high voltages generated by output stages, respectively. The input noise margins at 0 state and at 1 state after radiation exposure, i.e., NM_L' and NM_H', respectively, can be written as

$$NM_L' = NM_L^0 - \frac{3|\triangle V_{tp}| + 5|\triangle V_{tn}|}{8} \quad (3)$$

0-7803-3583-X/97 $10.00 ©1997 IEEE

and

$$NM'_H = NM^0_H + \frac{5|\triangle V_{tp}| + 3|\triangle V_{tn}|}{8} \quad (4)$$

where $\triangle V_{tn}$ and $\triangle V_{tp}$ are the threshold voltage shifts of NMOS and PMOS, respectively, due to irradiation [4]. Generally, $|\triangle V_{tn}|$ is larger than $|\triangle V_{tp}|$ [5], so we consider the case of $|\triangle V_{tn}|$ =2 $|\triangle V_{tp}|$ = 2$|\triangle V_t|$ [4]. Eqs. (3) and (4) can be written as follows:

$$NM'_L = NM^0_L - \frac{13}{16}|\triangle V_{tn}| \quad (5)$$

$$NM'_H = NM^0_H + \frac{11}{16}|\triangle V_{tn}| \quad (6)$$

From Eqs. (5) and (6), it is obvious that the noise margin of 0 state will become smaller and that of 1 state will become larger after irradiation. For example, with the SGS 4007 circuit under bias, total doses of 1, 5, and 10 Krads produce $\triangle V_{tn}$ values of 0.2, 0.8, and 1.5 Volts, respectively [5]. Generally, the noise margin of 0 state has been decreased to an unbearable value but that of 1 state has become better. Hence, our work is aimed at using some compensation circuit to make NM'_L to be as little correlated to $\triangle V_{tn}$ as possible.

An improved CMOS inverter with four additional NMOSFET's, i.e., N2, N3, N4, N5, is shown in Fig. 1. N1 and P1 form the original CMOS inverter with the source of NMOS not connecting to ground but to the drain of N4. The source voltage of N1 is V_x. Since what we want to do is improve NM'_L, we just consider the case that V_{out} varies from 1 state to 0 state, i.e., V_{in} varies from 0 state to 1 state.

Let V'_{tn} be the threshold voltage of the NMOSFET's after irradiation.

(A) $V'_{tn} < V_{in} < V'_{tn}$ + Vx:

N3 and N4 are in the saturation region. The equation describing the behavior of an MOSFET device in saturation region is:

$$I_{ds} = \beta(V_{gs} - V_t)^2. \quad (7)$$

β_3 and β_4 are the MOS transistor gain factors of N3 and N4, respectively. Let K = β_3 / β_4 = 1, we can get the following results from eq. (7).

$$\triangle V_{tn} < Vx < 2\triangle V_{tn}.$$

The voltage Vx decreases from 2 $\triangle V_{tn}$ to $\triangle V_{tn}$.

(B) $V_{in} = V'_{tn}$ + Vx:

N1 and N3 are in the saturation region. N4 is within the boundary between saturation and linear regions. V_{in} will be the NMOS threshold voltage in the improved inverter.

$$\frac{1}{2}\beta_1(V_{in} - Vx - V'_{tn})^2 +$$
$$\frac{1}{2}\beta_3(V_g - Vx - V'_{tn})^2$$
$$= \frac{1}{2}\beta_4(V_{in} - V'_{tn})^2$$
$$Vx = \triangle V_{tn},$$

so

$$NM'_L = NM^0_L.$$

We see that the threshold voltage of improved circuit does not vary with $\triangle V_{tn}$, i.e., NM_L is not affected by irradiation.

(C) Vx + $V'_{tn} < V_{in}$:

N1 and N3 are in the saturation region. N4 is in the linear region. The voltage Vx is insignificant when V_{in} exceeds the threshold voltage of the improved inverter. The current of N1 is not affected by the compensation circuit.

2.2 NOR and NAND gates

Improved NOR and NAND circuits are shown in Figs. 2 and 3, respectively. The compensation circuit design procedures are similar to those described for the improved inverter circuit in section 2.1.

β_3, β_4, β_5, and β_6 are the MOSFET gain factors of N3, N4, N5, and N6, respectively. In the NOR gate design, we choose $\beta_4 = \beta_5 = \frac{1}{2}\beta_3$ in NMOSFETs as shown in Fig. 2. In the NAND gate design, we choose $\beta_4 = \beta_5 = \beta_6$ in NMOSFETs as shown in Fig. 3.

3 Simulation Results and Discussion

3.1 Noise Margin Improvement

The technology we used here is a standard 0.8 μm technology [7]. All the circuits are simulated by HSPICE. The physical W/L sizes of PMOSFET and NMOSFET are $2\mu/1\mu$ and $1\mu/1\mu$, respectively. Simulation results for NM_L and NM_H of improved and traditional CMOS inverters are shown in Fig. 4. The NM_L and NM_H versus $\triangle V_t$ curves for the improved and traditional NOR and NAND gate circuits are similar in Fig. 4. From Fig. 4, we can see clearly that the NM_L of the traditional CMOS inverter decreases

rapidly with $\triangle V_{tn}$ as compared with improved one. The results are consistent with the analysis in section 2.1. Moreover, V_{DD} = 3 V is used in the simulation of inverter. The result of noise margin is similar as Fig. 4.

3.1.1 Area Complexity

Let m be the input number of each logic gate, for example, m = 1 for inverter, m = 2 for NOR and NAND gates. The complexities are 2m and (3m+2) for traditional and improved gates, respectively. The area of improved circuit is about 1.5 as large as that of the traditional one, as m is greater than one. This is the tradeoff between area and noise margin. To avoid area consumption, we may only adopt the method to the sensitive point in the circuit simulation level.

4 Conclusion

This work concerns about the problems in circuits under radiation environment. A compensation circuit is shown in simulation to keep the circuit in normal operation condition under radiation environment. The noise margin NM_L does not vary with $\triangle V_{tn}$. This work also proposes a method to solve the static power consumption problem. To simplify power supply circuits, a modified circuit using one voltage source V_{DD} is also given. The circuit also effectively increases the NM_L when V_{DD} is reduced in the future technology.

References

[1] M. G. Buehler, B. R. Blacs, and Y. S. Lin, "Radiation dependence of inverter propagation delay from timing sampler measurements," IEEE Trans. Nucl. Sci., vol. NS-36, p.1981, 1989.

[2] A. H. Johnston, "Super recovery of total dose damage in MOS devices," IEEE Trans. Nucl. Sci., vol. NS-31, p.1427, 1984.

[3] H. Hatano and M. Shibuya, "CMOS logic circuit optimum design for radiation tolerance," Electronics Letters, vol. 19, no. 23, p. 977, 1983.

[4] C. C. Chen, S. C. Liu, C. C. Hsiao, and J. G. Hwu, "A circuit design for the improvement of radiation hardness in CMOS digital circuits," IEEE Trans. Nucl. Sci., vol. NS-39, p.272, 1992.

[5] D. M. Fleetwood, P. S. Winokur, and C. L. Riewe, "An improved standard total dose test for CMOS space electronics," IEEE Trans. Nucl. Sci., vol. NS-36, p.1963, 1989.

[6] N. Weste, and K. Eshraghian, Principles of CMOS VLSI Design, Chap. 2. MA : Addison-Wesley, 1985.

[7] J. M. Wang, S. C. Fang, and W. S. Feng, "New efficient designs for XOR and XNOR functions on the transistor level," IEEE J. solid state Circuits, vol. 29, no. 7, pp. 780-786, July 1994.

Figure Captions

Figure 1 : Improved CMOS inverter.

Figure 2 : Improved CMOS NOR gate.

Figure 3 : Improved CMOS NAND gate.

Figure 4 : Simulation curves of noise margin NM's vs. radiation-induced threshold voltage shift $\triangle V_t$ for CMOS inverters with $\triangle V_{tn} = 2\triangle V_{tp} = 2\triangle V_t$.

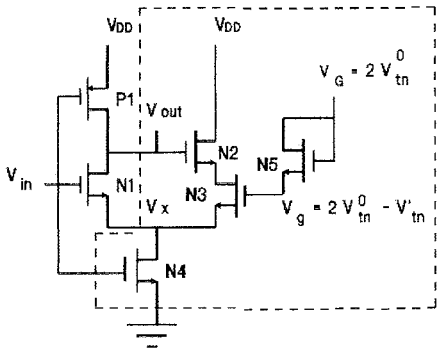

Fig. 1
Improved CMOS inverter.

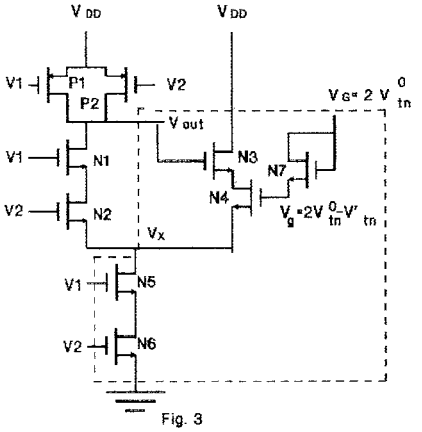

Fig. 3
Improved CMOS NAND gate.

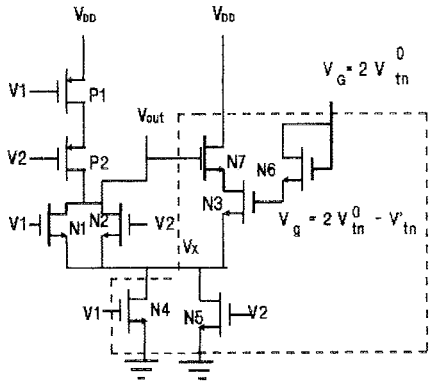

Fig. 2
Improved CMOS NOR gate.

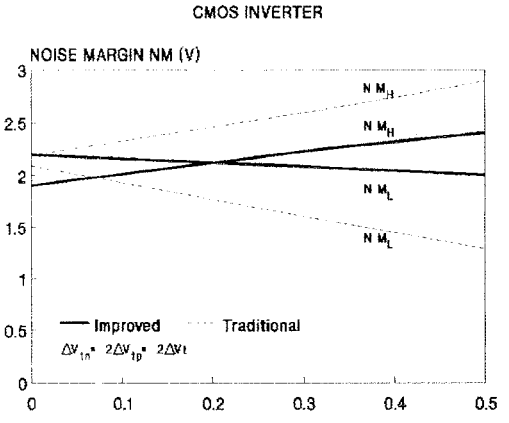

Fig.4 Simulation curves of noise margin NM's vs. radiation-induced shift threshold voltage.