A 0.5-14-GHz 10.6-dB CMOS Cascode Distributed Amplifier

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Abstract

A 0.5-14-GHz distributed amplifier (DA) using 0.18-μm CMOS technology has been presented. It demonstrates the highest gain bandwidth product reported for a CMOS amplifier using a standard Si-based IC process. This DA chip achieves measured results of 10.6 ± 0.9 dB gain, NF between 3.4 and 5.4 dB with good return losses better than from 0.5 to 14 GHz. The measured output IP3 and P_{1dB} are +20 dBm and +10 dBm, respectively, from 2 to 10 GHz.

Introduction

Distributed amplifiers are broadband circuits whose gain-bandwidth product substantially exceeds the transistor unit-gain frequency f_T, by absorbing the input and output capacitances of the active devices in the distributed structures. Table 1 summarizes the recently reported performance of CMOS distributed amplifiers compared with this work [1-6]. Using cascode gain cells and m-derived matching sections, the gain bandwidth product of our chip is believed to be the highest among the recent published results reported for a CMOS distruibted amplifier.

Circuit Design and Fabrication

The cascode configuration, known for its high maximum available gain, wide bandwidth, improved input-output isolation, and variable gain control capability, have been utilized in may applications such as mixers, frequency multipliers and distributed amplifiers. Fig. 1 compares the maximum available gain and maximum stable gain of cascode and common-source stages for the NMOSs with total gain-width of 160 μm, based on the S-parameters of a common-source NMOS from 1 – 30 GHz.

The schematic of the CMOS DA is shown in Fig. 2. It consists of an input and output transmission line formed by using lumped inductors and coupled by the transconducatnces of the MOSFETs. Cascode gain cells and m-derived matching sections are used to enhance the gain and bandwidth performance. Conventional cascode FETs suffer from a large feedback capacitance, the drain-source capacitance of the common-gate transistor. This makes it tend to be unstable and thus more difficult to use in an amplifier circuit than a common-source FET. The cascode devices of this design employ a 20-Ω damping resistor in the gate of common-gate transistor to improve the stability. The inductors were simulated by a full wave EM simulator, Sonnet 6.0, to ensure the model accuracy up to very high frequency [7]. The die micrograph is shown in Fig. 3. The proposed cascode CMOS DA was fabricated using a 0.18-μm 1P6M standard CMOS process. The chip size is approximately 1.0 x 1.6 mm^2 including testing pads.

Measurement Results

The CMOS DA chip was tested via on-wafer probing. Figs. 4 and 5 show the measured gain (S_{21}), return losses (S_{11} and S_{22}) and noise figure from 0.5 to 20 GHz. The power gain is 10.6 ● 0.9 dB and the noise figure is between 3.4 dB and 5.4 dB with good return losses better than 11dB from 0.5 to 14 GHz. The measured S-parameters results agree with the simulated results very well. The power gain of the DA can be controlled with the gate bias of the common gate stage. The measured gain-control range is greater than 25 dB with gain variation less than 3 dB from 0.5 to 14 GHz. The two-tone test result was showed as in Fig. 6. The output IP3 is +20 dBm and the measured output P_{1dB} is +10 dBm from 2 to 10 GHz. The overall performance rivals the recently published results reported for a CMOS dictruibted amplifier.

Acknowledgement

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Process	BW (GHz)	Gain (dB)	GBP (GHz)	NF (dB)	S11 (dB)	S22 (dB)	OIP3 (dBm)	P1dB (dBm)	V_{DD} (V)	P_{DC} (mW)	Ref.
0.8μm CMOS	3	5	9	5.1	<-6	<-9	+20	+7	3	54	[1]
0.6μm CMOS	4	6.5	18	-	<-7	<-10	-	+8.8	3	83.4	[2]
0.6μm CMOS	7.5	5.5	26	8.7 - 13	<-6	<-9.5	-	-	3	216	[3]
0.5μm SOS MOS	10	5	32	-	<-5	<-7	-	-	-	-	[4]
0.18μm CMOS	-	5	-	-	<-14	-	-	-	-	-	[5]
0.18μm CMOS	10	10	100	-	-	-	-	-	-	-	[6]
0.18μm CMOS	**14**	**10.6**	**160**	**3.4 - 5.4**	**<-11**	**<-12**	**+20**	**+10**	**1.3**	**52**	**This work**

Table 1. Recently reported performance of CMOS distributed amplifiers. BW: Bandwidth. GBP: Gain-bandwidth product. NF: Noise Figure. SOS: Silicon-on-sapphire.

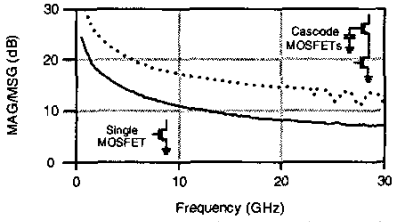

Fig. 1. Maximum stable gain of a single transistor and cascode-connected transistors.

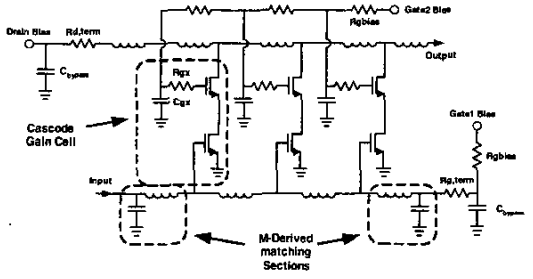

Fig. 2. Schematic circuit diagram of the cascode CMOS DA.

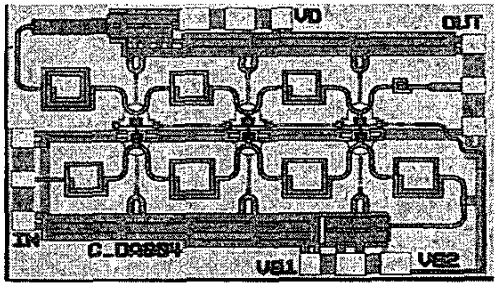

Fig. 3. Microphotograph of the fabricated cascode CMOS DA.

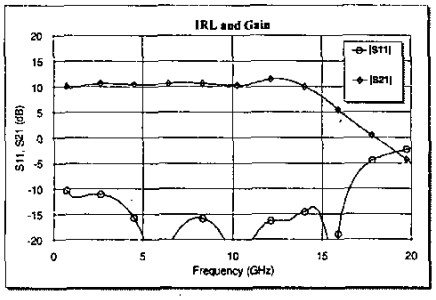

Fig. 4. Measured power gain and input return loss.

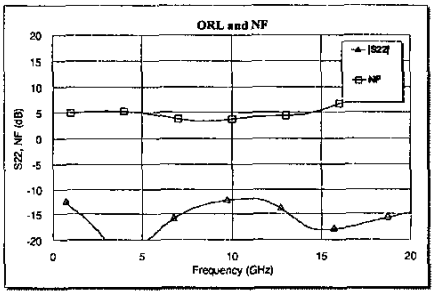

Fig. 5. Measured noise figure and output return loss.

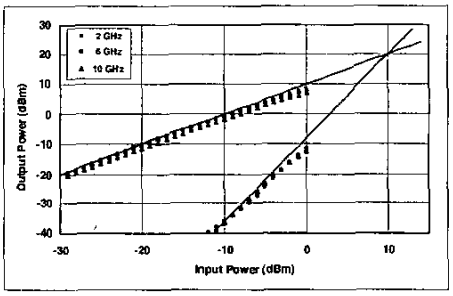

Fig. 6. 1-dB compression point and third order intercepts point measurement at 2, 6 and 10 GHz.

An optimally transformer coupled, 5GHz Quadrature VCO in a 0.18μm digital CMOS process

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Abstract

We present a 5GHz, voltage controlled quadrature oscillator, based on transformer coupling between the quadrature components. The oscillator is fabricated in a 0.18μm, low voltage digital CMOS process with a lossy substrate (ρ ~10mohm-cm) and thin, high resistivity metallization. Fully integrated low Q (~4) spirals form the transformer windings in the resonators. The coupling has been optimized to obtain quadrature accuracy with minimum phase noise degradation. The VCO achieves a tuning range of ~1GHz, and a phase noise of up to -123dBc/Hz at a 1MHz offset, while drawing 7.5mA at 1.6V. An image reject receiver built using the on-wafer quadrature signals, provides 43dB of image rejection, confirming better than 1^0 of quadrature matching.

Introduction

Accurate In-phase (I) and Quadrature (Q) signals are required in many wireless transceiver architectures. Traditionally, the required signals have been generated using poly-phase filters [1], [2], actively coupled oscillators [3], [4] or by a digital frequency divider from an oscillator at twice the desired frequency. All of the above degrade the intrinsic phase noise of the component resonators. In contrast, we produce quadrature linkage through the magnetic fields of mutually coupled resonators. We are thus able to simultaneously optimize area, energy and phase noise in a native 0.18μm digital CMOS process. The process we have used presents significant challenges to VCO design, including a lossy substrate (ρ ~10mohm-cm) and thin (1.6μm, 0.6μm resp.), high resistivity M6, M5, resulting in low Q (~4) inductors. No process enhancements are used in this work.

Quadrature Tank and Transformer Coupling

The conventional LC quadrature oscillator couples two negative impedance based oscillators, operating at the desired carrier frequency (Fig 1a). Without the negative impedance cells (NIC), this circuit can also be redrawn as an explicit 4 stage ring (Fig 1b). Barkhausen's criterion for sustained oscillations stipulates that each stage provide a phase shift of 90^0. Ignoring the inversion at each stage, we require:

$$\theta_{tank} + \theta_{stage} = 90^0 \quad (1)$$

Where θ_{stage} is the phase shift provided by the active devices in the transconductor stages and θ_{tank} is the phase shift across the tank at resonance. Typically, θ_{stage} is small and θ_{tank} is forced to be significantly greater than 0^0, its value at natural resonance. Since the effective quality factor of the tank ($Q_{eff} \alpha d\theta_{tank}/df$) peaks at $\theta_{tank} = 0$ [1], the effective quality factor of the stages of the loop is forced to be significantly lower. This reduces loop gain of the quadrature oscillator and in turn worsens the phase noise performance.

The resonant phase shift of the bandpass LC network (Fig.1c) [5], [6] varies in the range [0^0, 90^0] and can be controlled by the coupling coefficient k. In principle, this network can be used as the stage resonator to satisfy (1) while operating at a frequency close to tank resonance. At low values of k, the phase shift (from port 1 to port 2) of this 2nd order tank approaches 90^0 (Fig. 2a). However, due to the poor quality factor of on-chip inductors, the gain at resonance across the stage also reduces correspondingly. At high values of k, the gain at resonance is higher but the phase shift is very close to 0^0, which reduces to the conventional LC tank (Fig. 2b). Careful optimization of k (Fig. 2c) however shows that over a reasonably wide range of capacitive coupling, large values (close to 90^0) of θ_{tank} can be obtained with good gain.

Since the tanks provide close to 90^0 of phase shift, coupling two of them to form a quadrature pair suggests itself. The phase noise degradation can be minimized if the inter-stage coupling can be affected with the fewest number of active devices. The structure we have implemented (Fig. 3) further lowers the phase noise by using magnetic coupling in a dual transformer arrangement.

The shaded box in Fig. 3a, consisting of the primary winding of transformer T2, secondary of T1 and the nodes I90, $I90_{bar}$, form a differential version of the enhanced tank in Fig 1c. The primary of T1 couples this signal to Q and Q_{bar} , the signal nodes of the quadrature oscillator. The phase shift of the enhanced tank and the coupling arrangement ensures that the current directions in the secondary increase the effective inductance of the primary (the resonating element). For a 1 to 1 turns ratio we have;

Leq = Lp(1+m) where m is the magnetic coupling coefficient between the primary and secondary. The resultant Q boosting further reduces phase noise. A reciprocal arrangement using T2 couples I and I_{bar} on the primary to Q90 and $Q90_{bar}$ on the secondary. The primary is realized on M6 and the secondary on M5 strapped with M4 (also 0.6μm thick). It is important to note that absolute symmetry between the primary and symmetry is not required for quadrature acccuracy. It is sufficient for the bilateral coupling between the component oscillators to be identical. Capacitor Cc is a linear capacitor realized using vertical walls (M2 through M6), and sets the coupling coefficient (k) of the enhanced tank.

The tuning scheme we present does not use diodes or accumulation mode capacitors. The former is not compatible with low voltage techniques and the latter was not available naturally in this low cost digital process. We have achieved a large tuning range (~1GHz) by using a depeletion/inversion varactor (C in Fig. 4), sized with $L_{gate} > L_{min}$ (the minimum gate length). These varactors have a monotonic tuning characteristic with large signal swings, required for PLL stability. In the small signal case, at the maximum control voltage the channel will have disappeared and the capacitance is dominated by the overlap capacitance, resulting in $C_{min}=W.C_{ov}$, where W is the varactor width and C_{ov} is the drain to gate overlap capacitance. At minimum control voltage, the presence of the inversion layer results in $C_{max}=W*L*C_{ox}$. Hence by using an $L_{gate} > L_{min}$, we achieve the required large C_{max}/C_{min} ratio. The large signal effective capacitance