# A BiCMOS Tristate Buffer for High-Speed Microprocessor VLSI

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## Abstract

This paper presents a high speed BiCMOS tristate buffer with a single bipolar device pull-up structure for driving bus with a large capacitive load. With the new pull-structure, the BiCMOS tristate buffer, which is suitable for microprocessor VLSI, has an improvement in delay time over 30% as compared to standard BiCMOS tristate buffer.

## Summary

BiCMOS logic gates have been used intensively in the digital VLSI circuits with a large capacitive load. In a microprocessor VLSI, tristate buffers are often used in driving data bus with a large capacitive load as shown in Fig. 1. The design strategy for the BiCMOS tristate buffers used in driving data bus with a large capacitive load is different from static BiCMOS logic gates [1], owing to the additional disabled state of the tristate buffer. As shown in Fig. 2(a), the standard CMOS tristate buffer has PMOS and NMOS output transistors driven separately by the NAND and NOR gates with control and data signals as inputs. As the control signal is high, the CMOS tristate buffer functions as a standard CMOS static gate with the output determined by the input data. On the other hand, as the control signal is low, both PMOS and NMOS output transistors are disabled and the tristate buffer is disconnected from the data bus. The switching speed of a tristate buffer is determined by the turn-on time as the tristate buffer is accessed and the disabling time of the tristate buffer as another tristate buffer is being accessed. With BiPMOS and BiNMOS transistors to replace CMOS output transistors as shown in Fig. 2(b), the BiCMOS tristate buffer has a higher speed performance. However, the complexity of the circuit increases substantially, which may lower the integration density. As shown in Fig. 3, a concise BiCMOS tristate buffer, which has a single-BJT pull-up structure, is presented. Instead of BiPMOS pull-up structure in standard CMOS tristate buffer, a single bipolar device driven by a CMOS NOR gate is used. With the NOR-driven single-BJT pull-up structure, the new BiCMOS tristate buffer has a higher speed in pull-up as the tristate buffer is selected and a high speed in turning off as it is disabled.

In order to assess the merits of the new BiCMOS tristate buffers, a pair of tristate buffers, connected to the same data bus with a load capacitance of $0.1pf$, driven by a pair of complementary control signals as shown in Fig. 1, has been used in the study. Initially, the data bus is pulled down at 0.2V by a low (D2=low) at the input of the tristate buffer 2, which is enabled by control C2, and the tristate buffer 1 is disabled by C1 with input D1=high. After switching of the two control signals (C2=low-high, C1=high-low) in 1ns, the voltage at the data bus is slewing quickly toward 5V as shown in solid line in Fig. 4(a). The base voltage of the pullup bipolar transistor at tristate buffer 1 as shown in dashed line, is quickly moving toward 5V after the input ramp period, indicating the turning-on of the bipolar device. The pull-up transient of the tristate buffer 1, realized by the single bipolar device shows an about 30% shorter rise time as compared to the case implemented by the standard BiCMOS tristate buffer with a BiPMOS pull-up transistor as a result of the more quickly turn-on of the bipolar transistor without the PMOS device. Fig. 4(b) shows the pull-down transient of the data bus from 4.8V to 0.2V as the tristate buffer 1 is being disabled with D1=high and the tristate buffer 2 is being accessed with D1=low. Thanks to the single bipolar device pull-up structure, the pull-down of the data bus also shows an over 30% shorter fall time as compared to the case with the standard BiPMOS structure as shown in dotted line. Figs.5 show the transients at the data bus with tristate buffers implemented by CMOS, standard BiCMOS, and the new BiCMOS structure. As shown in the figures, speeds in both pull-up and pull-down have been improved. Figs. 6 show the rise and fall times of the data bus with two tristate buffers connected during switching. For a low capacitive load at the data bus, the improvement in the rise time of the standard BiCMOS structure diminishes as compared to the CMOS one. On the other hand, the new BiCMOS structure offers a consistent enhancement in rise time no matter what load capacitance is. As for the fall time, the new BiCMOS structure still shows an overall improvement. Fig. 7 shows the layout of the new tristate buffer in gate array structure using a $2\mu m$ BiCMOS technology. Compared to standard CMOS structure, the new BiCMOS tristate buffer occupies a comparable area. In conclusion, a high speed BiCMOS tristate buffer with a single BJT pull-up structure, suitable for driving a data bus with a large capacitive load, provides a much faster switching time.

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## References

[1] Y. Nishio, F. Murabayashi, S. Kotoku, A. Watanabe, S. Shukuri, K. Shimohigashi, "A BiCMOS Logic Gate with Positive Feedback," digest of 1989 ISSCC.

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[1] Y. Nishio, F. Murabayashi, S. Kotoku, A. Watanabe, S. Shukuri, K. Shimohigashi, "A BiCMOS Logic Gate with Positive Feedback," digest of 1989 ISSCC.

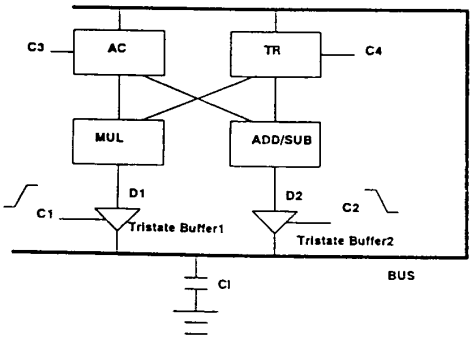



Fig. 1. A portion of a data bus related circuit in a microprocessor VLSI.

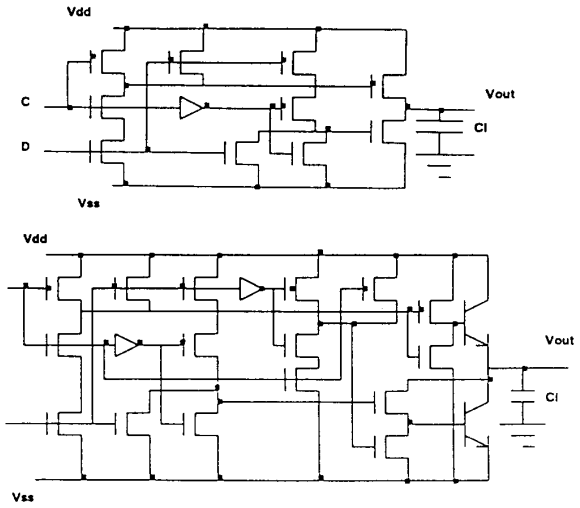



Fig. 2. (a)A standard CMOS tristate buffer. (b)A standard BiCMOS tristate buffer.

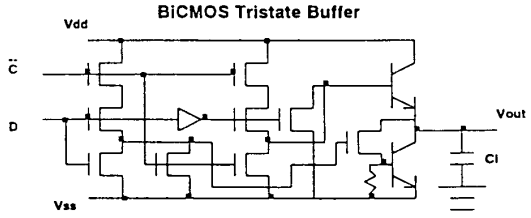
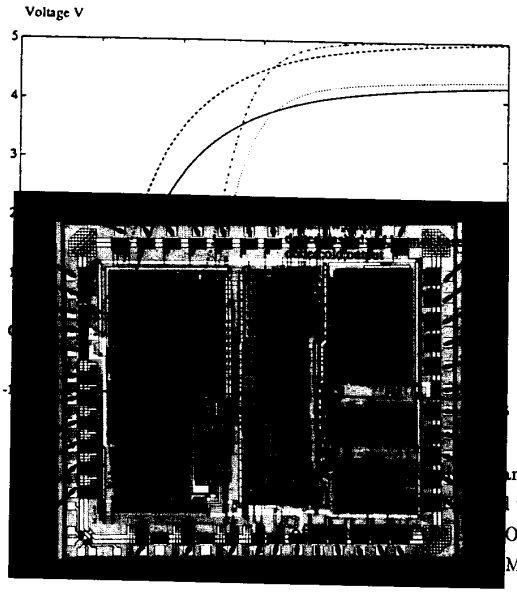
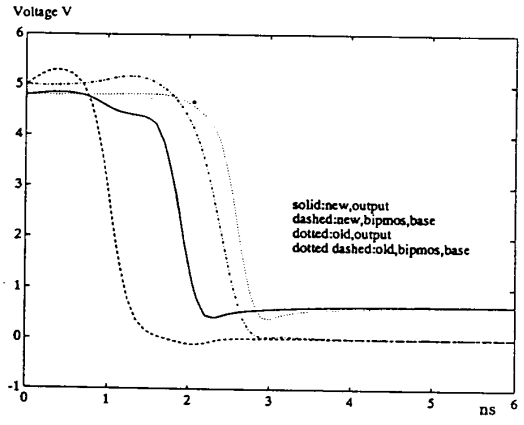



Fig. 3. The new BiCMOS tristate buffer




nsient of an accessed tristate buffer realized
the new BiCMOS techniques. (b)The turn-
OS transistor for an disabling tristate buffer
MOS and the new BiCMOS techniques.

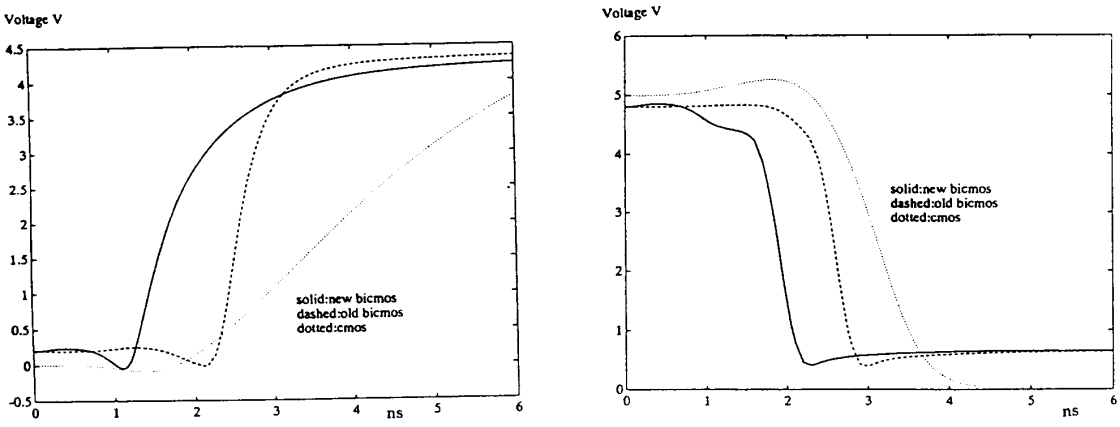



Fig. 5. The waveforms at data bus with a pair of tristate buffers, realized by CMOS, standard BiCMOS, and the new BiCMOS techniques, being switched. (a) Pull-up transient. (b) Pull-down transient.

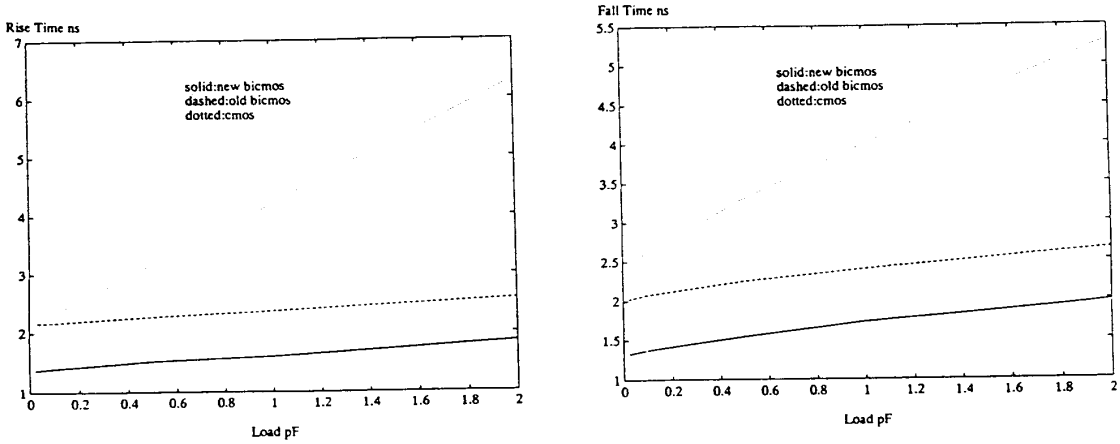



Fig. 6. The switching time of a pair of tristate buffers, realized by CMOS, standard BiCMOS, and the new BiCMOS techniques, connected to the same data bus. (a)The rise time. (b)The fall time.

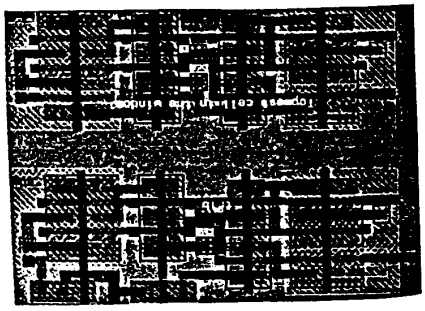


Fig. 7 Layout of the new BiCMOS and the CMOS tristate buffers using a gate array structure.