Performance prediction and function recovery of CMOS circuits damaged by Co-60 irradiation

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Abstract: A performance prediction of total-dose radiation effects on CMOS ICs is described. A good agreement between the simulated and the experimental results is obtained. The function recovery of the postirradiation CMOS ICs can be achieved by increasing the power supply voltage and input signal amplitude, or by an annealing treatment at 350°C in Ar ambient for 10 minutes.

1 Introduction

The total-dose radiation effect on CMOS circuits is important to power plant and space applications. Generally, the device parameters of MOSFETs are changed after irradiation exposure, due to the trapping of oxide charges and the generation of an interface state [1]. These changes may result in the malfunction of CMOS circuits. Some approaches have been proposed to estimate the radiation-induced failure level of CMOS circuits [2, 3]. Briefly, these methods employ the estimation of the key device parameters and the simulation of circuits.

In this paper, we propose a method to predict the failure level of postirradiation CMOS inverters. The key device parameters of MOSFETs, including threshold voltage (V_{TH}) and transconductance (G_M) were chosen according to the experimental results, and the simulation results of CMOS inverters according to these data can be applied to any CMOS circuit. A good agreement between the simulated and the experimental results is observed for the qualitative analysis.

In addition, the functional recovery of CMOS inverters after irradiation exposure is also discussed. The recovery process of the function of postirradiation CMOS inverters is useful, as it can revive the 'dead' circuits. It is known that the negative shift of V_{TH} (ΔV_{TH}) of the postirradiation pMOSFET results in a severe degradation for a CMOS inverter [4]. In this paper, it is shown that the malfunction of the postirradiation CMOS inverters can be recovered successfully by increasing the power supply voltage (V_{DD}) and input signal amplitude. In addition, since the radiation-induced positive charges and interface states can be suitably annealed out [5], it is also found that a functional recovery can be achieved by an anneal at 350°C in Ar ambient for 10 minutes.

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2 Prediction of total-dose radiation effects on CMOS inverters

2.1 Extraction of MOSFET device parameters

The experimental CMOS inverters and MOSFETs are obtained from the commercial RCA 4007 integrated circuits (ICs). The radiation exposure was performed by a Co-60 source with a total dose of 1 Mrad. This gamma source is frequently used to study the radiation-induced degradation of semiconductor devices [2, 4, 8]. The dose rate of the radiation source was about 5×10^3 rads/min and the devices were unbiased during radiation. The postirradiation time before measurement was about 16 hours. The device parameters of the MOSFETs were measured by an Hp4145 semiconductor parameter analyser. Note that the V_{TH} is obtained from the extrapolated value of the drain current I_D against the gate voltage V_G curve at the drain voltage $V_D = 0.1$ V. The G_M is the maximum slope of the measured curve. Fig. 1*a* shows the fresh and the postirradiation I_D against the V_G curves of an nMOSFET with $V_D = 0.1$ V. The extracted device parameters of V_{TH} and G_M are 1.39 V and 110 μA/V, respectively, before irradiation, and 0.911 V and 69 μA/V, respectively, after irradiation. They are also shown in Fig. 1*a*. It can be seen that the postirradiation I_D is larger than the fresh I_D when V_G is smaller than about 2.3 V, but is smaller when V_G is larger than 2.3 V. This is because when V_G is small, the I_D is primarily controlled by the value of V_{TH}. Radiation introduces a decrease in V_{TH}, and so the I_D is increased after irradiation in this region. However, when V_G is large (larger than 2.3 V in this case), the severe degradation of G_M becomes important in controlling I_D. A decrease in G_M due to irradiation introduces a decrease in channel mobility, and therefore a decrease in I_D. Similarly, the fresh and the postirradiation I_D against the V_G curves of a pMOSFET with $V_D = -0.1$ V are shown in Fig. 1*b*. The extracted device parameters of V_{TH} and G_M are -1.37 V and 91.8 μA/V, respectively, before irradiation, and -3.264 V and 66.9 μA/V, respectively, after irradiation, and are also shown in Fig. 1*b*. It is observed that the magnitude of the postirradiation I_D is smaller than the fresh I_D for V_G ranging from -2 to -5 V. This result is different from that observed in Fig. 1*a*. This is due to the greater ΔV_{TH} of a pMOSFET than that of an nMOSFET after irradiation exposure. The ΔV_{TH} of a pMOSFET is 1.89 V and that of an nMOSFET is only 0.48 V in this measurement. This is because in addition to the negative ΔV_{TH} of MOSFETs resulting from the trapping of a positive charge after irradiation exposure, the contribution of interface state generation to ΔV_{TH} is positive for nMOSFETs, but is negative for pMOSFETs [4]. It can be seen

from Figs. 1*a* and *b* that the G_M degradation of an nMOSFET is more severe than that of a pMOSFET. Fig. 2*a* shows that the fresh and the postirradiation I_D curves of an nMOSFET with V_G varies from 2 to 5 V. It is known that the I_D of an nMOSFET is proportional to $(V_G - V_{TH})^2$ in the saturation region, but is proportional to $(V_G - V_{TH})$ in the linear region. Therefore, the contribution of radiation-induced ΔV_{TH} to I_D is larger in the saturation than in the linear region. For an nMOSFET after irradiation, there are two parameters, V_{TH} and G_M, that control the variation of I_D. The V_{TH} is reduced after irradiation, and so its contribution to I_D is positive, but for G_M, its contribution to I_D is negative since its value is reduced after irradiation. Their contribution to I_D are strongly dependent on V_G and the current level. As can be is observed that the postirradiation I_D is larger than the fresh I_D in the linear region for $V_G = 2$ V, but is smaller for $V_G = 3$, 4 and 5 V. This phenomenon is consistent with the observation shown in Fig. 1*a*. In the saturation region, the postirradiation I_D is larger than the fresh I_D for $V_G = 2$ and 3 V, but is smaller for $V_G = 4$ and 5 V. It

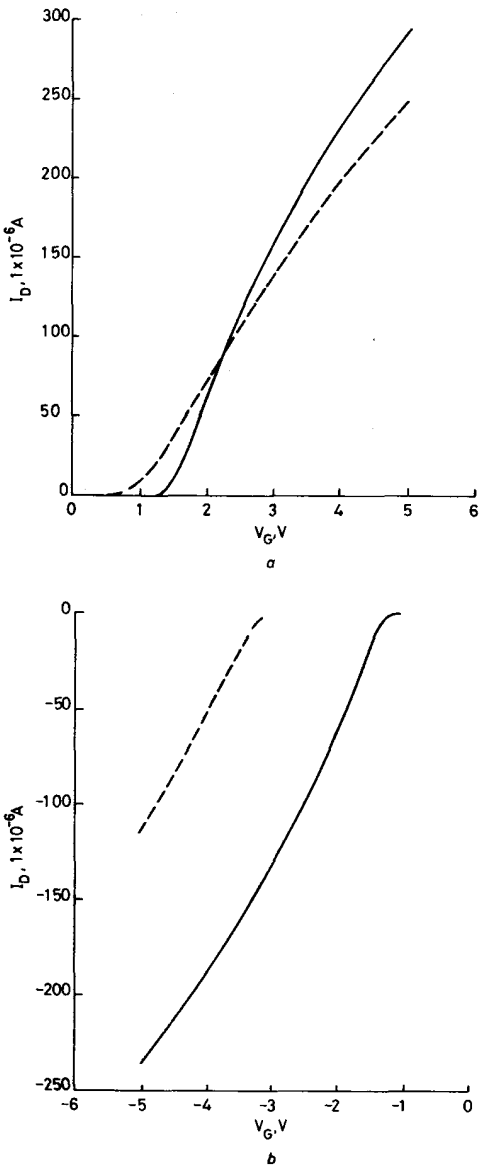

Fig. 1 *The fresh and the postirradiation I_D against V_G curves of*
a an nMOSFET with $V_D = 0.1$ V
——— Fresh, $V_{TH} = 1.39$ V, $G_M = 110$ μA/V
— — Postirradiation, $V_{TH} = 0.911$ V, $G_M = 69$ μA/A
b a pMOSFET with $V_D = 0.1$ V
——— Fresh, $V_{TH} = -1.37$ V, $G_M = 91.8$ μA/V
— — Postirradiation, $V_{TH} = -3.26$ V, $G_M = 66.9$ μA/V

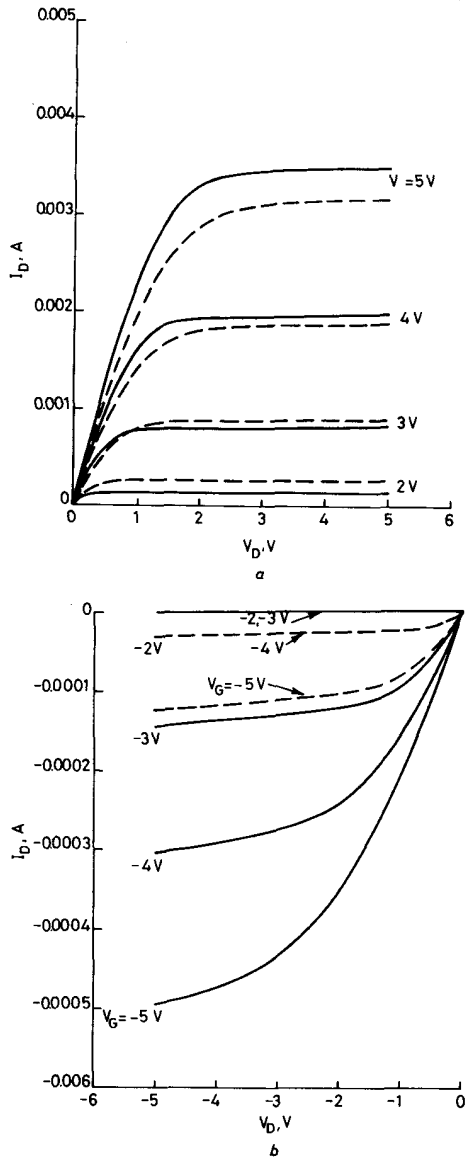

Fig. 2 *The fresh and the postirradiation I_D against V_D curves of*
a an nMOSFET with V_G varying from 2 to 5 V
b a pMOSFET with V_G varying from −2 to −5 V
——— Fresh
— — Postirradiation

seen from the curve of $V_G = 3$ V in Fig. 2*a*, the postirradiation I_D is smaller than the fresh I_D in the linear region, as the contribution of G_M to I_D is larger than the factor $(V_G - V_{TH})$. However, in the saturation region, the postirradiation I_D becomes larger than the fresh I_D as the contribution of G_M to I_D becomes smaller than the factor $(V_G - V_{TH})^2$. It is expected that the V_G needed for the postirradiation I_D to become equal to the fresh I_D in the saturation region is larger than in the linear region as observed in Fig. 2*a*. Fig. 2*b* shows that the fresh and postirradiation I_D against V_D curves of a pMOSFET with V_G varies from -2 to -5 V. It is clear that the magnitude of the postirradiation I_D is much smaller than the fresh I_D for V_G ranging from -2 to -5 V. From the results of Figs. 2*a* and *b*, the radiation-induced degradation of I_D for a pMOSFET can be seen to be much more severe than that for an nMOSFET. This is mainly because both the negative ΔV_{TH} and the decrease in G_M due to irradiation contribute the same trend of decrease in I_D of a pMOSFET. Therefore, the radiation exposure will reduce the on-state drive current, which is determined by the on resistance of the pMOSFET, significantly in CMOS inverters.

2.2 Simulated and experimental results

The CMOS inverter simulation is then performed by the SPICE level 2 model according to the device parameters of MOSFETs extracted from Fig. 1*a* and *b*, as described above. As most of the device parameters except V_{TH} and G_M are estimated by experience, the simulated and experimental data are of course not exactly identical. The discussion of the effects of V_{TH} and G_M in this paper is sufficient for the understanding of the radiation damage on circuit performance. It is known that the mobility μ_0 of the model parameters is proportional to G_M [6]. The μ_0 of postirradiation MOSFETs can be obtained from the multiplication of fresh μ_0 by the ratio of G_M (postirradiation)/G_M (fresh). It is noticeable that the changes in both V_{TH} and G_M should be taken into account in the simulation of the failure-level prediction of postirradiation CMOS inverters. If the change in V_{TH} only is taken into account, the results of simulations not shown in this work are quite different from those of the experimental areas.

Fig. 3*a* shows the simulated results of the fresh and the postirradiation output voltage V_{OUT} against the input voltage V_{IN} transfer curves of a CMOS inverter. The device parameters of the MOSFETs used in the simulation are shown in the figure. As can be seen from this figure, the postirradiation transfer curve is negatively shifted with respect to the fresh one, due to the changes in V_{TH} of the MOSFETs. It is observed from the postirradiation transfer curve that the high noise margin NM_H increases, and the low noise margin NM_L decreases [7]. As the increased value of NM_H is larger than the

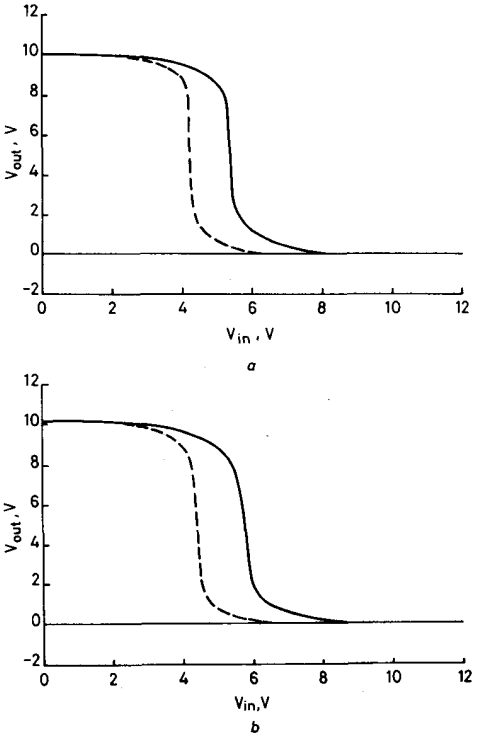

Fig. 3 *The fresh and the postirradiation V_{OUT} against V_{IN} transfer curves of CMOS inverters*

a simulation
——— Fresh, $V_{TO}(n) = 1.39$ V, $V_{TO}(p) = -1.37$ V, $\mu_0(n) = 600$ cm²/V S, $\mu_0(p) = 280$ cm²/V S
— — Postirradiation, $V_{TO}(n) = 0.911$ V, $V_{TO}(p) = -3.264$ V, $\mu_0(n) = 373$ cm²/V S, $\mu_0(p) = 210$ cm²/V S
b experimental
——— Fresh
— — Postirradiation

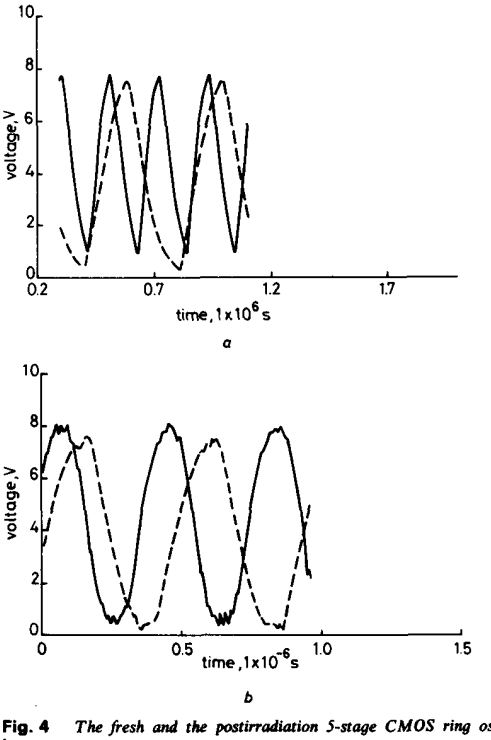

Fig. 4 *The fresh and the postirradiation 5-stage CMOS ring oscillators*

a simulation
——— Fresh, $V_{TO}(n) = 1.39$ V, $V_{TO}(p) = -1.37$ V, $\mu_0(n) = 600$ cm²/V S, $\mu_0(p) = 280$ cm²/V S, $t_{pd} = 68$ ns
— — Postirradiation, $V_{TO}(n) = 0.911$ V, $V_{TO}(p) = -3.264$ V, $\mu_0(n) = 373$ cm²/V S, $\mu_0(p) = 210$ cm²/V S, $t_{pd} = 122$ ns
b experimental
——— Fresh, $t_{pd} = 7.1$ ns
— — Postirradiation, $t_{pd} = 127$ ns

decreased value of NM_L, the uncertainty input range is decreased [7]. Fig. 3*b* shows the experimental results of the fresh and the postirradiation V_{OUT} against V_{IN} transfer curves of a CMOS inverter. Figs. 3*a* and *b* are quite similar. The negative shifts of the transfer curves in these figures are due to the negative ΔV_{TH} of both the nMOSFET and the pMOSFET after irradiation. Because the value of ΔV_{TH} of a pMOSFET is larger than that of an nMOSFET, the increased value of NM_H is larger than the decreased value of NM_L.

Fig. 4*a* shows the simulated results of the fresh and the postirradiation oscillation waveforms of a 5-stage CMOS ring oscillator. The device parameters used in the circuit simulation and the average propagation delay time t_{pd} are shown in the figure. Since the fresh t_{pd} is smaller than the postirradiation t_{pd}, the fresh oscillation frequency is higher than the postirradiation oscillation frequency. It is also noted that both the low-level output voltage V_{OL} and the high-level output voltage V_{OH} of the postirradiation waveform are lower than those of the fresh one. Fig. 4*b* shows the experimental results of the fresh and the postirradiation oscillation waveforms of a 5-stage CMOS ring oscillator. A good agreement is obtained between Figs. 4*a* and *b*. Therefore, it is clear from these figures that the performance of a CMOS inverter is severely degraded after irradiation exposure.

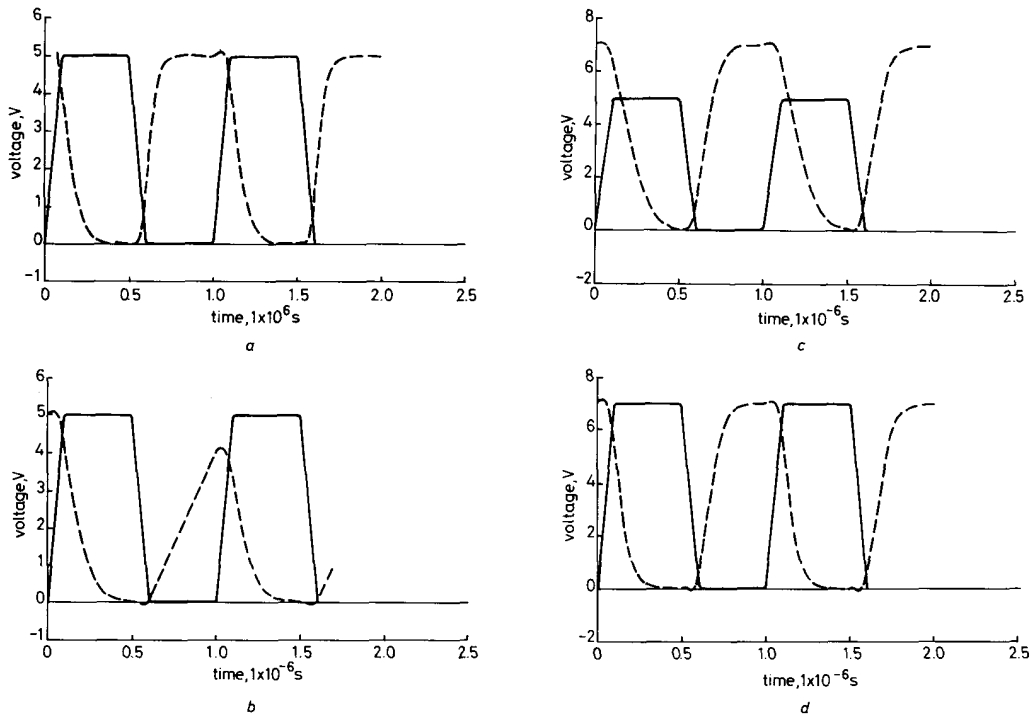

Fig. 5 *Simulated results of input and output waveforms of CMOS inverters*

a Fresh, with $V_{DD} = 5$ V and $V_{IH} = 5$ V
Freq. = 1 MHz, $V_{TO}(n) = 1.39$ V, $V_{TO}(p) = -1.37$ V, $\mu_0(n) = 600$ cm²/V S, $\mu_0(p) = 280$ cm²/V S, $V_{DD} = 5$ V, $V_{IN} = 0\,5, 5$ V
——— Input
— — Output
b Postirradiation, with $V_{DD} = 5$ V and $V_{IH} = 5$ V
Freq. = 1 MHz, $V_{TO}(n) = 0.911$ V, $V_{TO}(p) = -3.264$ V, $\mu_0(n) = 373$ cm²/V S, $\mu_0(p) = 210$ cm²/V S, $V_{DD} = 5$ V, $V_{IN} = 0$ V, 5 V
——— Input
— — Output
c Postirradiation, with $V_{DD} = 7$ V and $V_{IH} = 5$ V
Freq. = 1 MHz, $V_{TO}(n) = 0.911$ V, $V_{TO}(p) = -3.264$ V, $\mu_0(n) = 373$ cm²/V S, $\mu_0(p) = 210$ cm²/V S, $V_{DD} = 7$ V, $V_{IN} = 0$ V, 5 V
——— Input
— — Output
d Postirradiation with $V_{DD} = 7$ V and $V_{IH} = 7$ V
Freq. = 1 MHz, $V_{TO}(n) = 0.911$ V, $V_{TO}(p) = -3.264$ V, $\mu_0(n) = 373$ cm²/V S, $\mu_0(p) = 210$ cm²/V S, $V_{DD} = 7$ V, $V_{IN} = 0$ V, 7 V
——— Input
— — Output

Fig. 5 shows the simulated results of the input and the output waveforms of a CMOS inverter. Note that the frequency of the input waveform is 1 MHz, and the device parameters used in the simulation are noted in the figures. Fig. 5*a* shows a normal performance of a CMOS inverter. The high-to-low propagation delay time t_{pdHL} is approximately equal to the low-to-high propagation delay time t_{pdLH}. It is found that $V_{OH} = V_{DD}$ and $V_{OL} = 0$ V. Fig. 5*b* shows a degraded performance of a postirradiation CMOS inverter. It is found that $t_{pdLH} \gg t_{pdHL}$, $V_{OH} < V_{DD}$, and $V_{OL} = 0$ V. Fig. 5*c* shows a nearly normal performance of a postirradiation CMOS inverter when V_{DD} is increased. It is found that $t_{pdLH} = t_{pdHL}$, $V_{OH} = V_{DD}$, and $V_{OL} > 0$ V. Fig. 5*d* shows a normal performance of a postirradiation CMOS inverter when V_{DD} and V_{IH} are both increased. It is found that $t_{pdLH} = t_{pdHL}$, $V_{OH} = V_{DD}$, and $V_{OL} = 0$ V. Fig. 6 shows the experimental results of the input and the output waveforms of a

CMOS inverter. Note that the frequency of the input waveform is 1 MHz. A good agreement is obtained between Figs. 5 and 6. Fig. 6*a* shows a normal performance of a CMOS inverter. It can be seen from Fig. 6*b* that the on-state function of a CMOS inverter is severely degraded; in other words, the t_{pdLH} increases and the V_{OH} decreases. This is mainly due to the severe degradation of the I_D of the pNOSFET, as described above. Fig. 6*c* shows a more normal performance of a CMOS inverter than Fig. 6*b*, but the V_{OL} is still a little larger than 0 V. Owing to the increase in V_{DD}, an increase in the I_D of the pMOSFET can be achieved. Although Fig. 6*c* successfully obtains an improved on-state performance by increasing V_{DD}, the increase in V_{OH} will retard the off-state function of a CMOS inverter, as the V_{IH} is not increased. It is necessary for a postirradiation CMOS inverter to work as well as the fresh one, by increasing both V_{DD} and V_{IH}. It is clear from Fig. 6*d* that the output waveform shows a normal function of a CMOS inverter, as Fig. 6*a*. Therefore, by increasing V_{DD} and V_{IH}, the performance of a postirradiation CMOS inverter can be improved.

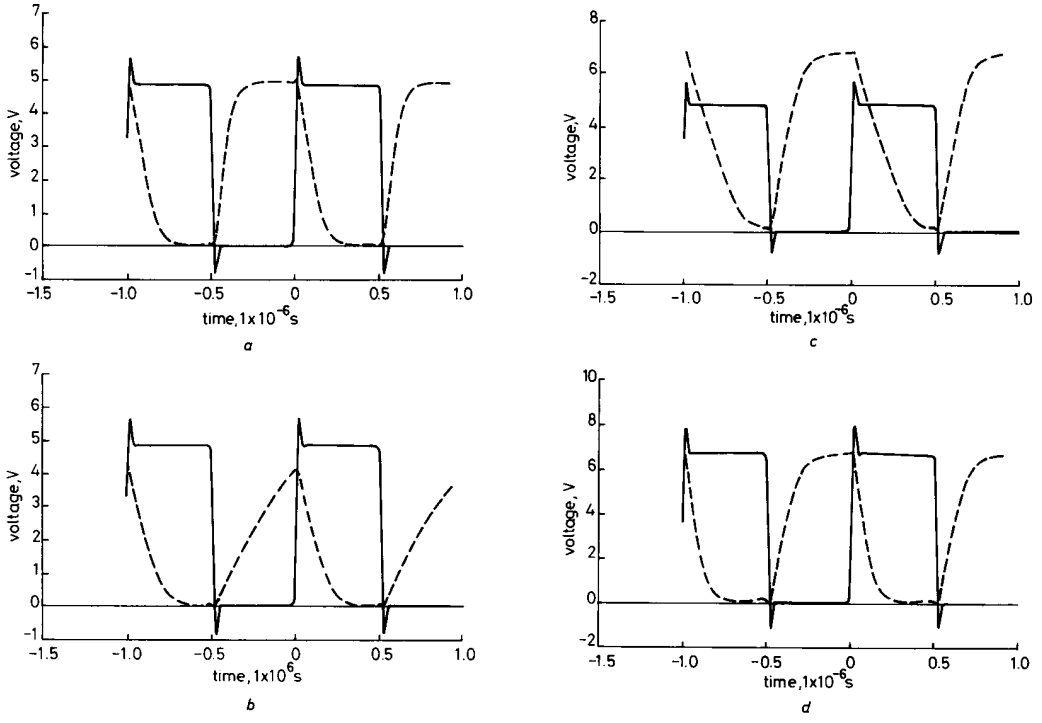

Fig. 6 *Experimental results of input and output waveforms of CMOS inverters*
a Fresh, with V_{DD} = 5 V and V_{IH} = 5 V
b Postirradiation with V_{DD} = 5 V and V_{IH} = 5 V
c Postirradiation with V_{DD} = 7 V and V_{IH} = 5 V
d Postirradiation, with V_{DD} = 7 V and V_{IH} = 7 V
—— Input
– – Output

3 Recovery of radiation-induced CMOS inverter malfunction

The radiation-induced degradation of MOSFETs may result in a malfunction of the CMOS circuit. A performance recovery of this malfunction is very important because it can revive the 'dead' circuit. To recover the function of a postirradiation CMOS inverter, the increases in V_{DD} and V_{IH} as described in Figs. 5*d* and 6*d* is obviously an easy way. In this paper, we propose another way to intrinsically recover the malfunction of a postirradiation CMOS inverter without changing V_{DD} and V_{IH}. It is known that most of the irradiation-induced damage can be annealed out at a suitable temperature or ambient [5, 8]. Generally, a temperature higher than 350°C is used for the annealing treatment of unpackaged devices, temperature higher than 350°C may not be suitable, as the endurable temperature of the commercially, packaged RCA 4007 ICs is limited by its user specification. It is noted that annealing temperatures below 350°C have

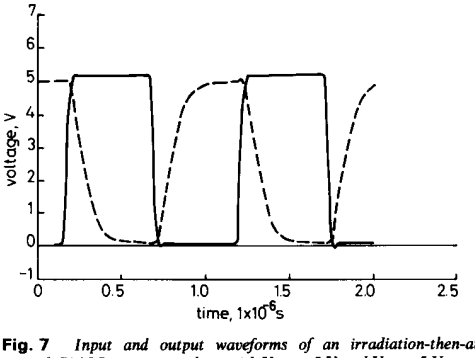

Fig. 7 *Input and output waveforms of an irradiation-then-anneal-treated CMOS inverter working with* V_{DD} = 5 V *and* V_{IH} = 5 V
—— Input
– – Output

been tried, but their efficiency in the recovery of circuit performance is very bad. A temperature of 350°C is therefore chosen for the annealing treatment. This was performed in an Ar ambient for 10 minutes. Fig. 7 shows the input and output waveforms of an irradiated/annealed CMOS inverter which is working with $V_{DD} = 5$ V and $V_{IH} = 5$ V. As can be seen from this figure, a significant recovery of function performance is achieved in comparison with that shown in Fig. 6*b*. Since the output waveforms of Fig. 7 and those of Fig. 6*a* are not completely identical, a further investigation of the annealing treatment condition is worthwhile.

4 Conclusions

A performance prediction of total-dose radiation effects on CMOS ICs is described. From the good agreement between the simulated and the experimental results as described above, it can be concluded that the radiation-induced failure level of CMOS circuits can be predicted precisely by the extraction of the device parameters from th postirradiation MOSFETs and the simulation of the CMOS circuit. The principal benefit of this approach is that it can estimate the total-dose radiation effects on any newly-designed CMOS ICs before fabrication. Although the simulated and the experimental results are not completely identical, they are close enough for qualitative analysis. For a more precise quantitative analysis, all the parameters of MOSFET device models for SPICE simulation should be extracted exactly by a professional technique, not discussed here. As it can be applied to any CMOS circuit, this approach is a novel method for predicting the total-dose radiation effects on the current CMOS circuits used in many applications. The functional recovery of a postirradiation CMOS IC is also discussed, and a simple method is proposed to achieve recovery by increasing the power supply voltage and input signal amplitude. In addition, a significant functional recovery of a postirradiation CMOS IC is also obtained by an annealing treatment at 350°C in an Ar ambient for 10 minutes.

5 Acknowledgment

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