A 0.8V CMOS TSPC Adiabatic DCVS Logic Circuit with the Bootstrap Technique for Low-Power VLSI

H. P. Chen and J. B. Kuo
Dept of Electrical Engineering, Rm 338
National Taiwan University
Taipei, Taiwan 106-17
Email: j.kuo@ieee.org

Abstract-This paper reports a novel 0.8V CMOS true-single-phase-clocking (TSPC) adiabatic differential cascode voltage switch (DCVS) logic circuit with the bootstrap technique for low-power VLSI. Via the pass transistors and compensating transistors, TSPC scheme has been obtained for easy clocking. Using the capacitance coupling from the bootstrap transistors, this 0.8V TSPC adiabatic DCVS logic circuit with the bootstrap technique consumes 31% less energy as compared to the one using the clocked adiabatic latch (CAL) approach.

I. INTRODUCTION

CMOS VLSI circuits have been evolving into low voltage and low power regimes [1]. For achieving low power requirements, CMOS adiabatic logic circuits have been proved to be an effective approach [1]. In the past a 1.5V energy efficient logic (EEL) circuit based on CMOS adiabatic differential cascode switch logic circuit (DCVS) has been reported [2]. For a low power supply voltage, bootstrap technique has been adopted to increase the speed performance of CMOS drivers [3][4]. Recently, a low-voltage CMOS adiabatic DCVS logic circuit using the bootstrap technique has been reported [5]. However, a four-phase clock is required, which may complicate the circuit design. A clocked CMOS adiabatic latch (CAL) using a TSPC scheme has been developed [6], however its power consumption may not be acceptable for low power applications. In this paper, the bootstrap technique is used to generate a 0.8V CMOS adiabatic DCVS logic circuit using a TSPC scheme. In the following sections, the low-voltage CMOS TSPC adiabatic DCVS logic circuit using the bootstrap technique is described first, followed by performance and discussion.

II. TSPC Adiabatic DCVS Logic with Bootstrap

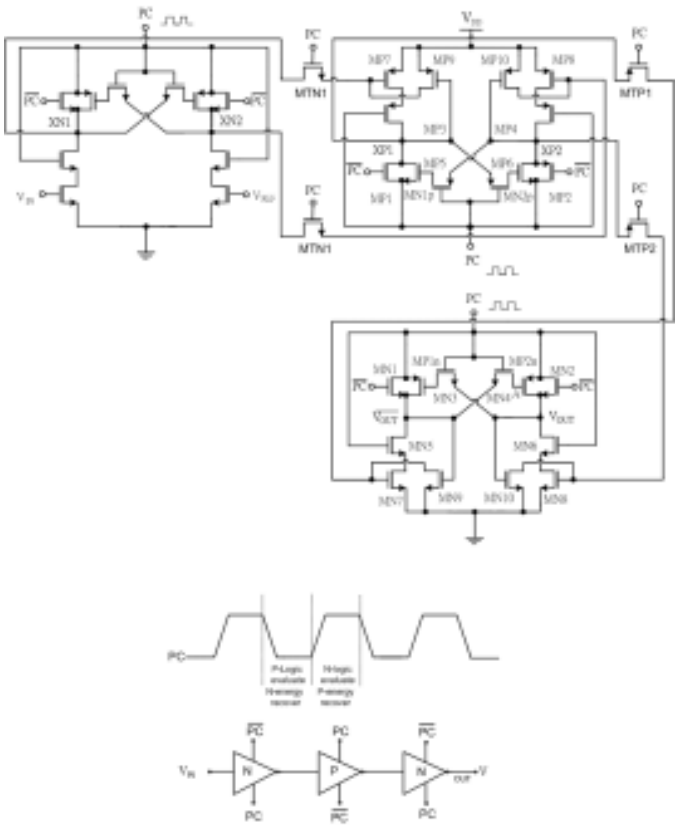

Fig.1. The 0.8V CMOS TSPC adiabatic DCVS logic circuit using the bootstrap technique.

Fig. 1 shows the 0.8V CMOS TSPC adiabatic DCVS logic circuit using the bootstrap technique. As shown in the figure, three cascading DCVS logic cells in n-p-n configuration to facilitate a TSPC clocking scheme have been used. In the n-type DCVS

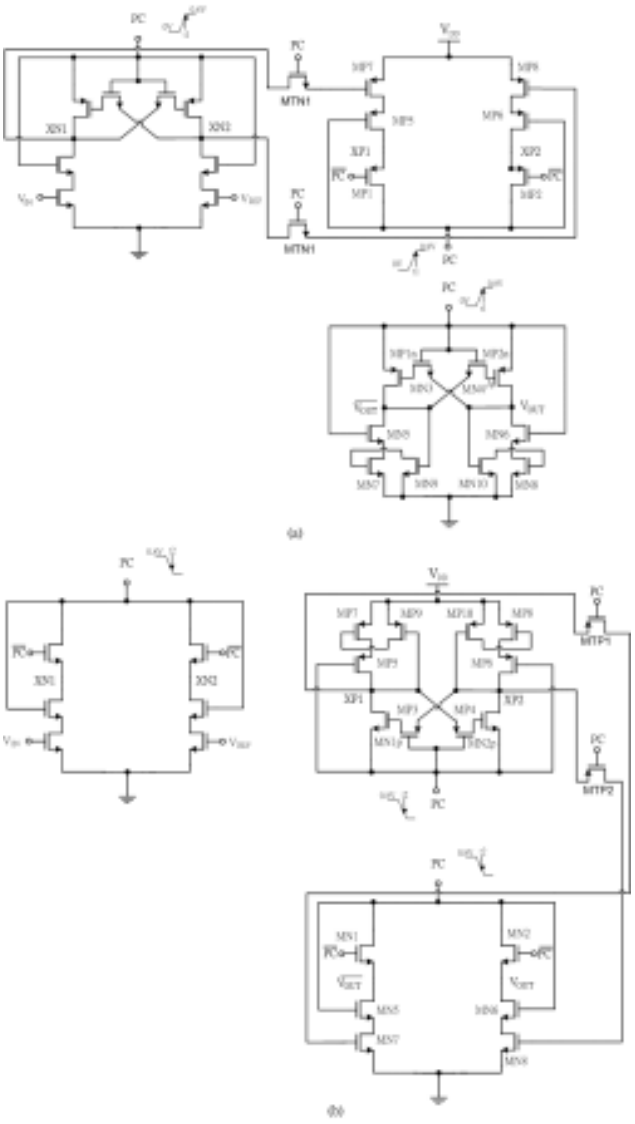

Fig. 2. Equivalent circuits of the 0.8V CMOS TSPC adiabatic DCVS logic circuit using the bootstrap technique when PC is switching from low to high (a) and from high to low (b).

cell, which is derived from a DCVS logic circuit, it contains the cross-coupled bootstrap transistors MN3 and MN4 and two NMOS devices MN5 and MN6 for providing isolation from the input devices. Two PMOS devices MP1 and MP2 are with their body tied to source, instead of being connected to V_{DD} as in the EEL circuit [2]. In p-type cell the configuration is upside down. The

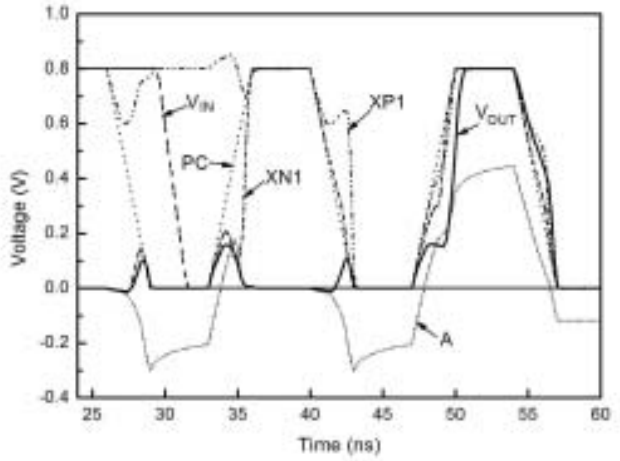

Fig. 3. Transient waveforms of the 0.8V CMOS TSPC adiabatic DCVS logic circuit using the bootstrap technique.

adoption of the complementary n-p-n DCVS logic cells facilitates an easy clocking scheme—single phase clock (PC), which is connected to the top power supply of the n-type DCVS logic cell and to the bottom of the p-type one to facilitate operation of logic evaluate and energy recover for fulfilling the adiabatic function.

When clock PC switches from low to high, the equivalent circuit of this 0.8V CMOS TSPC adiabatic DCVS logic circuit is as shown in Fig. 2(a). Under this situation, the p-type cell is under the energy recover operation and the n-type cells are under the logic evaluate operation with outputs available at XN1/XN2 and XN3/XN4. When PC switches from high to low, the operation is reverse— in the n-type cells energy recovery is carried out from the internal nodes XN1/XN2 and the output nodes and logic evaluation is carried out in the p-type cell with the outputs available at the internal nodes XP1 and XP2.

Owing to the implementation of the bootstrap technique from the cross-coupled bootstrap transistor, the energy efficiency of this 0.8V CMOS TSPC DCVS logic circuit has been enhanced.

III. PERFORMANCE

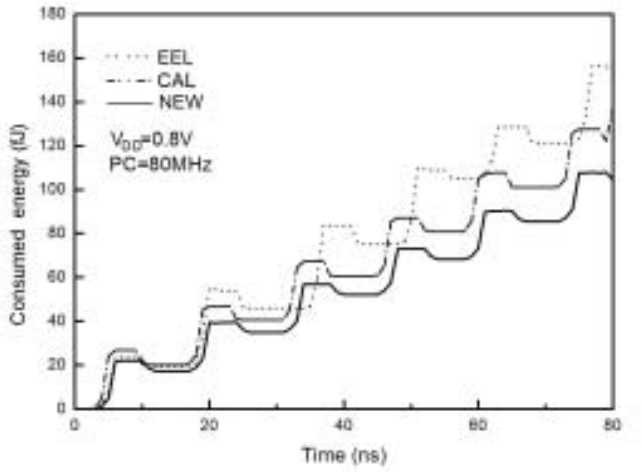

Fig. 4. Consumed energy of the 0.8V CMOS TSPC adiabatic DCVS logic circuit using the bootstrap technique.

In order to assess the performance of this low-voltage CMOS TSPC adiabatic DCVS logic circuit with the bootstrap technique, a test circuit using 0.8V power supply voltage with a capacitive load of 10fF at the output nodes, based on a 0.18um CMOS technology, has been designed. The channel length of all devices in the circuit is 0.2um. The channel width of each NMOS/ PMOS device is 2um/4um. Fig. 3 shows the transient waveforms of the 0.8V CMOS TSPC adiabatic DCVS logic circuit using the bootstrap technique. As shown in the figure, the internal node A may be below 0V when PC switches from high to low during transient due to the cross-coupled bootstrap transistors MN3 and MN4.

Fig. 4 shows the consumed energy of this 0.8V CMOS TSPC adiabatic DCVS logic circuit using the bootstrap technique operating at PC of 80MHz with an output load of 10fF. Also shown in the figure are the results for the energy efficient logic (EEL) circuit using a four-phase clock [2] and the one using the clocked adiabatic latch (CAL) approach [6]. As shown in the figure, this TSPC adiabatic DCVS logic

IV.DISCUSSION

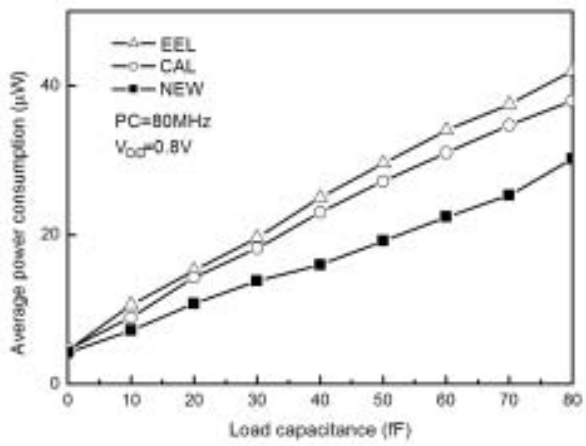

Fig. 5. Average power consumption versus load capacitance of the 0.8V CMOS TSPC adiabatic DCVS logic circuit using the bootstrap technique

circuit with the bootstrap technique indicates a 31% reduction in the energy consumption as compared to the one using the clocked adiabatic latch (CAL) approach [6]. Compared with the EEL one [2], this TSPC adiabatic DCVS logic circuit shows a 18% reduction in energy consumption.

This low-voltage CMOS TSPC adiabatic DCVS logic circuit using the bootstrap technique is especially advantageous when the load is large. Fig. 5 shows the average power consumption versus load capacitance of this 0.8V CMOS TSPC adiabatic DCVS logic circuit using the bootstrap technique at the clock frequency of 80MHz. Also shown in the figure are the results for the one using the energy efficient logic (EEL) approach [2] and the one using the clocked adiabatic latch (CAL) approach [6]. As shown in the figure, this 0.8V CMOS TSPC adiabatic DCVS logic circuit using the bootstrap technique could provide consistent advantages in average power consumption regardless of the load capacitance as compared to the EEL one and the CAL one. At a load capacitance of 80fF, this 0.8V CMOS TSPC adiabatic DCVS logic

circuit using the bootstrap technique offers a 31% reduction in the average power consumption as compared to the CAL one and a 22% reduction as compared to the EEL one.

CONCLUSION

In this paper a novel 0.8V CMOS TSPC adiabatic DCVS logic circuit with the bootstrap technique for low-power VLSI has been reported. Via the pass transistors and compensating transistors, TSPC scheme has been obtained for easy clocking. Using the capacitance coupling from the bootstrap transistors, this 0.8V TSPC adiabatic DCVS logic circuit with the adiabatic technique consumes 31% less energy as compared to the one using the clocked adiabatic latch (CAL) approach.

ACKNOWLEDGMENT

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