Wide Range Linear Tunable BiCMOS Transconductor and Four-Quadrant Multiplier

Shen-Iiuan Liu, Po-Ki Chen and Jiann-Horng Tsay*

Department of Electrical Engineering
National Taiwan University
Taipei, Taiwan 10664, R. O. C.

*Department of Electronic Engineering
Lunghwa Junior College
of Technology and Commerce
300, Wanshou Road, Sec 1, Kueishan,
Taoyuan, Taiwan 333, R. O. C.

Abstract

A new wide range BiCMOS transconductor and a multiplier were presented. Simulation results show that for a power supply of ±5V, the linear input range of this transconductor is over ±4V with the linearity error less than 2%. The total harmonic distortion is less than 0.69% with input range up to ±3V. Its -3dB bandwidth is 54MHz. A new BiCMOS multiplier is also presented. Its linear input range is over ±2.5V with the linearity error less than 1%. Its -3dB bandwidth is over 60 MHz. The proposed circuits are expected to be useful in analog signal-processing applications.

I. Introduction

For most of the proposed transconductors [1-4], the input range for a linear output swing did not exceed 60% of the power supply (±5V). A linear tunable transconductor [4] using the composite MOSFETs is achieved with the linear input range up to ±4V. However, there is a fundamental limitation for this transconductor [4], i.e., the transconductance parameter, K_p, of the PMOS transistor in the composite CMOS pair [3, 4] must be larger than that, K_n, of the NMOS transistor. Practically, since the mobility of PMOS transistors is smaller than that of NMOS transistors (e.g., $\mu_n \cong 3\mu_p$), one must choose very large aspect ratios for PMOS transistors. It will increase the chip area and degrade the high-frequency performance of the transconductor.

The emergence of BiCMOS technologies as a viable approach to VLSI offers new opportunities for improving system performance by combining both bipolar and CMOS technologies [1]. In this paper, a new wide range BiCMOS transconductor and a four-quadrant multiplier using pseudo PNP transistors [5,6] are proposed. Simulation results are given to verify the theoretical analysis.

II. Circuit Description

A wide range BiCMOS transconductor is shown in Fig. 1 [4]. It consists of two pseudo PNP transistors [5,6] (i.e. M_7-Q_1 and M_8-Q_2) and six

0-7803-3073-0/96/$5.00

NMOS transistors, M_1-M_6. Assume that all the devices in Fig. 1 are in their active regions (i.e., BJTs in active and MOSFETs in saturation) and the NMOS transistors M_1 through M_6 have the equal K_n and threshold voltages, V_{Tn}. Transistors M_1 and M_6 have the individual wells to eliminate the body effect. The currents I_1 and I_2 can be given as

$$I_1= K_n(V_1-V_M -V_{Tn})^2=K_n(V_M-V_{SS} -V_{Tn})^2 \quad (1)$$

and $$I_2= K_n(V_2-V_N -V_{Tn})^2=K_n(V_N-V_{SS} -V_{Tn})^2 \quad (2)$$

The voltages V_M and V_N can be obtained with

$$V_1-2V_M=V_2-2V_N= -V_{SS} \quad (3)$$

The current I_3 through the transistors M_5, M_7 and Q_1 can be [3]

$$I_3= K_{eff}(V_C-V_M -V_{Tn}-|V_{Tp}|)^2 \quad (4)$$

where $\frac{1}{\sqrt{K_{eff}}} = \frac{1}{\sqrt{K_n}} + \frac{1}{\sqrt{(\beta+1)K}}$, V_{Tp} is the threshold voltage of the PMOS transistor, and β is the ratio of the collector current to the base current for NPN transistors. For example, since β can be as large as 160 in a standard 2μm BiCMOS process [1], one can approximate that $K_{eff}=K_n$. Similarly, the drain current for M_6 can be obtained with

$$I_4= K_n(V_C-V_N -V_{Tn}-|V_{Tp}|)^2 \quad (5)$$

From eqs. (3)-(5), the output current I_o of this transconductor can be defined and obtained as

$$I_o= I_1+I_4-I_2-I_3=K_n(V_1-V_2)(V_C-V_{SS} -2V_{Tn}-|V_{Tp}|) \quad (6)$$

By using the large intrinsic current gain, β, of a NPN transistor, one can relax the requirement of $K_p>>K_n$ in [4]. To guarantee linear operation for this transconductor, the linear input range can be approximately given as

$$V_{SS}+2V_{Tn}<V_1, V_2<V_{DD}+V_{Tn} \quad (7)$$

A BiCMOS four-quadrant multiplier using the pseudo PNP transistors [5,6] and composite CMOS pairs [7] is shown in Fig. 2. The currents for M_1, M_2, M_3 and M_4 can be

$$I_1= K_{eff}(V_X-V_M -V_{Tn}-|V_{Tp}|)^2 \quad (8)$$

$$I_2= K_{eff}(V_X-V_N -V_{Tn}-|V_{Tp}|)^2 \quad (9)$$

$$I_3= K_{eff}(V_Y-V_M -V_{Tn}-|V_{Tp}|)^2 \quad (10)$$

$$I_4= K_{eff}(V_Y-V_N -V_{Tn}-|V_{Tp}|)^2 \quad (11)$$

where $\frac{1}{\sqrt{K_{eff}}} = \frac{1}{\sqrt{K_n}} + \frac{1}{\sqrt{(\beta+1)K}}$. Assume that the transistors, M_5-M_8, are biased in the saturation region. One can obtain that

$$V_1-V_M=V_2-V_N=\sqrt{\frac{I_{B1}}{K_7}}+V_{Tn} \quad (12)$$

where K_7 and I_{B1} are the transconductance parameter and current of M_7 and M_8 in Fig. 2, respectively. Similarly, for the transistors M_{13}-M_{16}, one can obtain

$$V_X-V_3=V_Y-V_4=\sqrt{\frac{I_{B2}}{K_{13}}}+|V_{Tp}| \quad (13)$$

where K_{13} and I_{B2} are the transconductance parameter and current of M_{13} and M_{14}, respectively. From eqs. (8)-(13), the output current of this BiCMOS multiplier can be expressed as

$$I_o=I_1+I_4-I_2-I_3=2K_{eff}(V_N-V_M)(V_X-V_Y)$$
$$=2K_{eff}(V_2-V_1)(V_3-V_4) \quad (14)$$

III. Simulation Results

The following simulation results are obtained using SPICE with a standard 2μm BiCMOS process in [1]. The aspect ratios for all transistors in Fig. 1 and Fig. 2 are listed in Table 1. The power supply is ±5V and R_L =1kΩ. The transfer curves of Fig. 1 for

various V_C are shown in Fig. 3 with V_2=0, V_{Tn}=0.972V and V_{Tp}=-0.748V. The total harmonic distortion with V_C =5V is found to 0.61, 0.65, 0.69, 1.3% for V_1= 1, 2, 3, 4V. The input range is over ±3V and ±4V with the nonlinearity error less than 1% and 2%, respectively. The -3dB bandwidth is also simulated to be 54, 64, 72 MHz for V_C= 3, 4, 5V.

The transfer curves of Fig. 2 are shown in Fig. 4 with R_L =1kΩ, V_1=-V_2 and V_4=-V_3=±2.5 and ±1V. The input range is over ±2.5V with the nonlinearity error less than 1%. Its -3dB bandwidth is also over 60MHz .

IV. Conclusions

A wide range BiCMOS OTA and a four-quadrant multiplier are proposed. Their performances have been demonstrated by simulations. Using the BiCMOS technologies can increase not only the linearity performance of the OTA and multiplier, but also improve their frequency response. The proposed circuits are expected to be useful in many analog signal processing applications.

References:

[1] M. Ismail and T. Fiez, edited, *Analog VLSI signal and information processing*, McGraw-Hill 1994.

[2] A. Neudungadi and T. R. Viswanathan, "Design of linear CMOS transconductor element", IEEE Trans. Circuits and systems, CAS-31, pp. 891-894, Oct. 1984.

[3] E. Seevinck and R. F. Wassenaar, "A versatile CMOS linear transconductor/square-law function circuit", IEEE J. Solid-State Circuits, SC-22, pp. 366-377, June 1987.

[4] S. C. Huang and M. Ismail, "Linear tunable COMFET transconductor", Electronics Letters, vol. 29, pp. 459-461, March 1993.

[5] K. Tsugaru, Y. Sugimoto, M. Noda, T. Ito and Y. Suwa, "A single-power-supply 10b video BiCMOS sample-and-hold IC", IEEE J. Solid-State Circuits, SC-25, pp. 653-659, June 1990.

[6] S. Sen and B. Leung, " A low-power class-AB BiCMOS opamp using 'pseudo-pnp' transistors", Proceedings of ISCAS '93 , pp. 1136-1139, 1993.

[7] S. I. Liu and Y. S. Hwang, "CMOS four-quadrant multiplier using bias-offset crosscoupled pairs", Electronics Letters, vol. 29, pp. 1737-1738, Sept. 1993.

Table 1 The aspect ratios for devices in Figs. 1 and 2

Fig. 1	M_1-M_6	M_7-M_8	Q_1-Q_2
W(μm)/L(μm)	4/8	12/4	A_E=1
Fig. 2	M_1-M_4	M_5, M_6, M_{15}, M_{16}	M_7-M_8
W(μm)/L(μm)	4/8	4/4	20/4
	M_9-M_{12}	M_{13}-M_{14}	Q_1-Q_4
	24/4	16/4	A_E=1

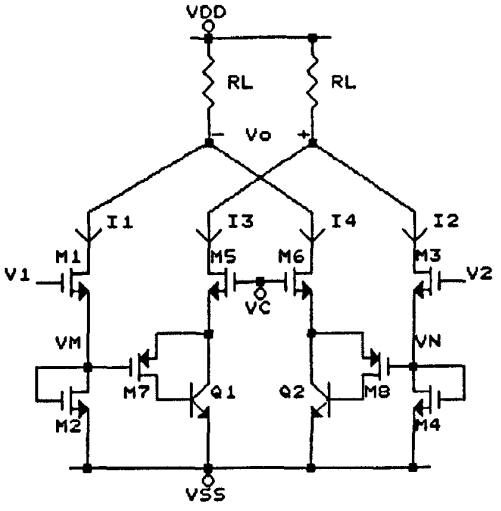

Fig. 1 The proposed BiCMOS transconductor

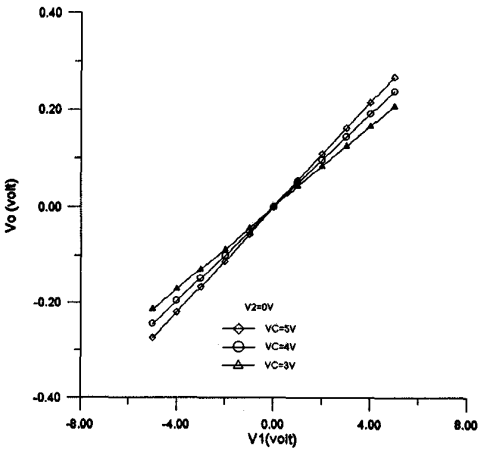

Fig. 3 The transfer curves of Fig. 1 with V_2=0, V_C=3, 4, 5V.

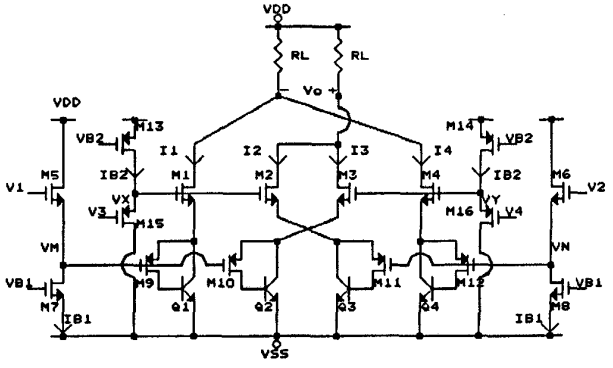

Fig. 2 The proposed BiCMOS four-quadrant multiplier

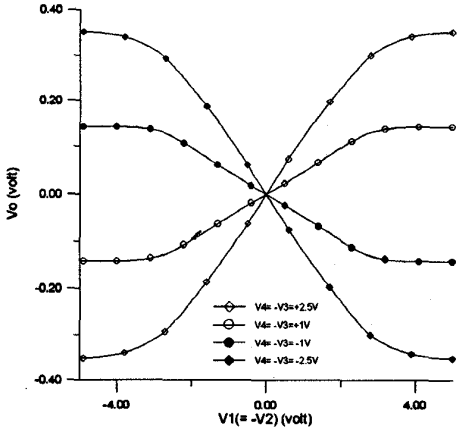

Fig. 4 The transfer curves of Fig. 2 with V_1= -V_2 and V_4= -V_3= ±2.5, ±1V.