variable threshold function in order to eliminate the deadband. The others are used for attenuation using the weighted sum operation of the FG-MOSFETs. When $w_{i n}=w_{i p}=w_{i}$, from eqn. $2, v_{j}$ of $F M_{n}\left(V_{f n}\right)$ and $F M_{p}\left(V_{f p}\right)$ are given by

$$
\begin{align*}
& V_{f n}=V_{i n}\left(D_{0} w_{1}+D_{1} w_{2}+D_{2} w_{3}\right)+w_{4} V_{B n}  \tag{4}\\
& V_{f p}=V_{i n}\left(D_{0} w_{1}+D_{1} w_{2}+D_{2} w_{3}\right)+w_{4} V_{B p} \tag{5}
\end{align*}
$$

where $D_{0}, D_{1}$ and $D_{2}$ are the digital signals and are equal to 1 or 0 . If $V_{B n} \geq V_{T_{n}} / w_{4}$ and $\left|V_{B \eta}\right| \geq \mid V_{T_{p} p} / w_{4}$ are satisfied, the polarities of $V_{T_{n}}^{*}$ and $V_{T_{n}}^{*}$ are changed, and so both $F M_{n}$ and $F M_{p}$ operate as depletion-mode MOSFETs. Consequently, the current operates as a Class AB circuit so that each conducts a small quiescent current for $V_{i n}=0$. Therefore, the deadband can be eliminated perfectly. When we design $w_{1}: w_{2}: w_{3}=2^{0}: 2^{1}: 2^{2}$, from eqns. 4 and 5 , the ideal $V_{\text {out }}$ can be given by

$$
\begin{equation*}
V_{\text {out }}=V_{\text {in }} w_{1} \sum_{j=0}^{2} D_{j} 2^{j}+I_{R L 0} R_{L} \tag{6}
\end{equation*}
$$

where $I_{R L D}$ is $I_{R L}$ at $V_{i n}=0$. From eqn. 6, the circuit operates as a digitally programmable Class AB attenuator.


Fig. 3 Gain against $\left(D_{2}, D_{1}, D_{0}\right)$
$\square$ without $R_{L}$
$\bigcirc R_{L}=10 \mathrm{k} \Omega$


Fig. 4 THD against input signal level
$-\square-\left(D_{2}, D_{1}, D_{0}\right)=(0,0,1)$
$-\triangle-\left(D_{2}, D_{1}, D_{0}\right)=(1,0,0)$

-     - $\left(D_{2}, D_{1}, D_{0}\right)=(1,1,1)$

Simulation and experimental results: The proposed circuit was evaluated using HSPICE simulation with $0.6 \mu \mathrm{~m}$ CMOS process parameters (LEVEL 28). In this simulation, W/L of $F M_{n}$ and $F M_{p}$ were $40 \mu \mathrm{~m} / 3 \mu \mathrm{~m}$ and $80 \mu \mathrm{~m} / 3 \mu \mathrm{~m}$, respectively. To satisfy $w_{i n}=w_{p}$, we used a sufficiently large $C_{4}$ to satisfy $C_{4} \gg C_{0}$, and the value of which was 3 pF . The other weighted capacitors and supply voltage were $C_{3}=2 C_{2}=4 C_{1}=250 \mathrm{fF}$ and $V_{D D}=-V_{S S}=V_{B n}=-V_{B p}$ $=1.5 \mathrm{~V}$, respectively. Fig. 3 shows the relationship between the gain of the circuit and ( $D_{2}, D_{1}, D_{0}$ ). It has high linearity and has variable gain range of -13 dB to -31 dB when $R_{L}=10 \mathrm{k} \Omega$. The total harmonic distortion (THD) against input signal level at $R_{L}=$ $10 \mathrm{k} \Omega$ is shown in Fig. 4. In the simulation, a $3 \mathrm{~V}_{\mathrm{p}-\mathrm{p}}, 500 \mathrm{kHz}$ input signal at $\left(D_{2}, D_{1}, D_{0}\right)=(1,1,1)$ resulted in a THD below $2.3 \%$. The -3 dB bandwidth with $R_{L}=10 \mathrm{k} \Omega$ and the total static power consumption without loads were 11.5 MHz and $14.3 \mu \mathrm{~W}$, respectively. The proposed attenuator was also verified experimentally using discrete devices. In the experiment, $V_{D D}=-V_{S S}=V_{B n}=-V_{B p}=$
$3 \mathrm{~V}, R_{L}=10 \mathrm{~kW}, C_{3}=2 C_{2}=4 C_{\mathrm{t}}=0.1 \mu \mathrm{~F}$ and $C_{4}=0.44 \mu \mathrm{~F}$ were used. Fig. 5 shows an oscilloscope photograph of the circuit with a $6 \mathrm{~V}_{\mathrm{p}-\mathrm{p}}$ triangular wave input. This photograph shows that the experimental circuit operates well as an attenuator without a deadband. The variable gain range of the circuit was -5.0 dB to -20.5 dB .

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Fig. 5 Oscilloscope photograph of experimental circuit
(i) $\left(D_{2}, D_{1}, D_{0}\right)=(0,0,1)$
(ii) $\left(D_{2}, D_{1}, D_{0}\right)=(1,0,0)$
(iii) $\left(D_{2}, D_{1}, D_{0}\right)=(1,1,1)$

Conclusion: A simple digitally programmable attenuator using FG-MOSFETs has been proposed. The device is very useful for analogue signal processing systems.
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## References

1 QIN, S., and GEIGER, R.: 'A $\pm 5$-V CMOS analog multiplier', IEEE J. Solid-State Circuits, 1987, SC-22, (6), pp. 1143-1146
2 OTAKA, s., tanimoto, h., Watanabe, s., and maeda, t.: 'A $1.9-\mathrm{GHz}$ Si-bipolar variable attenuator for PHS transmitter', IEEE J. SolidState Circuits, 1997, 32, (9), pp. 1424-1429
3 GRAY, P.R., and MEYER, R.G.: 'Analysis and design of analog integrated circuits' (John Wiley \& Sons, 1993), 3rd edn., Chap. 5
4 shibata, t., and Ohmi, t.; "A functional MOS transistor featuring gate-level weighted sum and threshold operation', IEEE Trans. Electron Devices, 1992, 39, (6), pp. 1444-1455

## ZVT-PWM boost converter for unity power factor applications

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A ncw single-phase ZVT-PWM boost converter with an active snubber is proposed to achieve unity power factor operations for a wide load range. The unique location of the resonant inductor and capacitor ensures that low switching stress and commutation losses are obtained in the converter. The proposed converter is suitable for high power factor correctors.

Introduction: In recent years, various soft-switching techniques have been proposed to reduce switching losses and EMI noise in switching mode converters. The zero voltage transition-pulsewidth modulation (ZVT-PWM) converters introduced in [1, 2] have been the most successful. They combine desirable features of both the conventional PWM and the soft switching resonant technique.

Soft switching commutation is achieved in the main switch and, as a result, the power losses and EMI are reduced considerably. However, the auxiliary switch in [1] is turned off with hard switching. In [2], the voltage across the auxiliary switch is higher than the output voltage. To overcome these disadvantages, a new sin-gle-phase ZVT-PWM boost converter is suggested in this Letter. This converter is able to improve on the disadvantages of the conventional ZVT-PWM boost converter [1, 2].


Fig. 1 Circuit diagram of proposed converter


Fig. 2 Theoretical waveforms of proposed converter

Proposed converter: The main circuit topology is depicted in Fig. 1. The proposed converter is the combination of the conventional PWM boost converter and the active snubber resonant branch. When the input line is positive (or negative), $D_{b-}$ (or $D_{b+}$ ), $D_{r-}\left(\right.$ or $\left.D_{r+}\right)$ and $D_{n}$ (or $D_{p}$ ) are always turned off, $D_{b+}$ (or $D_{b}$ ), $D_{p}$ (or $D_{n}$ ), $D_{r^{+}}$(or $D_{r-}$ ), $D$ and $S$ perform the boost function with power factor correction. This converter differs from the conventional one. The changed location of the resonant inductor, capacitor and diode ensure low current and voltage stresses in the converter. In order to simplify the analysis, it is assumed that all the components are ideal ( $C_{b+}=C_{b}=C_{b}>C_{s}$ ) and $L$ is treated as a constant current source $I_{L}$. For convenience in analysing the proposed converter, we will consider only the positive half-cycle of the input source. The circuit operation in one switching cycle can be divided into ten stages, and the key operating waveforms of the proposed converter are shown in Fig. 2.

Stage (i) ( $t_{0}, t_{1}$ ): Prior to $t_{0}, S$ and $S_{a}$ are off, $D$ is conducting. At $t_{0}, S_{a}$ is turned on in a zero current switching (ZCS) way and $I_{L r}(t)$ rises linearly from zero to $I_{L}$. At $t_{1}, D$ and $D_{b+}$ are turned off with soft commutation.

Stage (ii) $\left(t_{1}, t_{2}\right)$ : This is the resonant stage. The first resonant path is $C_{s}-C_{b+}-D_{r+}-L_{r}-S_{a}-C_{s}$, and the second resonant path is $C_{a}^{-}$ $L_{r}-S_{a}-C_{a}$. During this stage, $C_{s}$ and $C_{a}$ are discharged, and $C_{b+}$ is charged, then the growth rate of the voltage across $D$ is restricted by the voltage across $C_{s}$ to achieve zero voltage switching (ZVS) turn off. At $t_{2}$, the voltage on $S$ is zero, which is the end of this stage.

Stage (iii) $\left(t_{2}, t_{3}\right)$ : This stage begins when $S$ is turned on at ZVS form. The resonance between $L_{r}, C_{a}$, and $C_{b+}$ continues through $D_{r^{+}+}, S_{a}$, and $D_{s^{*}}$. This stage finishes when $I_{L r}(t)$ reaches $I_{L}$ again.

Stage (iv) ( $t_{3}, t_{4}$ ): In this stage, the current in $S_{a}$ falls from $I_{L}$ to zero while the current in $S$ rises from zero to $I_{L}$. This stage ends when $I_{L r}(t)$ is equal to zero.

Stage (v) $\left(t_{4}, t_{5}\right)$ : During this stage, $C_{b+}$ is linearly discharged by $I_{L}$ and the resonance between $L_{r}$ and $C_{a}$ continues through $D_{S a}, S_{a}$ can be turned off in a ZVS way. This stage finishes when $I_{L r}\left(t_{5}\right)=$ 0.

Stage (vi) $\left(t_{5}, t_{6}\right)$ : During this stage, $C_{b+}$ continues to linearly discharge by $I_{L}$ through $S$. It finishes when the voltage on $C_{h+}$ is zero.
Stage (vii) $\left(t_{6}, t_{7}\right)$ : This stage begins when $D_{b+}$ is turned on in a ZVS way. The circuit operation is identical to the turn-on behaviour of a conventional PWM boost converter.

Stage (viii) ( $t_{7}, t_{8}$ ): This stage begins when $S$ is turned off and ends when $V_{C s}(t)$ is charged to $V_{c a}\left(t_{5}\right)$. During this stage, $C_{y}$ is charged linearly and the growth rate of the voltage across $S$ is limited.

Stage (ix) $\left(t_{8}, t_{9}\right)$ : During this stage, $C_{s}$ and $C_{a}$ are charged linearly by current $I_{L}$. It finishes when $V_{C s}(t)$ and $V_{c u}(t)$ is charged to $V_{0}$.

Stage (x) ( $t_{9}, t_{0}$ ): This stage begins when $D$ is turned on under ZVS. The operation of the circuit at this stage is identical to the normal turn-off operation of a PWM boost circuit. It ends at the moment that $S_{a}$ is turned on to begin a new switching cycle.

Based on the circuit analysis presented above, the proposed active snubber is activated only during the short ZVT transient; the ZVT-PWM converter is identical to a common PWM converter most of the time. Moreover, this converter can be easily built in conjunction with a power factor correction circuit.


Fig. 3 Measured waveforms of proposed converter
a Experimental results of proposed converter
Time: 1 us/div
$b$ Waveform of input line voltage and linc current Time: $5 \mathrm{~ms} / \mathrm{div}$

Experimental results: A 250 W prototype of the proposed converter was buill and tested ( $V_{s}=120 \mathrm{~V}_{\text {rms }}, V_{o}=250 \mathrm{~V}, L_{r}=6 \mu \mathrm{H}$, $C_{b+}=C_{b-}=22 \mathrm{nF}, C_{s}=2 \mathrm{nF}, C_{b}=2 \mathrm{nF}, L=740 \mu \mathrm{H}, C=680 \mu \mathrm{~F}$, $f_{s}=100 \mathrm{KHz}$ ). The key experimental results of the proposed converter are shown in Fig. $3 a$. It can be seen that the experimental waveforms are relatively clean and agree with the theoretical analysis waveforms very well. The main switch is turned on and turned off with ZVS. The auxiliary switch is turned on with ZCS and turned off with ZVS. The conversion efficiency was found to be $92 \%$ at the rated load. Fig. $3 b$ shows the waveform of the input line voltage and line current. The input power factor is nearly unity.

Conclusions: A new ZVT-PWM boost converter using an active snubber has been proposed and tested. Its salient features are as follows: (i) soft switching operation can be easily maintained for a wide line and load range; (ii) there are low switching stress and commutation losses in the converter, and (iii) the auxiliary snubber circuit is simple.
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## References

1 HUA, G., LIEU, C.S., JIANG, Y., and LEE, F.C.: 'Novel zero-voltagetransition PWM converter', IEEE Trans. Power Electron., 1994, 9. (2), pp. 213-219

2 YANG, L., and LEE, C.Q.: 'Analysis and design of boost zero voltage transition PWM converter'. IEEE Power Electron. Spec. Conl Rec., 1993, pp. 707-713

