AMORPHOUS SILICON EDGE DETECTOR FOR APPLICATION TO ELECTRONIC EYES

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Abstract

Two types of novel a-Si:H edge detectors, i.e., concentric and directional ones, are succesfully fabricated. The measured performance of the edge detector is similar to that of the resistor network Si retina using analog VLSI technology. 2-D and 3-D architecture of the a-Si:H image detection array combined with the Si VLSI technology are also discussed with application to the preprocessor of a smart vision system.

1 INTRODUCTION

Pattern recognition is the key technique in machine vision. In conventional approach, the image of the object is recorded by a two dimensional photodetector array like charge-coupled device (CCD), then the brightness level of each pixel is analyzed to extract some special features of the image, usually the edge position or the skeleton of the object, and based on these features the recognition function is performed. Recently, much effort has been made not only in software [1-3] but also in hardware design [4] to implement pattern recognition by means of neural network technique. The strategy is to build a smarter processor such that the recognition can be performed more efficiently and fault tolerant. Much effort is now devoted to the design of the complicated edge detector using silicon very large scale integrated (VLSI) technology [4], and the performance resembles the response of a biological retina. However, the signal extraction is still serial not parallel.

For the past few decades, much is learned about the visual perception function in mammalian brain, which is no doubt the most efficient recognition machine in the world. It is found that the signal sent from the detection system (retina) to the processor (the brain) contains only the edge information and the contrast across the boundary while the absolute brightness level at each photoreceptor in the retina is ignored. In other words, to perform an efficient recognition function, the edge signal of the object is enough, and this information is already extracted by the multilayer structure including bipolar, horizontal, and ganglion cells in the retina, prior to being transferred to the cerebral cortex to make further analysis and final decision [5]. The key feature of the biomachine is that it has a smart detection system and process the information in parallel and hierachically. As a result, in order to build a smarter vision machine, the first step is to design a smarter detection system from which the output already contains only the edge information and the contrast, with all redundancy discarded. A pioneer work has been done by Mead [4], who built the silicon retina by analog VLSI technology. This man-made retina is composed of more than 30 field effect transistors and one phototransistor as a pixel unit, and could be used to extract the edge position of an object image. In this paper, we present a much simpler way to fabricate the edge detector by means of a-Si:H technology. Moreover, we discuss the possibility of combining a-Si:H and crystal Si VLSI technologies to design a three dimensional (3-D) detection system which processes the input data from two dimensional (2-D) array in parallel and in a hierachical manner.

2 DEVICE STRUCTURE

The a-Si:H edge detector is composed of two p-i-n cells in juxtaposition and one resistor as a pixel element. The cross section view of an "off-center" edge detector is shown schematically in Fig. 1 (a). The top geometry of the detector could be many, two of them are shown in Fig. 1 (b), i.e., concentric or two halves. The left part of the edge detector (Fig. 1 (a)) is a simple pin cell with its photocurrent flowing out of p^+ layer representing the excitatory signal. The right part is composed of two carefully designed back to back pin diodes such that its photocurrent normally flows into the top n^+ layer which represents the inhibitory signal. When light is shed simultaneously on the two cells, the photocurrent from the individual cell cancels out, only when the edge of the

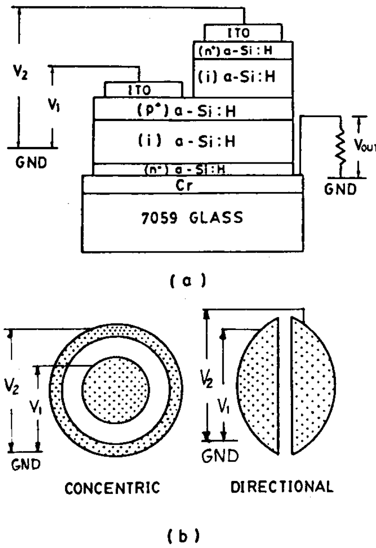

Figure 1: (a) Schematic diagram of the cross-section view of the edge detector. (b) Top geometry of the concentric and directional edge detector.

image happens to fall on the detector will the difference of photocurrents emerges as the edge signal. The concentric one is sensitive to an edge with any orientation but the elongated two-half detector is only sensitive to an edge with preferred orientation along its axis. Each of the two cells can be used as the building block of a 2-D array. However, their wiring diagrams and analysis method are different.

3 EXPERIMENTS

The a-Si:H edge detector shown in Fig. 1(a) is fabricated on Corning 7059 glass substrate. All of the a-Si:H layers are deposited by RF glow discharge decomposition of silane, the substrate temperature and chamber pressure are fixed at 250 °C and 0.5 Torr., respectively. At first the substrate is coated with 800 Å Cr as the ground contact by thermal evaporation. Secondly, the first p-i-n layer was deposited on Cr to form the excitatory cell, the thickness and doping of n^+, undoped, and p^+ layer are 500 Å with 3600 ppm PH_3, 5000 Å, and 500 Å with 3600 ppm B_2H_6, respectively. Then the second Cr layer (1500 Å) is deposited on top of the p^+ layer, patterned and etched away. Only those on the excitatory cell region are retained. The Cr acts as the excitatory cell marker and etch stop for the following processes. The second deposition of the undoped and n^+ a-Si:H follows, the thickness and doping level being 3500 Å and 500 Å with 3600 ppm PH_3, respectively. At this stage, back to back diode is formed in the region not covered by Cr, which is to be used as the inhibitory cell. The undoped and n^+ a-Si:H and the Cr on the excitatory cell is then etched away to expose the top p^+ layer. A final 800 Å ITO is deposited and patterned to complete the process. Two top geometries are adopted as shown in Fig. 1(b), one (concentric rings) for orientational independent and the other (two halves) for directional edge detection.

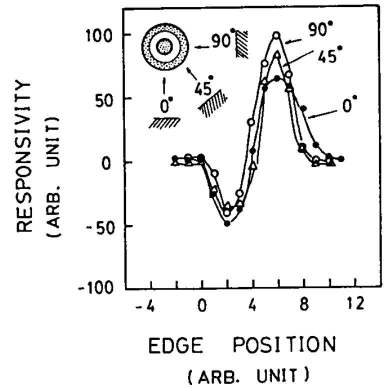

Figure 2: Responsivity of the concentric edge detector as a function of the relative position between the image edge and the detector, there is only little difference between the three curves, indicating the concentric detector is only sensitive to the edge position but not its orientation.

4 RESULTS & DISCUSSION

Figs. 2 and 3 show the measured responsivity of the concentric and directional edge detector as a function of the relative position between the edge and the detector, respectively. The concentric detector has an "off-center" receptive field, it means that when only the center ring is illuminated, the output of the detector is "off", i.e., in our case the output voltage is negative. The measurement is performed as the edge is moving in three different directions, i.e., 0, 45, and 90 degrees with respect to the long axis of the detector. The responsivity of the concentric detector shows little difference among three directions (Fig. 2) whereas those of the directional detector show significant orientation effect (Fig. 3). It

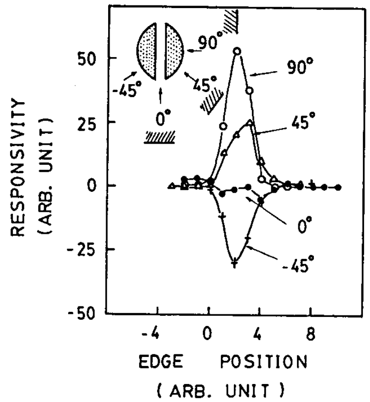

Figure 3: Responsivity of the directional edge detector as a function of the relative position between the image edge and the detector, there is significant difference between the four curves, indicating the directional detector is very sensitive to the edge orientation.

is clear that these simpler new devices can perform the edge extraction function very well. Using the concentric edge detector described above, we are able to build a 2-D detector array, as shown in Fig. 4, which extracts the edge information of the object image only. To increase the cell density, the concentric detectors are arranged in hexagonal shape with each cell addressed by two conducting wires, i.e., one is straight, the other is zigzag. Although this design saves one signal processing step to extract the object edge as compared to the traditional CCD, the access of each pixel is still serial.

It is known that the efficiency of the brain attributes very much to the layer structure and massive parallel processing capability. And the most important thing is that all of these abilities are embedded in the hardware architecture. The data are transferred and processed in parallel in the third dimension normal to the detector plane, layer by layer. Within several layers, the recognition function is completed with fault tolerance. As a result, the most practical way to build an efficient vision machine must be resorted to the 3-D hardware architecture. The 3-D process capability of combining a-Si:H thin film technology with Si VLSI technology just meets the requirement. Fig. 5 displays one possible architecture. The a-Si:H 2-D edge detector array serves as the first layer (the retina) under which lies the crystal Si circuit which extracts the information of the edge orientation. Within two layers the most important features, i.e., edge position and orientation, could be extracted. Because the deposition of a-Si:H

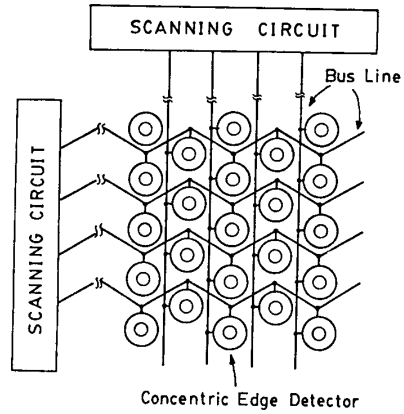

Figure 4: Schematic diagram of the 2-D edge detector array architecture.

is a low temperature process, it can be deposited directly on the VLSI chip. This architecture saves two signal processing steps, and the rest of the analysis can be implemented using software. The key point is that the signal is transferred and analyzed vertically and in parallelity. Prior to the VLSI layer much of the redundancy is filterred away and so it is inherently efficient than the conventional approach. Certainly, more a-Si:H layers can be added to save more processing steps, however, the wiring algorithm between neighboring layers becomes more and more complicated and is still under investigation.

5 CONCLUSION

The a-Si:H edge detectors with two types of device geometries, i.e., concentric and directional, have been successfully fabricated. The measured results show that the much simpler device performs almost the same as that of the more complicated Si retina implemented by the Si analog VLSI technology. Two layer detection system which can extract the object edge and its orientation is proposed which are suitable for application to the implementaion of the 3-D neural network vision system.

References

[1] H. Wechsler, and G. L. Zimmerman; "2-D Invariant Object Recognition Using Distributed Associated Memory", *IEEE Trans. on Pattern Analysis and Machine Intelligence*, Vol. 10, No. 6, pp. 811-821, 1988.

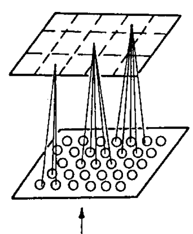

Figure 5: Schematic diagram of one possible connection architecture of the 3-D image detection system incorporated with an a-Si:H edge detector plane, which extracts the edge position, on the Si VLSI chip for orientation extraction and further data processing.

[2] K. Fukushima; "A Neural Network for Visual Pattern Recognition", *IEEE Computer Magazine*, Vol. 21, No. 3, pp. 65-75, 1988.

[3] S. Grossberg, E. Mingolla, and D. Todorovic; "A Neural Network Architecture for Preattentive Vision", *IEEE Trans. on Biomedical Eng.*, Vol. 36, No. 1, pp. 65-84, 1989.

[4] Carver Mead, *"Analog VLSI and Neural Systems"*, Ch. 15, Addison Wesley, U.S.A., 1989.

[5] S. W. Kuffler, J. G. Nicholls and A. R. Martin, *"From Neuron to Brain"*, 2nd. ed., Ch. 2, Sinauer Associates Inc., Massachusetts, 1984.