SPICE Compact Modeling of PD-SOI CMOS Devices

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Abstract

This paper presents PD-SOI SPICE, which is based on compact BiCMOS charge-control models and includes second-order effects, electron and lattice temperatures, for circuit simulation of low-voltage CMOS circuits using deep-submicron partially-depleted (PD) SOI CMOS devices. This PD-SOI SPICE performs transient simulation of the write-access critical path in an SRAM composed of 42 PD SOI CMOS devices without convergence problems, which are commonly encountered while modeling PD devices due to kink effects.

Summary

1.Introduction

SOI CMOS technology has been becoming another major technology for VLSI [1]. Partially-depleted SOI CMOS technology has been used to integrate high-speed microprocessors[2][3]. Due to convergence problems coming from the kink effect[4], simulation of VLSI circuits using partially-depleted SOI CMOS devices has been difficult. In this paper, using a set of compact BiCMOS charge-control models, PD-SOI SPICE performs transient simulation of the write-access critical path in an SRAM, composed of 42 PD SOI CMOS devices without convergence problem, which are commonly encountered while modeling PD devices due to their kink effects.

2.PD Model

Fig. 1 shows the compact BiCMOS charge-control models of the PD SOI NMOS device[5], which are composed of the MOS portion at the surface and the BJT portion with its base formed by the neutral region and its emitter/collector formed by source/drain at the bottom of the silicon thin-film. The MOS portion is composed of the parasitic source/drain resistances (R_S/R_D), the surface channel current (I_T), the related terminal capacitances (C_{ij}; $i,j = D,G,S,B$), and the impact ionization current (I_{ii}). In the BJT portion, Gummel-Poon model has been adopted to include the diode currents (I_{diode}, $\alpha_0 I_{diode}$) and the generation-recombination current (I_{gr}) in the base-source/drain junctions. In addition, the mobile charge (Q_e) and the junction space charge (Q_V) are included. As shown, R_B and C_{Sub} are used to account for the extra parasitic resistance and capacitance. In addition, small-geometry effects, body effect, electron temperature and lattice temperature by inclusion of thermal effect for deep-submicron PD SOI CMOS devices have been included. Using this set of compact BiCMOS charge-control equivalent circuit models for deep-submicron PD SOI CMOS devices, PD-SOI SPICE can perform transient simulation of VLSI circuits accurately without convergence problems.

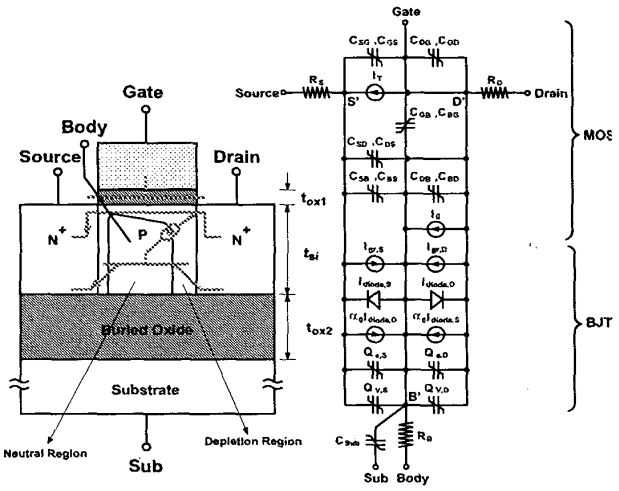

Fig. 1: Compact BiCMOS charge-control models for deep-submicron PD SOI NMOS devices used in PD-SOI SPICE.

3.Lattice & Electron Temperatures

Fig. 2 shows the transient performance in terms of drain current, lattice and electron temperatures, and effective mobility of a PD SOI NMOS device with a channel length of 0.2μm, a channel width of 10μm, a gate oxide of 70Å, and a silicon thin-film of 1000Å, considering the thermal effects: a thermal capacitance of $C_{TH} = 7 \times 10^{-10} J/K$ and a thermal resistance of $R_{TH} = 2 \times 10^4 K/W$ and $8 \times 10^3 K/W$ based on PD-SOI SPICE results. A pulse from 0V to 2V with a rise/fall time of 0.1ns is imposed on

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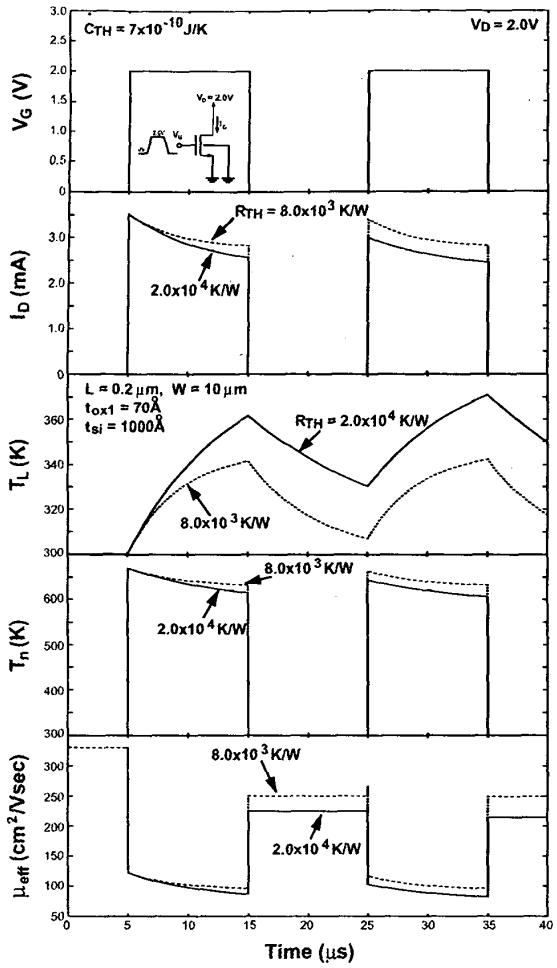

Fig. 2: Transient performance of a 0.2μm PD SOI NMOS device in terms of drain current, lattice and electron temperatures and effective mobility, based on PD-SOI SPICE results.

the input of the PD SOI NMOS device, which is biased at $V_{DS} = 2V$. When the gate voltage rises from 0V to 2V, the drain current rises to the maximum value. However, due to the heat generated by the power consumption, the lattice temperature increases gradually. During turn-on of the device, the electron temperature decreases slightly. The electron mobility, which is related to the electron and the lattice temperatures, reacts accordingly. Hence, the drain current decays gradually. When V_G switches from 2V to 0V, the device turns off. Therefore, the lattice temperature decreases slowly. When the lattice temperature is not back to the room temperature, if V_G turns high again, the peak drain current will be lower than the previous peak value. With a larger thermal resistance, the decrease in the drain current due to thermal effect is more noticeable. Due to a longer thermal time constant ($R_{TH}C_{TH}$) at a larger R_{TH}, the time for the lattice temperature to reach thermal equilibrium is longer.

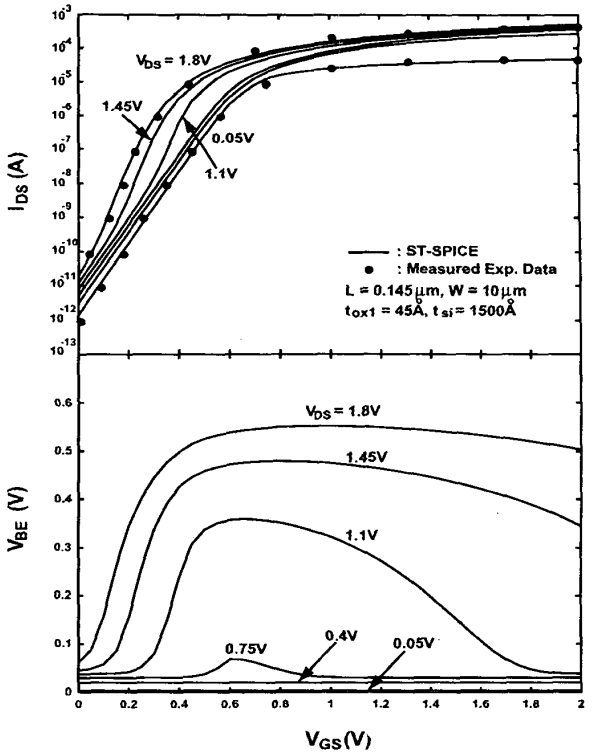

Fig. 3: (a) Drain current (b) body-source voltage characteristics of a PD SOI NMOS device biased in the subthreshold region, with its body node floating, based on the PD-SOI SPICE results, and measured data.

4.Subthreshold Kink

Fig. 3 shows the subthreshold drain current characteristics of a PD SOI NMOS device biased at various drain voltages and with its body node floating, based on the PD-SOI SPICE results and the experimentally measured data[6]. As shown in the figure, as predicted by the PD-SOI SPICE results and confirmed by the experimentally measured data, when the drain voltage exceeds 1.1V, a larger drain voltage leads to a steeper subthreshold slope—the subthreshold kink effect. In the subthreshold kink effect region, when the drain voltage is increased, its impact ionization current also leads to the accumulation of holes in the neutral region. Therefore, the body-source voltage is raised and the threshold voltage of the surface MOS portion is lowered and its drain current increases suddenly— its subthreshold slope is steeper as compared to the case without kink effects. As shown in the figure, as verified by the experimentally measured data, PD-SOI SPICE predicts the subthreshold kink effects well.

5.Circuit Examples

Fig. 4 shows the transient waveforms of an inverter circuit using body-floating PD, body-tied PD and DTMOS PD SOI CMOS devices with a channel length of 0.3μm and a channel width of 10μm, at V_{DD} of 0.7V, based on PD-SOI SPICE and MEDICI results. As shown in the figure,

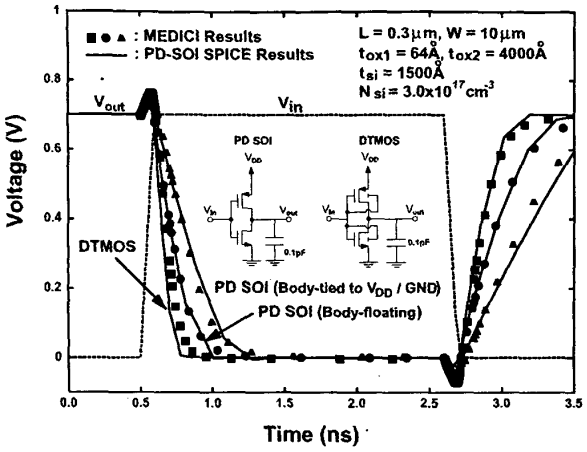

Fig. 4: Transient waveforms of an inverter circuit using body-floating, body-tied and DTMOS PD SOI CMOS devices, based on PD-SOI SPICE and MEDICI results.

the DTMOS one has the faster switching speed, followed by the body-floating one. The body-tied to V_{DD}/GND (for PMOS/NMOS) one has the slowest speed due to body effect. Fig. 5 shows the write transient waveforms of a 6T SRAM memory cell (a) and a two-port 6T SRAM memory cell with single-bit-line simultaneous read-and-write access (SBLSRWA) capability (b)[7] using 0.2μm body-floating(a) and DTMOS(b) PD SOI CMOS devices, based on PD-SOI SPICE and MEDICI results. As shown in the figure, as verified by the MEDICI result, the PD-SOI SPICE results predicts the transients well. Fig.6 shows (a) the write transient waveforms of an SRAM critical path with 42 body-floating and body-tied PD SOI CMOS devices and (b) lattice and electron temperatures of the body-floating PD SOI NMOS devices in the SRAM critical path, based on PD-SOI SPICE and MEDICI results. As shown in the figure, due to the smaller magnitude in the threshold voltage of the precharge body-floating SOI NMOS device connected to the bit lines, after precharge, the bit lines (BL) is set at a higher voltage for the body-floating case. Therefore, a slower sensing speed can be seen for the body-floating case. As shown, the trend on the electron temperatures follows the voltage curves and the variation of the lattice temperatures is not noticeable. Via using compact BiCMOS charge-control equivalent circuit models, PD-SOI SPICE performs transient simulation of an SRAM critical path having 42 PD SOI CMOS devices without convergence problems, which are commonly encountered while modeling PD devices due to kink effects.

Conclusion

In this paper, PD-SOI SPICE, which is based on compact BiCMOS charge-control models and includes second-order effects, electron and lattice temperatures, for circuit simulation of low-voltage CMOS circuits using deep-submicron partially-depleted (PD) SOI CMOS devices has been described. Via using BiCMOS charge-control models, PD-SOI SPICE performs transient simulation of the write-access critical path in an SRAM composed of 42 PD SOI CMOS devices accurately without convergence problems, which are commonly encountered while modeling PD devices due to kink effects.

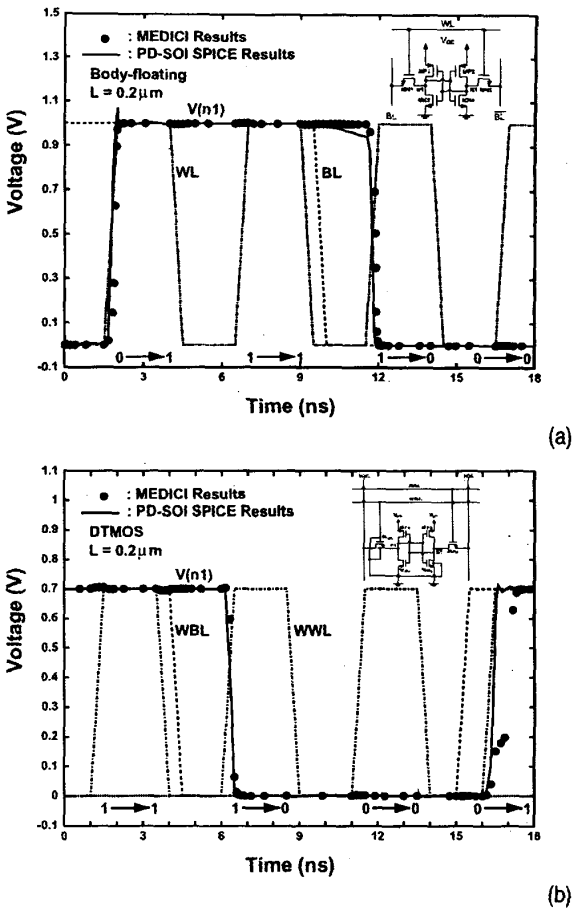

Fig. 5: Write transient waveforms for (a) a 6T SRAM memory cell using 0.2μm body-floating PD SOI CMOS devices and (b) a two-port 6T SRAM memory cell with single-bit-line simultaneous read-and-write access (SBLSRWA) capability using DTMOS PD SOI CMOS devices(5), based on PD-SOI SPICE and MEDICI results.

Acknowledgments

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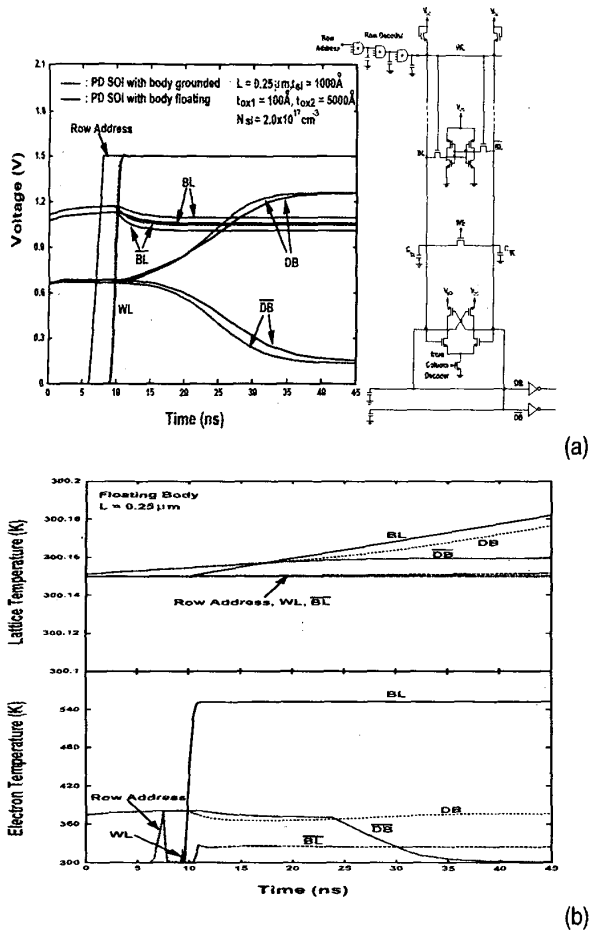

Fig. 6: (a) Write transient waveforms of an SRAM critical path with 42 body-floating and body-tied PD SOI CMOS devices, based on PD-SOI SPICE results. (b) Lattice and electron temperatures of the body-floating PD SOI NMOS devices in the SRAM critical path, based on PD-SOI SPICE results.

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