A 2V Clock Synchronizer using Digital Delay-Locked Loop

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Abstract *: A 2V clock synchronizer chip using digital delay-locked loop is presented. It is targeted to provide synchronous clock distribution in high-speed digital systems. A simple structure with a counter-based delay line is used for compensating the skew caused by process, voltage, temperature and length. A stability criterion is also obtained. Experimental results have demonstrated its advantages like good stability, wide tuning range and low power consumption.*

I. INTRODUCTION

Due to the rapid progress in modern technology, the speed of synchronous data transfer among boards may be up to 100MHz[1]. Clock skew becomes an important issue for both larger die size and higher system clock frequency. Clock skew among chips at different locations may degrade the system performance, and even cause system malfunction. The major reason for clock skew comes from the system clock distribution and the propagation delay of the clock chip. The clock skew resulting from propagation delay is dependent on process, voltage, temperature, and length (PVTL), which are not easy to be eliminated. Traditional methods like analog phase-locked loop (PLL)/delay-locked loop (DLL) suffer from larger power or shorter deskewing range[3-4]. Alternatively, digital DLL's [1-2] will provide good immunity to power supply noise and PVTL effects. Comparing to analog method, digital DLL can provide larger deskewing range and consume lower power in standby mode. Especially, digital DLL's will provide good ability of technology migration in scaling of VLSI devices.

II. CIRCUIT DESCRIPTION

The block diagram of the proposed clock synchronizer is shown in Fig.1. It consists of an improved bang-bang type phase comparator, a set of control logic, a 6-bit up/down counter, a digital controlled delay line (DCDL) and on-chip receivers and driver.

A.Basic Principle

The main function of the clock synchronizer is to distribute the system clock to a remote chip. There should be as less skew as possible between the system clock and input clock. At first, a replica feedback path to the clock synchronizer itself having the same delay as the path to the remote chip is established on board. This makes both ICLK & FCLK to be in phase since Δt_{Line1} is identical to Δt_{Line2}. Then the DCDL will be adjusted to change the phase of OCLK via the up/down counter so as to reduce the skew between SCLK and FCLK. The phase comparator will generate UP/DOWN signal to adjust the delay of DCDL. After both clocks are in phase, the total propagation delay from input clock to the feedback clock becomes a multiple of clock cycles (T_{cycle}). That is

$$\Delta t_{Receiver} + \Delta t_{DCDL} + \Delta t_{Driver} + \Delta t_{Line2} = m * T_{cycle} \quad (1)$$

Since $\Delta t_{Line2} = \Delta t_{Line1}$ for two identical paths, this also makes the total propagation delay from SCLK to ICLK equal to an integer multiple of clock cycles. SCLK and ICLK become in phase after deskewing operation.

A set of control logic including a divider and simple gates will determine the operating speed at one fourth of system clock frequency. These extra circuits will eliminate wrong result of phase comparison since there is a time difference ($m^* T_{cycle}$) between SCLK and FCLK. While receiving the 'JUST' signal, the DCDL will stop adjusting its delay.

B.Phase Comparator

An improved phase comparator that consists of two traditional bang-bang type phase detectors[5] with a few extra logic gates is shown in Fig.2. When one clock speeds the other, either UP or DN signal will be generated. One may find there's one unit delay added in front of the second phase detector. This will force this new phase comparator to generate a "JUST" signal when the phase difference of the two input clocks fall within one unit delay.

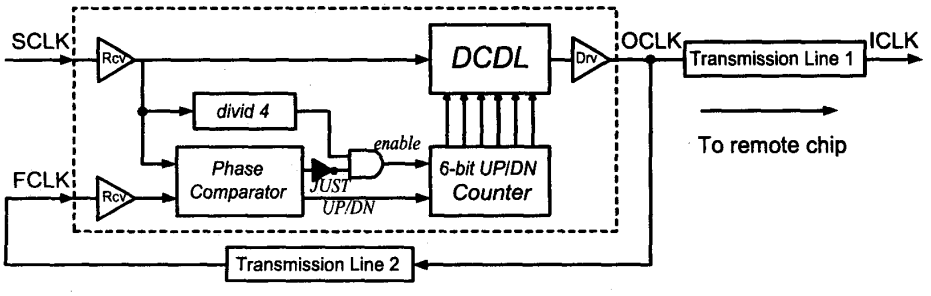
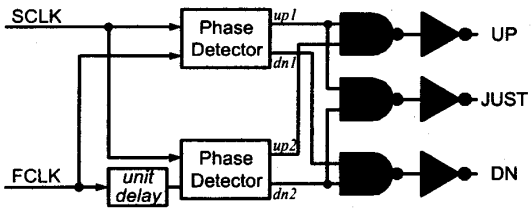
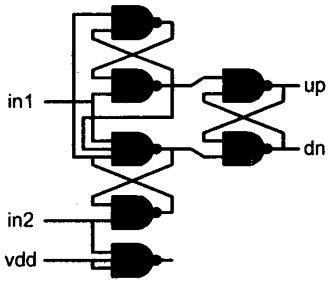


Fig.1 Block diagram of the proposed Clock Synchronizer

Then the "JUST" signal will disable the counter. The main reason and benefit can be shown in later discussion about stability analysis. Thus, the unstable oscillatory phenomenon of DCDL phase can be eliminated. This can also reduce jitter at the clock buffer output.



(a) Whole circuit



(b) Bang-bang type phase detector

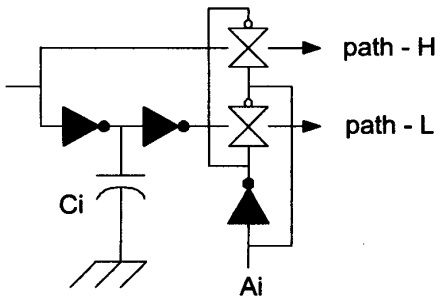
Fig.2 Improved phase comparator

C.Digital Controlled Delay Line

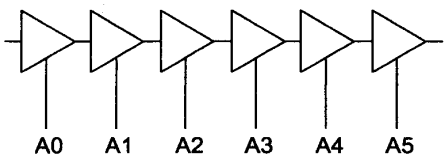
A binary-weighted delay line with 6-bit up/down counter is used to adjust the phase of the output clock. As shown in Fig.3, the delay path of each stage is determined by the counter output word. The capacitance, Ci, is well designed to satisfy the requirement of binary ratio in succeeding stages. The total delay of this DCDL is

$$\Delta t_{DCDL} = \Sigma_i A_i \times 2^i \times Ku + \Delta t_{intrinsic}, \; i = 0 \sim 5 \quad (2)$$

where Ku is the unit delay and $\Delta t_{intrinsic}$ is the delay through the multiplexors. The delay time of DCDL versus control word is shown in Fig.4. The Ku is 170ps and the tuning range is up to 11ns. With only 6 stages, the DCDL will produce less jitter at its output effectively.



(a) Basic structure of delay cell



(b) Binary-weighted delay line

Fig.3 Digital controlled delay line

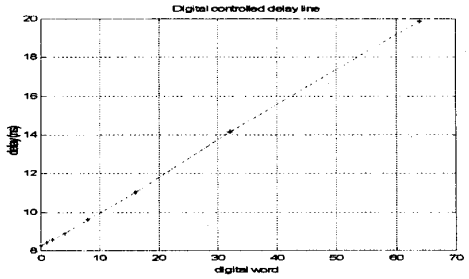


Fig.4 DCDL delay versus control word

D.Stability Analysis

The stability of this clock synchronizer can be analyzed by using the block diagram in Fig.5. The phase comparator is modeled as the combination of a subtractor and a sign function. θe represents the phase difference between system clock and feedback clock. The loop gain of DCDL is modeled as one unit delay Ku because DCDL is digitally controlled and only toggled at ±1 LSB (Ku). Since the system will measure the phase error θe only after a time of an integer multiple of system cycles, the Z^{-m} represents the loop delay, e.g. m=1 means one cycle delay. The close loop transfer function is

$$H(z) = \frac{\text{sign}(\theta e) \times \frac{Ku}{\theta e}}{z^m + \text{sign}(\theta e) \times \frac{Ku}{\theta e} - 1} \quad (3)$$

To maintain the stability of a discrete-time system, the poles should be located within the unit circle of the z-plane. Then we may obtain $|\theta e| > Ku/2$ for stable operation. For $|\theta e| < Ku/2$, the system will become unstable and start to oscillate in its step response as shown in Fig. 6. Two simulation results with $Ku = 2\% * T_{cycle}$ and $10\% * T_{cycle}$ obtained from Matlab are shown in Fig.6. Since the phase error θe will fall into the range of ±Ku/2 at last, the improved phase comparator will generate a "JUST" signal to "open" the feed-forward path to maintain the phase error at a fixed value within ±Ku/2 while in-lock. This will reduce the system jitter effectively.

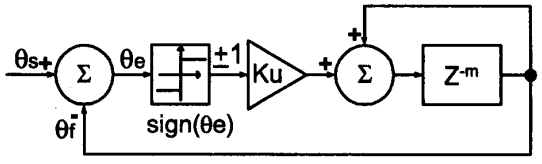
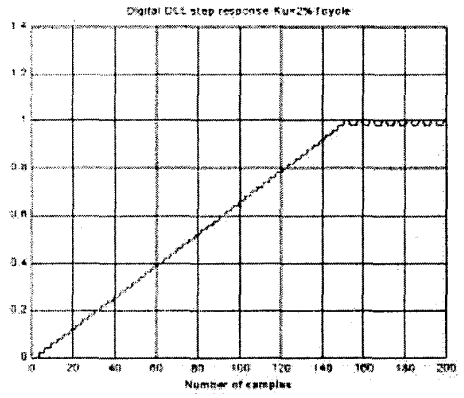
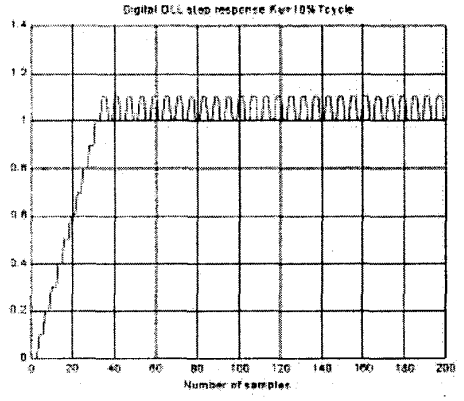


Fig. 5 Equivalent block diagram for stability analysis



(a) Ku=2%*T_{cycle}



(b) Ku=10%*T_{cycle}

Fig.6 Unit-step response

III. EXPERIMENTAL RESULTS

The proposed clock synchronizer chip has been fabricated in Holtek 0.8um SPDM CMOS process. The chip layout is shown in Fig.7. The die size is 2mm x 4mm including I/O pads. And the working voltage can be as low as 2 volts. Using a 10-inch transmission line and input clock range 40 ~ 125 MHz, the maximum skew is less than 400ps. The measured waveforms at 80MHz are shown in Fig.8. The peak jitter at 100MHz is 170ps as shown in Fig.9. The power consumption including an on-chip driver is only 25mW at 100MHz.

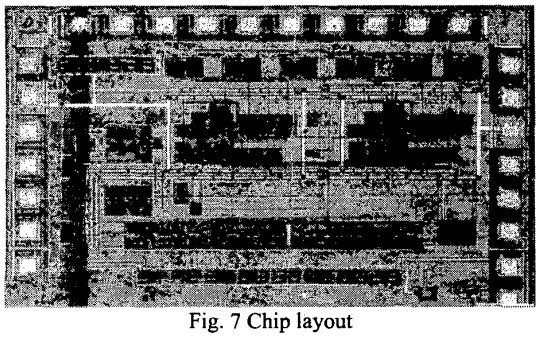
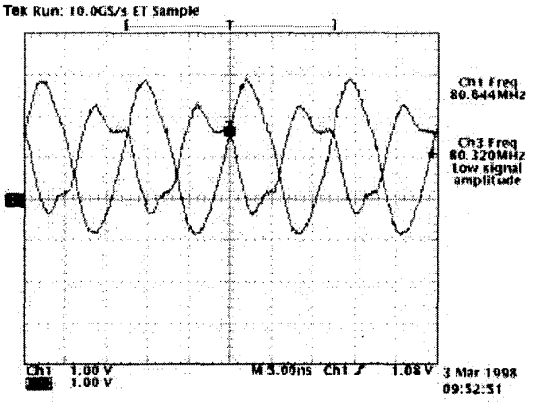
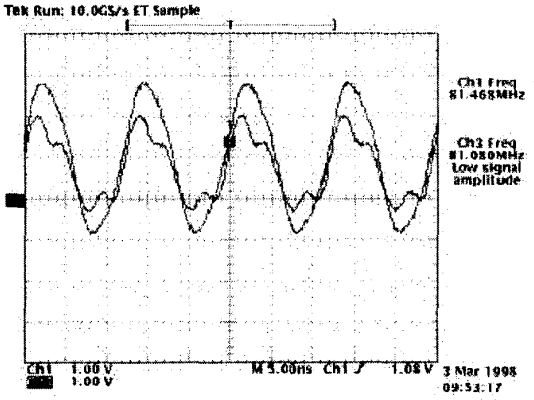


Fig. 7 Chip layout



(a) Before synchronization



(b) After synchronization

Fig.8 Measured waveform at 80MHz

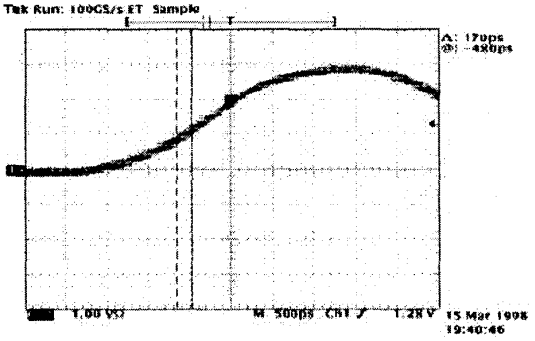


Fig.9 Clock Jitter of clock synchronizer at 100MHz

IV. CONCLUSIONS

A clock synchronizer chip that consists of a counter-based DCDL and an improved phase comparator is presented. A large deskewing range is achieved by using DCDL. The measured results of low skew, jitter, and power also demonstrate its feasibility. The circuit architecture can be easily realized in the future VLSI technology.

ACKNOWLEDGEMENT

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