Fast Fab Scheduling Rule Selection by Ordinal Comparison-Based Simulation

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Abstract -In this paper, an ordinal comparison(OC)-based simulation tool is designed and applied to achieve fast selection of wafer release and lot dispatching rule combination for fab operations. By comparing relative orders of performance among scheduling rules to a specified level of confidence, the OC approach reduces simulation time significantly. The tool consists of 1) a discrete event simulator, 2) a fab model database, 3) a library of scheduling rules, 4) a library of performance indices, 5) an ordinal comparator, and 6) a computation budget allocation. Rule selections from a set of prominent fab scheduling rules under frequently considered fab performance indices such as mean and variance of cycle time and smoothness are studied over various time horizons by using a benchmark fab model. Results demonstrate a potential improvement in efficiency over traditional simulation by two orders of magnitude. In addition to insights about static selection of rules over various objectives and time horizons, our simulation studies also indicate the necessity of dynamic selection.

INTRODUCTION

Semiconductor fabrication is a business of high capital investment, high technology and fierce global competition. It is characterized by short product life cycle, high production add-on values and demands for both excellent quality and timely delivery. Production scheduling has significant impacts on fab performance such as output volume, cycle time and on time delivery. Major fab scheduling problems include how wafers should be released into a fab and how they should be dispatched among machines for processing. As the capital investment and operational complexity of a fab continue to grow, efficient production scheduling has been more important and challenging than before to both practitioners and researchers [3].

A popular practitioners' approach for scheduling the production in a fab is to select from the many empirical or heuristic scheduling rules available in a library for IC fabs. Since there are various combinations of release and dispatching rules and different rules are preferred at different machine groups, a fab usually faces far too many if not formidable options for rule selection. Nevertheless, various fabs have reported that good selections of scheduling rules may lead to 30-60% reductions in mean cycle time [1,4] and are significantly beneficial to production smoothness and equipment utilization [10]. Dynamic selection of rules based on fab status is also highly desirable for competitive fab operations [9].

Simulation tools have been widely adopted as a tool for design and/or selection of scheduling rules [3,8]. It has the advantages of high fidelity and flexibility in coping with the fast-changing characteristic of wafer fabrication, especially foundry fabs. However, in a fab with tens of product types, over 200 failure-prone tools, and more than 300 operation steps per production flow, it usually takes an extensive amount of computation time to obtain a statistically significant performance evaluation for a scheduling rule. In practical applications, quick selection of a good enough scheduling rule is frequently more valuable than finding an optimal rule. Speed in simulation can further facilitate dynamic rule selection.

OC-BASED SIMULATION TOOL

To quickly select a good enough scheduling rule from a rule library, we develop a fast simulation tool based on the ordinal comparison method [2]. Instead of finding the accurate performance among scheduling rules, the method compares relative orders of performance among scheduling rules to a specified level of confidence. It thus finds a good enough rule with a much reduced simulation time requirement than that of finding the best rule. Figure 1 depicts a schematic diagram of our ordinal comparisonbased simulation tool. A snapshot of current states is first taken from the MES as input, which includes machine status, the stage arrival times of each wafer lot, the lot under processing, etc. The simulator evaluates the performance measures of rule options picked up from the library. Ordinal comparison is performed to rank the rules and calculate the confidence probability defined as the probability that the simulated top-ranking rule is actually the best one. The optimal computation budget allocation function allocates along with the simulation more simulation times to rule options that are more promising for improving the probability of correct rule selection. Simulation continues till the confidence probability reaches the specified confidence level. The final ranking then serves as a recommendation for rule selection.

In our study, three performance indices are considered: mean cycle time (MCT), variance of cycle time (VCT) and production smoothness (SM), which are among the most

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frequently used fab performance indices. Smoothness of production flows is defined as the mean of scores of individual stages, where the score of a stage measures how actual production matches the planned target production at the stage. There are fifteen scheduling rules in our rule library, which are combinations of five prominent dispatching rules and three representative wafer release policies as listed in Tables 1 and 2 respectively. Workload regulation release policy proposed by Wein [11], FSMCT and FSVCT dispatching rules proposed by Lu et al. [6], and the OSA rule proposed by Li et al. [7] are known to be good for reducing mean and variance of cycle time. We designed the LDF rule for controlling production smoothness and for tracking production targets.

SIMULATION EXPERIMENTS

To investigate the feasibility and assess computational efficiency of the ordinal comparison-based simulation tool, we consider an aggregated model of a reentrant production line. The model in Figure 2 is from Lu et al. [6]. It involves 12 failure-prone processing stations. With a release rate of 0.52 lots/hour, percentage utilization for most service stations is greater than 90%. Table 3 specifies detailed model parameters.

Static Selection

Experiments are first conducted to select a good scheduling rule for MCT, VCT, and SM from a given initial state of the fab over two different horizons, seven days and four weeks, with a confidence level set to 90%. The initial states are generated by simulating the fab over a one-year horizon starting from an empty fab by using a FSMCT, FIFO, or OSA dispatching rule under deterministic release policy. Traditional simulations with relative standard errors less than 0.5% are also performed for comparison.

As shown in Figure 3, when the operation objective is to minimize MCT over a seven-day horizon, initial states significantly affect rule selection to no surprise. The MCT performances among scheduling rules under a given initial state are extremely close. For VCT minimization, FSMCT and FSVCT dispatching rules are much superior to other dispatching rules over either a seven-day or a four-week horizon (Figure 4). LDF outperforms other dispatching rules in the aspect of SM improvement over a seven-day horizon (Figure 5). This is not unexpected since the LDF dispatching rule is directly designed for improving SM. Although they are not designed directly for improving SM, FSMCT or FSVCT rules can achieve the same or even better SM performance than LDF over a longer time horizon.

Computation times of the OC and traditional simulation approaches for the experiments are shown in Figure 6. The simulation time of each simulation experiment is within eight minutes. It is observed that traditional simulation approach requires up to 195 times more computation time than our OC approach in rule selection under VCT performance criterion. But in the experiments of rule selection for MCT, using the OC simulation tool does not save CPU time. There are two reasons of this phenomenon. First, the performance measures of the top-ranking rules are quite close. Second, the sample variance of the MCT measure is not large; i.e. the MCT performances of most rules are quite close. Except for this experiment, most of the simulations require one to two orders of magnitude less computation time than traditional approach.

In addition, a two-product fab model extended from that of Lu et al. is adopted to study the scheduling rule selection of multi-product IC fabs [5]. Many similar conclusions as those of the single-product model are obtained. It is observed that the CPU time required for selecting a good rule is not a function of number of product types.

From this set of experiments, it is observed that rule selections vary with initial states, performance indices and time horizons. The "state-dependent" feature of rule selection implies that scheduling rule should be selected dynamically according to current system state and operation objective. Another set of experiments is then conducted to explore the necessity of dynamic selection of scheduling rules [9].

Dynamic Selection

In this set of experiment, there are two cases of initial states, "normal" and abnormal by having one bottleneck machine failed for 2 days. Four prominent scheduling rules FSMCT, FIFO, LDF, and OSA combined with the closedloop release policy are considered. Exhaustive evaluation of scheduling rule combinations over a four-week horizon are performed, where rule changes weekly; there are therefore 256 options to evaluate. Results show that using FSMCT throughout the four weeks achieves the best MCT and VCT performance in the normal case. In the abnormal case, the best selections are to apply LDF for the first one or two weeks and then switch to FSMCT (Table 4). The differences in performance as compared with using FSMCT throughout range are between 5% and 28%. It is also observed from the weekly statistics that myopic rule selection of the best rule over each week leads to an inferior performance. In terms of computation efficiency, OC is 12 times faster than the traditional approach when SM is the objective function and over 100 times faster when VCT is the objective. Again, there is no speed up by OC when MCT is the objective.

CONCLUSIONS

In this paper, an ordinal comparison-based simulation tool is proposed for selecting scheduling rules in wafer fabs. Simulation studies clearly indicate that dynamic selection of scheduling rules based on fab status leads to significantly superior fab performance than static selection. Key to the feasibility of dynamic selection for a real fab is computation speed of the simulation. The study of this paper has demonstrated that the ordinal comparison-based simulation is one to two orders faster than the traditional simulation. It is assess that the ordinal comparison-based simulation tool has a good potential in real fab application for fast and dynamic selection of scheduling rules.

ACKNOWLEDGEMENT

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TABLES AND FIGURES

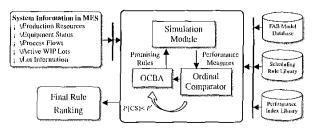


Figure 1. Ordinal comparison-based simulation tool

Table 1.	Description	of wafer	release rules
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SYMBOL	DESCRIPTION			
DETERM	Interarrival times of lots are constant.			
CL(N)	When the number of lots in the fab drops to N-1, release a new lot into the fab.			
WR(C)	Workload regulation release for one bottleneck system. When the expected work in fab for bottleneck machine drops to C hours, then release a new lot.			

Table 2. Description of lot dispatching rules

SYMBOL	DESCRIPTION
FSMCT	Choose the lot with smallest $(\frac{n_p}{\lambda_p} + C_p - \zeta_i)$, where
	<i>n</i> is the number of the lot, <i>C</i> is the mean cycle time, • is the throughput rate, ζ_i is the estimate of the remaining flow time from buffer <i>i</i> , and subscript <i>p</i> represents the index of each product type.
FSVCT	Choose the lot with smallest $(a_n + C_p - \zeta_i)$, where a_n is the release time of lot <i>n</i> .
LDF	Choose a stage with the largest deviation of completed moves from the desired moves and then choose a lot from the stage by FSMCT rule.
_	Choose a stage according to the following priorities: Priority I: stage <i>i</i> s.t. $N_i(t) > \overline{N_i} \& N_{i+1}(t) < \widetilde{N_{i+1}}$;
OSA	Priority II: stage <i>i</i> s.t. $N_i(t) < \overline{N}_i$ & $N_{i+1}(t) < \overline{N}_{i+1}$;
	Priority III: stage <i>i</i> s.t. $N_i(t) > \overline{N}_i \& N_{i+1}(t) > \overline{N}_{i+1}$;
	Priority IV: stage <i>i</i> s.t. $N_i(t) < \overline{N}_i \& N_{i+1}(t) > \overline{N}_{i+1}$,

	where $N_i(t)$ is the WIP at time t at stage i, \overline{N}_i is the
	average WIP at stage <i>i</i> . Choose a lot with the same priority using FSMCT.
FIFO	Select the lot which arrived in the queue at the earliest time.

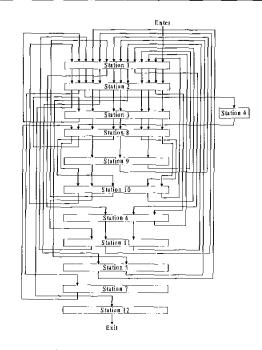


Figure 2. A single product fab model

Table 3. Plant data of the single-product fab model

Station	No. of Machines	No. of Visits	MPT(hr)	MTBF(hr)	MTTR(hr)	% Util
1	4	14	0.5	150	5	94.2
2	3	12	0.375	200	9	82.3
3	10	7	2.5	200	5	93.4
4	1	L	1.8	200	1	94.1
5	1	2	0.9	200	1	94.1
6	2	3	1.2	200	1	94.1
7	1	1	1.8	200	1	94.1
8	4	8	0.8	150	5	86.4
9	i	3	0.6	200	5	96.0
10	9	5	3.0	130	5	90.3
11	2	3	1.2	200	5	96.0
12	2	I	2.5	200	5	67.4

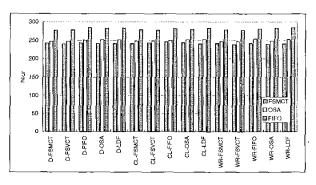


Figure 3. Insignificant difference among rules for MCT

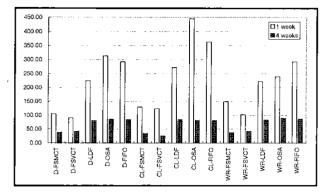


Figure 4. VCT performance under D-FSMCT initialization

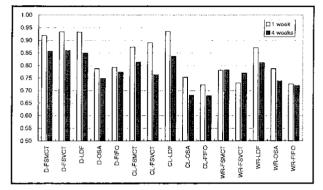


Figure 5. SM performance under D-FSMCT initialization

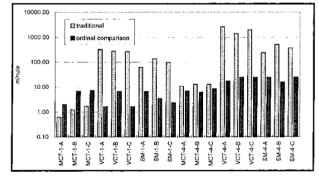


Figure 6. Comparison of computation times

Rank '		Normal Case				Abnormal Case			
	Rule	мст	Rule	VCT	Rule	мст	Rule	VCT	
1	1-1-1-1	269.39	1-1-1-1	86.00	3-3-3-3	286.84	3-3-1-1	381.58	
2	3-3-1-4	271.08	1-1-1-3	94.70	3-3-3-4	288.06	3-3-1-3	397.68	
3	3-3-1-3	271.33	3-1-1-1	98.36	3-3-3-1	288.14	3-3-1-4	400.05	
4	1-3-1-1	271.39	1-1-1-4	98.75	3-3-1-2	289.79	3-3-1-2	402.15	
5	1-3-3-1	271.49	1-1-1-2	98.80	3-3-3-2	289.88	4-3-1-1	428.03	
6	3-1-3-1	271.74	1-1-3-1	101.79	3-3-4-1	290.04	3-3-2-1	430.08	
7	1-3-1-2	271.83	1-1-2-1	103.60	3-3-4-2	290.46	3-4-1-1	431.56	
8	3-1-1-1	271.84	1-1-4-1	106.66	3-3-2-1	290.57	1-3-1-1	432.70	
9	1-1-1-4	271.88	3-1-1-4	107.24	3-3-4-3	290.66	3-4-1-3	444.18	
10	3-1-1-3	272.01	3-1-1-2	109.80	3-3-1-4	290.73	4-3-1-2	446.13	

^{*} Rule 1 represents CL-FSMCT; rule 2 represents CL-FIFO; rule 3 represents CL-LDF; and rule 4 represents CL-OSA.

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