A VLSI Architecture of DMT Based Transceiver for VDSL System

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ABSTRACT

This paper presents a VLSI architecture of the transceiver for DMT-VDSL system with data rate as high as 52 Mbps. Consisting of four radix-2 stages and three radix2/4/8 stages, a variable length pipelined architecture of FFT/IFFT compatible with 5 modes is proposed to perform the DMT modulation/demodulation. Based on LMS adaptation algorithm, time domain equalizer (TEQ) and frequency domain equalizer (FEQ) are built. The former makes $SSNR > 40dB$ in the steady-state, while the latter performs 11-bit accuracy. Moreover, timing recovery is adopted to compensate $\pm$200ppm symbol rate offset. The RTL simulation shows that the design achieves 52Mbps transmission in short channel model and 16Mbps for long channel environment.

1. INTRODUCTION

Very-high-speed digital subscriber loop (VDSL) serves as the next generation of high-speed networking technology over telephone line infrastructure. Among the modulation schemes considered by the standard bodies, discrete multi-tone (DMT) modulation is the adopted multi-carrier modulation technique that provides spectral compatibility with other DSL services and resilience to fickle channel conditions. Partitioning channels into narrow subchannels, DMT systems offer fine granularity in data rates.

Common cables used in the subscriber loops contain 25 to 100 twisted pairs and suffer from two different types of crosstalk, Near-End Crosstalk (NEXT) and Far-End Crosstalk (FEXT). Besides, the frequency band for VDSL overlaps the bands from amateur radio transmission as well as several other DSL services. The radio frequency interference (RFI) contains ingress and egress issues. The differential mode (DM) strength of the ingress amateur radio noise is -10dBm. Thus, RFI cancellation may be necessary in the digital domain. For RFI egress, the VDSL transmitting power in frequency regions reserved for wireless or radio services must be reduced to 20dB. Thus the notching function is needed to restrict the power level in these regions to no bigger than -80dBm/Hz. At the same time the loop is interfered by multiple AM broadcast services. The AM broadcast sources are modeled by fixed frequency carriers 30% AM modulated with a flat Gaussian noise source band limited to 0~5KHz [4]. In addition, the additive white Gaussian noise (AWGN) has the level of -140dBm/Hz. Fig.1 summarizes these channel factors.

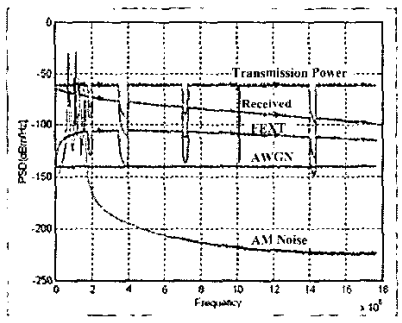

Figure 1: The VDSL transmission environment

In this paper, we present a transceiver architecture for the DMT based VDSL system. The VLSI design of the VDSL transmitter is introduced in Section 2. The design of VDSL receiver is presented in Section 3. The simulation results are shown in Section 4. Finally, the conclusion is drwan in Section 5.

2. TRANSMITTER ARCHITECTURE

Discrete multi-tone (DMT) is considered to be the modulation scheme for VDSL system. The transmission channel will be divided into numbers of sub-channels which the incoming data will be distributed into. Each sub-channel is allocated with the certain number of bits according to its SNR. Each sub-carrier is quadrature amplitude modulated (QAM) to carry the assigned bits. Fig.2 shows the DMT-based VDSL transmitter architecture [5].

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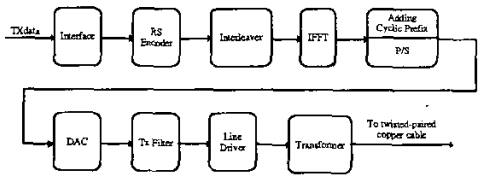

Figure 2: The transmitter architecture of the DMT based VDSL system

The IFFT/FFT processor is the main feature of the transmitter. In a VDSL system, IFFT is used to orthogonally divide the sub-carriers and modulate them with the incoming data, while the FFT with the same structure is for the demodulation. The FFT/IFFT length is different for various loop length and quality-of-service (QoS) and is set up during the initialization. The proposed architecture for 8192-point IFFT/FFT is shown in Fig.3. The VLSI-oriented

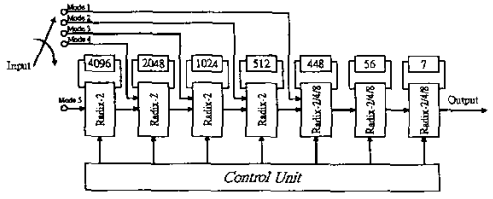

Figure 3: The proposed variable length pipelined FFT/IFFT architecture

FFT algorithm (Radix 2/4/8) [3] is employed to implement the proposed variable length IFFT/FFT architecture. This method takes the advantage of radix-2, radix-2/4 and radix-2/8 that minimize the number of twiddle factor and power consumption. Based on the pipeline technique [6], the series-in series-out feature is used to reduce the number of buffer stages. Moreover, single-path delay feedback (SDF) is employed as the unit blocks for the DMT-based VDSL 8192-point IFFT/FFT module. In order to be compatible with five loop lengths considered, four radix-2 stages and three radix-2/4/8 process elements (PE) are chosen for the implementation.

3. RECEIVER ARCHITECTURE

Fig.4 shows the block diagram of the DMT-based VDSL receiver[5]. It includes the automatic gain control (AGC), the ADC, the TEQ, the FFT, the RFI canceller, the FEQ, the deinterleaver, and the decoder. In the VDSL system, the received signal suffers from severe amplitude attenuation and phase shift due to channel effects. First, the strength of received signal may vary to a large extent for different conditions in term of the loop length of the channel. Variant signal amplitude affects the behavior of the synchronization mechanism in the receiver due to the different loop gain factor. Therefore, the automatic gain control (AGC) in analog front end is employed to compensate this problem. Second, the system requires equalization in both time domain and frequency domain, namely TEQ and FEQ. When the channel impulse response is longer than the cyclic extension, the

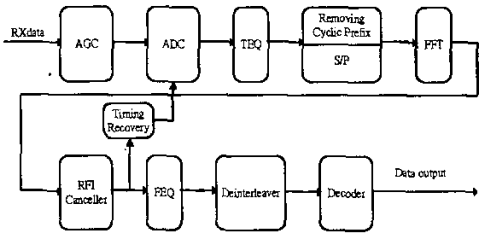

Figure 4: The receiver architecture of the DMT based VDSL system

inter-DMT symbol interference will affect the behavior of the FEQ. TEQ is used to shorten the impulse response of the channel, whereas FEQ is used to compensate the attenuation in each sub-channel. Third, the system requires timing recovery to correct the timing phase. The following illustrates the main functions of the receiver.

3.1 Symbol Synchronization

For a DMT system where the cyclic prefix is employed to avoid ISI, it is important to extract the exact frame of a DMT symbol in order to maintain the orthogonality for the FFT demodulation. Besides, it is also useful for TEQ training. The non-data-aided synchronization method is adopted to detect the DMT-symbol from the received signals. In order to find out the symbol boundary, we can calculate the correlation between the cyclic prefix A and the interval B as shown in Fig.5. With the transmitted signal treated as

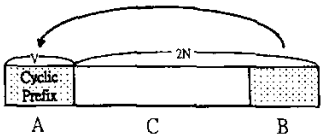

Figure 5: The symbol formate of the DMT-based VDSL system

a wide-sense stationary (WSS) random process, the correlation between period A and B can be utilized by searching the maximum value. This value represents the symbol boundary. The block diagram of the correlation estimator is shown in Fig.6.

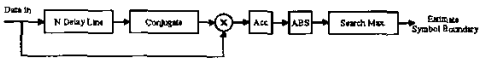

Figure 6: The architecture of the correlation estimator

3.2 Time Domain Equalizer

TEQ is generally designed for two purposes. First, it shortens the impulse response of the channel as mentioned above. Second, the it can be used to partially bandpass the incoming signal and filters out-of-band noise power. TEQ is generally adaptive by nature and its coefficients are trained during initialization. The time domain least-mean square error

(LMS) algorithm is employed since it is an on-line approach suitable for VLSI implementation. The TEQ mechanism is shown in Fig.7 and the equation of the LMS algorithm is derived as

$$y_k = x_k * h_k + n_k \quad (1)$$

$$e_k = b_k * x_k - w_k * y_k \quad (2)$$

$$w_k(n+1) = w_k(n) + \mu \cdot e_k \cdot y_k \quad (3)$$

where x_k and y_k are the transmitted and the received signals, respectively. With the LMS updating step μ_k, the optimal coefficient w_k may be found out in the steady state. The cascade of the TEQ and channel impulse response h_k approximately forms an FIR target impulse response b_k which suffices the orthogonality condition.

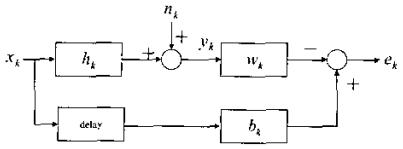

Figure 7: The time domain equalizer of the VDSL system

3.3 Frequency Domain Equalizer

The main goal of FEQ is to compensate the amplitude attenuation and phase shift in frequency domain of the incoming signals due to the effect of the band-limited channel. The architecture of the frequency domain equalizer is shown in Fig.8. Each tone has one adaptive complex tap FEQ. The updating algorithm used in FEQ is also LMS algorithm and derived in the following.

$$Y_k = C_k * X_k \quad (4)$$

$$e_k = \widetilde{Y_k} - Y_k \quad (5)$$

$$C_k(n+1) = C_k(n) + \mu \cdot e_k \cdot X_k \quad (6)$$

Where X_k is the output signal of the FFT, Y_k is the output signal after FEQ, and $\widetilde{Y_k}$ is the output signal of the decision device. C_k is the coefficient of the complex tap and μ is the updating step.

3.4 Timing Recovery Architecture

The closed loop timing recovery has a feedback loop and high jitter performance. Taking the advantage of the phase-locked-loop (PLL), which is composed of a phase detector (PD), a prefilter, a loop filter (LF), and a voltage control oscillator (VCO), the symbol timing error can be estimated and then fed back to the VCO to adjust the sampling instant for the ADC[1]. The proposed timing recovery architecture for DMT based VDSL transceiver is shown in Fig.9. The prefilter is used to improve the timing jitter performance whose bandwidth is 5 to 10 times wider than the bandwidth of the loop filter. Cooperated with the prefilter, the organized architecture of the prefilter and the loop filter performs a second order filter. Tone 64 is selected as pilot tone, which could provide better signal-to-noise ratio (SNR) in general.

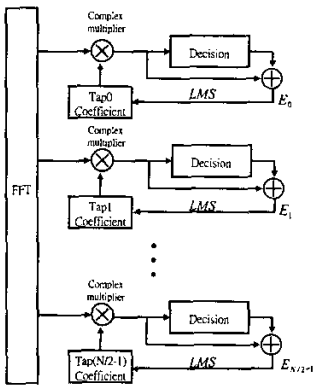

Figure 8: The recovered 512-QAM and 1024-QAM constellations

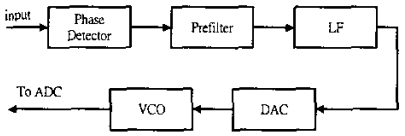

Figure 9: The timing recovery loop of the VDSL system

4. SIMULATION RESULTS

Using Verilog RTL code with long time simulations, the results can fulfill the system requirements. The PSD of the transmitted signals with the amateur radio bands reductions is shown in Fig.1. The simulation result of the symbol synchronization is shown in Fig.10. The tolerance for the timing offset in a VDSL system demanded is ±50ppm; the proposed timing recovery achieves more than ±200ppm locking range, as shown in Fig.11. Fig.12 shows the shortening channel response signal-to-noise-ratio (SSNR) simulation result of the TEQ, as soon as the receiver enters the steady state, the SSNR can be achieved more than 40dB. The Fig.13 shows the original channel and the shortened channel impulse response. Fig.14(a) and Fig.14(b) show the 512-QAM and 1024-QAM constellations for decision in the steady state, respectively. After the simulations, the data rate of the VDSL transceiver system can achieve 52Mbps in the short channel and 16Mbps in the long channel.

5. CONCLUSION

In this paper, the IFFT that is compatible with five modes is proposed. The architecture consists of four radix-2 stages and three radix2/4/8 stages. In the receiver, in order to recover data, the cyclic prefix and one tap FEQ are realized to equalize the data. For long channel that has long impulse response, the TEQ can shorten the channel impulse response so that the performance of BER can be improved. In the timing recovery, a PLL is adopted to provide the compensation ability of ±200ppm symbol rate offset. The data rate can achieve 52Mbps in the short channel with BER less than 10^{-7}. Besides, the TEQ provides more than 40dB of

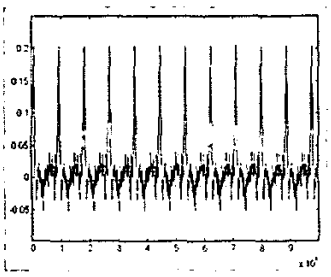

Figure 10: The detection result of the symbol synchronization

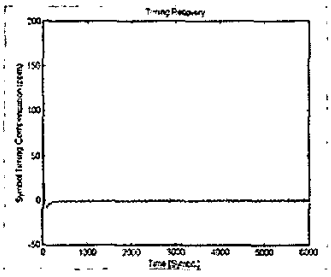

Figure 11: The $+200ppm$ frequency compensation of the timing recovery

the SSNR so that the data rate can achieve 16Mbps in the long channel circumstance.

6. ADDITIONAL AUTHORS

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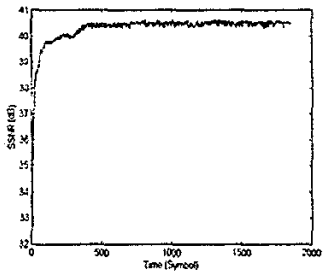


Figure 12: The SSNR performance of the time domain equalizr

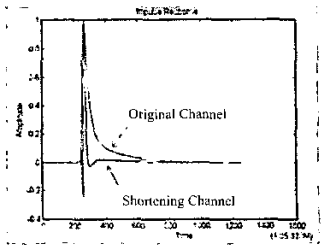
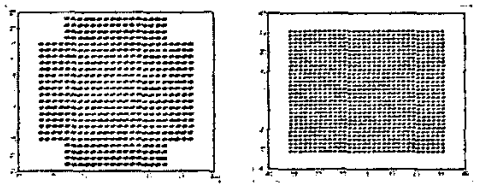


Figure 13: The shortened channel response of the VDSL system



(a) (b)

Figure 14: The recovered 512-QAM and 1024-QAM constellations