ductor optical amplifier can be significantly improved by splitting the contact into two separate contacts. Calculations indicate that 16 dB improvement is possible with 30 dB internal gain. Experimental results using an unoptimised device show a 4 dB improvement in good agreement with the calculated value of 5 dB.

Acknowledgments: We would like to thank H. Nagai of Anritsu Corporation for supplying the optical amplifier. This work was supported by the Australian Telecommunications and Electronics Research Board.

2nd January 1992

R. M. Fortenberry, A. J. Lowery and R. S. Tucker (*Photonics Research Laboratory, Department of Electrical and Electronic Engineering, University of Melbourne, Parkville, Victoria 3052, Australia*)

References

1 GUSTAVSSON, M., KARLSSON, A., and THYLEN, L.: 'Traveling wave semiconductor laser amplifier', *IEEE J. Lightwave Technol.*, 1990, **LT-8**, pp. 610–617

2 FORTENBERRY, R. M., LOWERY, A. J., HA, W. L., and TUCKER, R. S.: 'Photonic packet switch using semiconductor optical amplifier gates', *Electron. Lett.*, 1991, **27**, pp. 1305–1306

3 KOAI, K. T., OLSHANSKY, R., and HILL, P. M.: 'Laser amplifier detector for broadband network control'. Tech. Dig. Topical Meeting on *Optical Amplifiers and their Applications*, Snowmass, CO, 1991, paper WB7

4 IZADPANAH, H., ELREFAIE, A., SESSA, W., LIN, C., TSUJI, S., and INOUE, H.: 'A multi-Gb/s self-synchronized optical regenerator using a 1·55 μm traveling wave semiconductor optical amplifier'. Tech. Dig. topical Meeting on Optical Amplifiers and their Applications, Snowmass, 1991, paper WC5

5 KAMINOW, I. P., and TUCKER, R. S.: Chapter 5 *in* TAMIR, T. (Ed.): 'Guided-wave optoelectronics' (Springer-Verlag, New York, 1988)

6 WAKE, D., JUDGE, S. N., SPOONER, T. P., HARLOW, M. J., DUNCAN, W. J., HENNING, I. D., and O'MAHONY, M. J.: 'Monolithic integration of 1·5 μm optical preamplifier and PIN photodiode with a gain of 20 dB and a bandwidth of 35 GHz'. Postdeadline paper no. PDP18, Conf. on Lasers and Electro-Optics (CLEO), Anaheim, CA, May 1990, pp. 636–637

BiCMOS DYNAMIC MANCHESTER CARRY LOOK AHEAD CIRCUIT FOR HIGH SPEED ARITHMETIC UNIT VLSI

J. B. Kuo, H. J. Liao and H. P. Chen

Indexing terms: Large-scale integration, Integrated circuits

A new BiCMOS dynamic Manchester carry look ahead circuit is presented, which is free from race problems, for VLSI implementation in a high speed arithmetic unit. Using the BiCMOS dynamic Manchester carry look ahead circuit, a 16 bit full adder test circuit which has been designed based on a 2 μm BiCMOS technology, shows a more than two times improvement in speed as compared to the CMOS Manchester carry look ahead circuit. The speed advantage of the BiCMOS dynamic carry look ahead circuit is even greater in a 32 bit or 64 bit adder, which is very helpful for high speed VLSI CPU designs.

Introduction: A CMOS Manchester adder based on precharge/discharge dynamic techniques [1], provides speed and density advantages over static adders for VLSI implementation of arithmetic circuits. The speed performance of the CMOS dynamic Manchester adder is mainly determined by the pass-transistor-related ripple-carry propagation delay [2]. For a large scale arithmetic circuit, this pass-transistor-related ripple-carry propagation delay limits the overall speed performance in an ALU circuit. In addition, extra inverters are needed in the full adder circuit using the Manchester carry look ahead scheme. In this Letter, a faster BiCMOS dynamic carry look ahead circuit, which is built by cascading BiCMOS dynamic logic gates without race problems, is described.

BiCMOS dynamic carry look ahead circuit: Fig. 1 shows the new 4 bit BiCMOS dynamic MCLA circuit in two pairs of *N*- and *P*-type BiCMOS MCLA cells. The output of each BiCMOS MCLA cell, the carry signal, is taken as the input to another cell. To shorten the precharge/predischarge time, BiCMOS precharge/predischarge circuits have been used in every cell. As in a pipelined system, cascading dynamic logic gates may cause serious race problems [3]. In the new BiCMOS dynamic MCLA circuit, race problems have been avoided by placing the 'complementary' BiCMOS dynamic MCLA cells as shown in Fig. 1 alternatively in the MCLA circuit. In the *N*-type cells as shown in Fig. 1, the Bi*p*MOS circuit, which is composed of the bipolar transistor Q_1 and MOS transistors MP_1 and MN_5, has been used as the precharge circuit. In the *N* cell, initially, during the precharge period as defined by the CK signal, the output node is precharged to a high voltage, close to 5 V. During the precharge period, the pull-down bipolar transistor Q_2 is turned off by turning on the MOS transistor MN_4. A logic evaluation period follows the precharge period. During this period, the Bi*p*MOS precharge circuit is turned off and the output voltage is determined by the Bi*n*MOS logic gate including the MOS transistors MN_1, MN_2, MN_3 and the bipolar transistor Q_2. As shown in Fig. 1, the *P*-type cell has a complementary characteristic. During the predischarge period, its output node is discharged to close to 0 V by the Bi*n*MOS predischarge circuit. During the logic evaluation period, the output is determined by the Bi*p*MOS logic gate. To avoid race problems, in each *N* or *P* cell, one transition state is prohibited at the input. Specifically, in the *N* cell, inputs cannot have a transition state from 5 to 0 V because the output may be accidentally switched to an incorrect state. In the *N* cell, after the precharge period, the output is set high. During the logic evaluation period, if inputs A and B are low and input C is initially high, the output node is discharged via the Bi*n*MOS logic gate. After C settles to its logic level −0 V, the output voltage may be already at a low state. Because it is a dynamic circuit, the output cannot be pulled high again at this moment. An error state is thus created. Similarly, in the *P* cell, inputs cannot have a transition state from 0 to 5 V. In addition, the *N* and *P* cells are placed alternatively in the BiCMOS dynamic MCLA circuit such that the output of an *N*(*P*)-cell and is also the input to a *P*(*N*)-cell. After the precharge/predischarge period, in the BiCMOS dynamic MCLA, each internal output node is set high and low alternatively. With this arrangement, race problems are successfully avoided in our circuit.

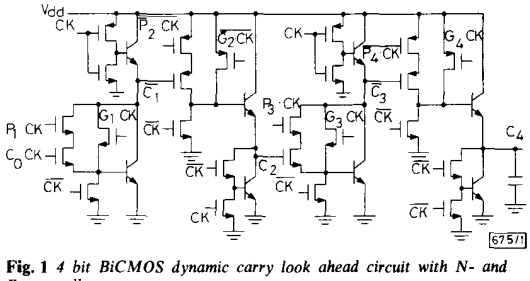

Fig. 1 *4 bit BiCMOS dynamic carry look ahead circuit with N- and P-type cells*

Speed performance and discussion: To evaluate the performance of the BiCMOS dynamic MCLA circuit, a test chip including two 16 bit full adders using the BiCMOS and CMOS dynamic MCLA circuits has been designed based on a 2 μm BiCMOS technology. Fig. 2 shows the layout of two 16 bit full adders using CMOS and BiCMOS dynamic MCLA circuits. As shown in the centre region of both test chips, the 16 bit BiCMOS dynamic MCLA circuit occupies an area of 184 × 713 μm^2, which is about 30% larger as compared to the CMOS circuit, which has an area of 219 × 459 μm^2. Fig. 3 shows the transient waveforms of the carry signals C_4, C_8, C_{12} and C_{16} in the 16 bit CMOS and BiCMOS dynamic

MCLA circuits with an output capacitance of 0·01 pF. As indicated in the Figure, the propagation delay C_{16} associated with the longest critical path in the BiCMOS dynamic MCLA

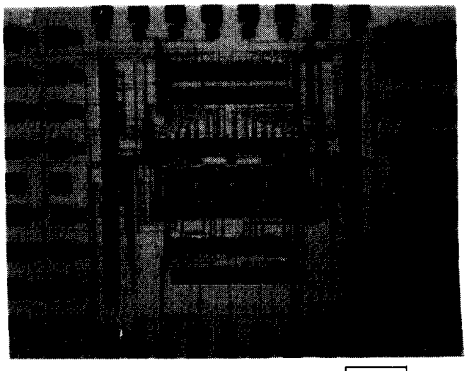

Fig. 2 *Layout of 16 bit CMOS and BiCMOS full adders using CMOS and BiCMOS dynamic carry look ahead circuits*

circuit is less than 20 ns, which is more than twice the speed of the CMOS dynamic MCLA circuit (42 ns). Fig. 4 shows the propagation delay in the longest critical path against bit number of the CMOS and BiCMOS dynamic MCLA circuits. In a CMOS MCLA circuit, the propagation delay is linearly proportional to the bit number. Specifically, in a CMOS MCLA circuit, the propagation delay increases from 42 ns at 16 bit to over 160 ns at 64 bit. On the other hand, in a BiCMOS MCLA circuit, the propagation delay increases more slowly as the bit number increases. Specifically, in a BiCMOS MCLA circuit, the propagation delay increases from 20 ns at 16 bit to 50 ns at 64 bit. Although the integration size increases four times, the propagation delay increases only 2·5 times in the BiCMOS MCLA circuit. In fact, for 4 bit or 8 bit applications, the difference in the propagation delay between the BiCMOS and CMOS MCLA circuits is small. For large scale applications, the BiCMOS MCLA circuit shows an absolute advantage in speed performance. The propagation delay of the 64 bit BiCMOS MCLA circuit is more than three times shorter than the CMOS circuit. In fact, the dynamic BiCMOS techniques described in this Letter are applicable not just to MCLA circuits; they can be used in any large scale pipelined system implemented by CMOS dynamic circuits to enhance the speed performance at a cost of two extra bipolar transistors per stage, one bipolar transistor is for the precharge/predischarge and the other is for the logic gate.

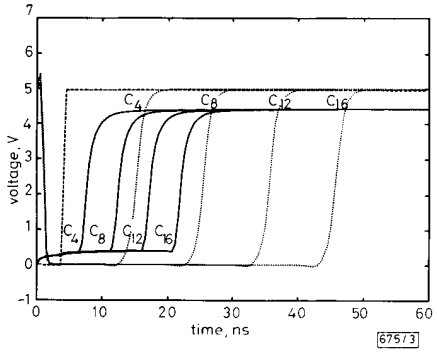

Fig. 3 *Transients of 16 bit carry look ahead circuit using BiCMOS circuit techniques*

——— BiCMOS
····· CMOS
– – – – clock

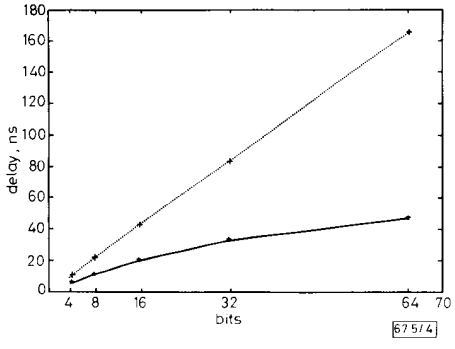

Fig. 4 *Propagation delay of longest critical path against bit number of CMOS and BiCMOS dynamic MCLA circuits*

* BiCMOS MCLA
\+ CMOS MCLA

23rd December 1991

J. B. Kuo, H. J. Liao and H. P. Chen (*Department of Electrical Eng., National Taiwan University, Rm. 526, #1, Roosevelt Rd., Sec. 4, Taipei 107, Taiwan*)

References

1 WESTE, N., and ESHRAGHIAN, K.: 'Principles of CMOS VLSI design: a system perspective' (Addison-Wesley, 1985), pp. 322–326
2 CHAN, P., and SCHLAG, M.: 'Analysis and design of CMOS Manchester adders with variable carry-skip', *IEEE Trans.*, 1990, **C-8**
3 GONCALVES, N., *et al.*: 'NORA: A racefree dynamic CMOS technique for pipeline logic structures', *IEEE J. Solid-State Circuits*, 1983, **SSC-6**, pp. 261–266

COST-EFFICIENT CONTROLLER FOR ROBOTIC MANIPULATOR

S. Szumko and I. P. W. Sillitoe

Indexing terms: Automata theory, Control systems

A new method based on disturbance attenuation is developed for enabling a manipulator to follow a given path. Its main advantage is the reduction of computation when compared with established techniques such as the computed torque control. This is achieved by regarding the effects of certain components of the dynamics as disturbances. Its effectiveness is illustrated using a simulation for a six degree of freedom industrial robot.

Introduction: The motion of a manipulator with six degrees of freedom may approximately be described by a dynamic equation in configuration space as [1]

$$\ddot{\theta} = M^{-1}(\theta)\{\tau - B(\theta)[\dot{\theta}\dot{\theta}] - C(\theta)[\dot{\theta}^2] - G(\theta)] \quad (1)$$

where, in this example, $\theta = [\theta_1, \theta_2, \theta_3, \theta_4, \theta_5, \theta_6]^T$ is the vector of joint angles, τ is the 6×1 vector of joint input torques, $M(\theta)$ is the 6×6 mass matrix, $B(\theta)$ the 6×15 Coriolis matrix, $C(\theta)$ the 6×6 centrifugal matrix, and $G(\theta)$ the 6×1 gravity vector. Quantities $[\dot{\theta}\dot{\theta}]$ and $[\dot{\theta}^2]$ are given by

$$[\dot{\theta}\dot{\theta}] = [\dot{\theta}_1\dot{\theta}_2, \dot{\theta}_1\dot{\theta}_3, \ldots, \dot{\theta}_5\dot{\theta}_6]^T$$
$$[\dot{\theta}^2] = [\dot{\theta}_1^2, \dot{\theta}_2^2, \dot{\theta}_3^2, \dot{\theta}_4^2, \dot{\theta}_5^2, \dot{\theta}_6^2]^T$$

A common method of control used to track a given 6×1 position demand vector θ_d is the so called computed torque method [2], where if $E = \theta_d - \theta$ is the error then τ defined by eqn. 2

$$\tau' = \ddot{\theta}_d + K_v\dot{E} + K_pE \quad (2a)$$