

Amorphous silicon TFT capacitance model using an effective temperature approach

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Indexing terms: Silicon, Thin film transistors, Amorphous semiconductors

An analytical capacitance model for a-Si:H thin film transistors, that considers deep and tail states simultaneously, is presented. Using an effective temperature approach and a charge-oriented concept, the localised deep and tail states have been considered in the capacitance model. As verified by the published data, this analytical capacitance model provides an accurate prediction of the C-V characteristics of an a-Si:H thin film transistor.

Introduction: Hydrogenated amorphous thin film transistors (a-Si:H TFTs) have been used for active matrix LCDs, complex arrays of electronic devices and large-area microelectronics using amorphous material [1]. To facilitate circuit design for a-Si:H digital control circuits, effective device models for a-Si:H TFTs are important. To date, DC models for a-Si:H TFTs have been reported [2-6]. However, for transient analysis, a capacitance model as for a typical MOS device as shown in Fig. 1 [7, 8] is important. Owing to the complicated distribution of localised acceptor states in the energy gap of amorphous silicon, an analytical capacitance model is difficult to obtain because analytical models of the free and trapped charges in the channel of the a-Si:H TFT are difficult to obtain. Shur *et al.* [9, 10] reported a capacitance model for a-Si:H TFTs based on field-dependent mobility. Neudeck *et al.* [11] developed a capacitance model but numerical iteration is required. In this Letter, using an effective temperature approach and charge-oriented concept, both deep and tail states can be included in deriving the analytical capacitance model in a simple way.

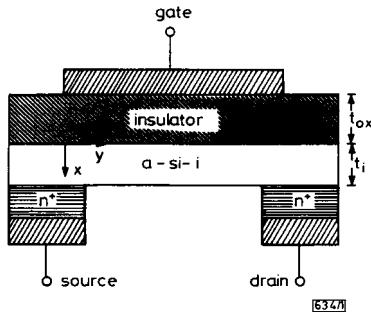


Fig. 1 Capacitance model of a-Si:H TFT

Model derivation: Consider a typical a-Si:H TFT with its cross-section as shown in Fig. 2. The source charge and the drain charge are as shown in eqns. 1 and 2 in Appendix 1. The total induced charge Q_g at the gate is given by eqn. 3. N_{free} and N_{total} can be derived using an effective temperature approach [6]. The localised trapped charge density in a-Si:H can be computed by considering the distribution of localised acceptor states as shown in eqns. 4 and 5. Applying the Poisson equation in the a-Si:H TFT and using the relationship: $2d\psi/dx(d^2\psi/dx^2) = d/dx(d\psi/dx)^2$, the electric field is expressed by eqn. 6. By integrating the free carrier density in the vertical direction of the a-Si:H TFT from the oxide/a-Si interface ($x = 0$) to the end of the channel in the a-Si thin film ($x = t$), the total free carriers in the a-Si:H TFT can be obtained as shown in eqn. 7. Applying the Gauss law at the oxide/a-Si interface and considering the voltage drop in the oxide region, the transport current can be expressed by eqn. 8. The drain charge and the gate charge are described by eqns. 9 and 10, respectively. Therefore, the gate-to-drain capacitance C_{gd} can be expressed as the sum of the gate-to-drain overlapped capacitance and the intrinsic gate-to-drain capacitance (similarly for the drain-to-gate capacitance) as shown below

$$C_{gd} = C_{gdo} + C_{gdi} = C_{gdo} + \partial Q_g / \partial V_{ds}, \quad C_{dg} = C_{dgo} + C_{dgi} = C_{dgo} + \partial Q_d / \partial V_g.$$

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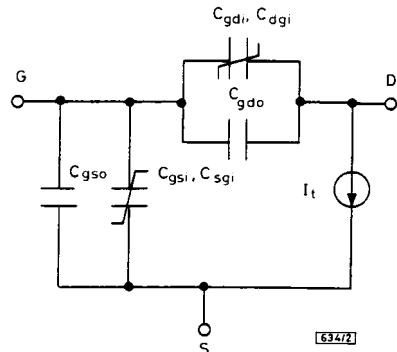


Fig. 2 Cross-section of typical a-Si:H thin film transistor

Comparison with experiment data: To verify the analytical capacitance model using the effective temperature approach, an a-Si:H TFT with a channel length of 7 μm and a channel width 150 μm has been used in the study. The a-Si:H TFT has an a-Si thin film of 500 Å and a gate oxide of 3000 Å. The band mobility μ_b is 13.5 cm²/Vs. The effective density of states (N_e) is 5×10^{18} cm⁻³. Fig. 3a and b show the C_{gd} against V_{ds} characteristics of the a-Si:H TFT biased at $V_g = 0, 5, 10, 15$ V, based on the analytical model using the effective temperature approach and the published data [10]. A close fit between the model results and the published data can be observed.

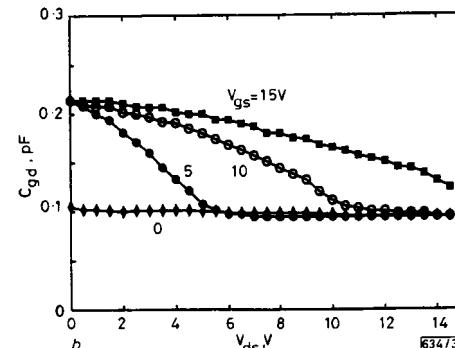
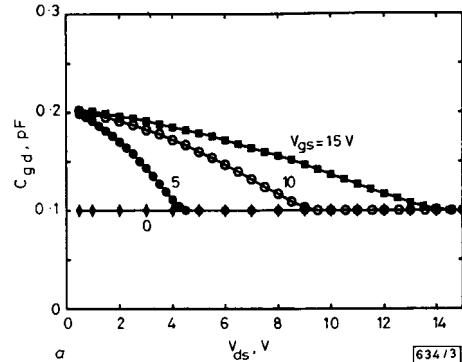


Fig. 3 C_{gd} against V_{ds} of a-Si:H TFT for $V_{gs} = 0, 5, 10, 15$ V

a Model results
b Experimental data

From the analytical model derived in the previous sections, the differences between the a-Si:H TFT and single-crystalline MOSFET come from the trapped charges. If no trapped charges exist ($g_d = 0, g_i = 0$), the analytical a-Si:H TFT capacitance model becomes the typical formula as for single-crystalline MOSFETs.

Neglecting trapped charges, the effective temperature at the oxide/a-Si interface becomes $T_{eq} = 2T$. From eqns. 9–11, C_{gdi} and C_{gdo} become as for conventional MOS devices.

Appendix 1: Important equations:

$$Q_s = qW \int_0^L \left(1 - \frac{y}{L}\right) N_{total}(y) dy \quad (1)$$

$$Q_d = \frac{qW}{L} \int_0^L y N_{total}(y) dy \quad (2)$$

$$Q_g = -(Q_s + Q_d) = -\frac{qW}{L} \int_0^L N_{total}(y) dy \quad (3)$$

$$g(E) = g_d e^{\frac{q\Psi - E_{f_d}}{kT_d}} + g_t e^{\frac{q\Psi - E_{f_t}}{kT_t}} \quad (4)$$

$$\begin{aligned} n_{loc} = & \left(g_d k T_d - \frac{g_d}{(\frac{1}{kT} + \frac{1}{kT_d})} + \frac{g_d}{(\frac{1}{kT} - \frac{1}{kT_d})} \right) e^{\frac{q\Psi - E_{f_d}}{kT_d}} \\ & + \left(g_t k T_t - \frac{g_t}{(\frac{1}{kT} + \frac{1}{kT_t})} - \frac{g_t}{(\frac{1}{kT} - \frac{1}{kT_t})} \right) e^{\frac{q\Psi - E_{f_t}}{kT_t}} \\ & + \left(g_t \frac{1}{(\frac{1}{kT_t} - \frac{1}{kT})} - \frac{g_d}{(\frac{1}{kT} - \frac{1}{kT_d})} \right) e^{\frac{q\Psi - E_{f_d}}{kT}} \end{aligned} \quad (5)$$

$$E(\Psi) = \sqrt{\frac{2}{\epsilon} \left(k T_d n_A e^{\frac{q\Psi - E_{f_d}}{kT_d}} + k T_t n_B e^{\frac{q\Psi - E_{f_t}}{kT_t}} + k T n_C e^{\frac{q\Psi - E_{f_o}}{kT}} \right)} \quad (6)$$

$$\begin{aligned} n_A &= g_d k T_d - \frac{g_d}{(\frac{1}{kT} + \frac{1}{kT_d})} + \frac{g_d}{(\frac{1}{kT} - \frac{1}{kT_d})} \\ n_B &= g_t k T_t - \frac{g_t}{(\frac{1}{kT} + \frac{1}{kT_t})} - \frac{g_t}{(\frac{1}{kT} - \frac{1}{kT_t})} \\ n_C &= g_d \frac{1}{(\frac{1}{kT_d} - \frac{1}{kT})} + g_t \frac{1}{(\frac{1}{kT_t} - \frac{1}{kT})} + N_c \\ N_{free} &= \frac{N_c}{qA} \frac{1}{(\frac{1}{kT} - \frac{1}{kT_{ef}(\Psi_s)})} e^{(q\Psi_s - E_{f_o})(\frac{1}{kT} - \frac{1}{kT_{ef}(\Psi_s)})} \end{aligned} \quad (7)$$

$$\begin{aligned} I_T &= \frac{W}{L} \mu_o \frac{N_c}{A(\frac{1}{kT} - \frac{1}{kT_{ef}})} \left(\frac{C_{ox}}{\epsilon A} \right)^{\frac{T_{ef}}{T} - 1} \\ &\times \frac{T}{T_{ef}} \left((V_{gs} - V_{fb})^{\frac{T_{ef}}{T}} - (V_{gd} - V_{fb})^{\frac{T_{ef}}{T}} \right) \end{aligned} \quad (8)$$

$$\begin{aligned} Q_g &= -WLC_{ox} \frac{T_{ef}/T}{1 + T_{ef}/T} \\ &\times \frac{(V_g - V_{fb} - V_s)^{\frac{T_{ef}}{T} + 1} - (V_g - V_{fb} - V_d)^{\frac{T_{ef}}{T} + 1}}{(V_g - V_{fb} - V_s)^{\frac{T_{ef}}{T}} - (V_g - V_{fb} - V_d)^{\frac{T_{ef}}{T}}} \end{aligned} \quad (9)$$

$$Q_d = \frac{qW}{LI_T^2} \int_{V_s}^{V_d} N_{total} q^2 W^2 \mu_o^2 N_{free} \int_{V_s}^{\Psi_s} N_{free} d\Psi_s d\Psi_d \quad (10)$$

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Cryogenic investigation of gate leakage and RF performances down to 50K of 0.2μm AlInAs/GaInAs/InP HEMTs

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0.2μm Al_{0.48}In_{0.52}As/ Ga_{0.47}In_{0.53}As LMHEMT on InP with an undoped GaInAs layer to reduce gate leakage have been realised and their DC and RF properties have been investigated at cryogenic temperatures. The cutoff maximum frequencies of oscillation F_{max} up to 260Hz are extrapolated at 50K from the maximum unilateral gain (MUG) determined using S parameters measured up to 40GHz. Evolution of gate leakage current and RF characteristics against gate and drain biases are presented between 50 and 300K.

The cryogenic RF study of 0.2μm gated HEMTs on InP bonded on chip carriers has been reported up to ~10–12GHz [1]. We present an investigation down to 50K of lattice matched HEMTs on InP, with direct on-wafer coplanar S parameter measurements up to 40GHz. The heterostructure grown by MBE (Fig. 1) consists of a 2500Å Al_{0.48}In_{0.52}As buffer layer, a 300Å n.i.d. Al_{0.47}In_{0.53}As channel, a 30Å AlInAs spacer, 60Å heavily Si doped (10¹⁸cm⁻³) AlInAs layer, a 100Å n.i.d. AlInAs layer, followed by a 50Å n.i.d. GaInAs layer to reduce gate leakage currents and gate capacitances and a 100Å Si doped (2.10¹⁸cm⁻³) GaInAs cap layer. A mixed and matched process is applied in the HEMT fabrication. Electrode pads and mesa area are patterned optically, and the gate is e-beam patterned with JEOL JBX5DII.

The shift in threshold voltage (300K–50K) is less than 0.1V ($V_{th} = -1.6$ V). The structure has good breakdown characteristics shown by intensive RF testing up to $V_d = 4$ V without failure. The maximum intrinsic transconductance $G_{m,max}$ which is obtained at $V_{gs} \approx -0.5$ V and low $V_d \approx 0.6$ V rises from 500mS/mm at 300K to 690mS/mm at 50K. The corresponding gate leakage current I_{gn} which at low V_d is essentially tunnelling current, decreases in this temperature range from 8 to 4μA/mm. These values are much smaller than in conventional InP HEMTs with same gate length. Fig. 2 shows that at higher V_d (> 1.4V) another gate current component appears in the pinch-off region which is currently associated with impact ionisation [2]. We observe a peak, the amplitude