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A 1.8V 2.5-5.2 GHz CMOS Dual-input Two-stage Ring VCO

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ABSTRACT

A 1.8V 2.5-to-5.2 GHz dual-input two-stage CMOS voltage-controlled ring oscillator (VCO) is presented. A novel delay cell used for the two-stage ring VCO is proposed to achieve low power dissipation and better phase noise performance. The delay cell adopts both inductive-peaking and shunt-shunt feedback circuit techniques to obtain high gain and wide. Implemented in a 0.18μm CMOS technology using 1.8V supply voltage, the VCO has a wide operating frequency range from 2.5GHz to 5.2GHz with coarse-tune VCO gain of 4.75GHz/V and fine-tune VCO gain of 80MHz/V. At 3.6GHz, the phase noise of the VCO is -90.1dBc/Hz at 1MHz frequency offset with low power consumption of 17mW. Because of the two-stage ring topology, the VCO can provide quadrature outputs. The total chip area is 0.4mm x 0.6mm.

1. INTRODUCTION

Voltage-controlled oscillators (VCOs) are critical building blocks in phase-locked loops (PLLs) and clock and data recovery circuits (CDRs), which are widely used in wireless and wire-line communication systems. Designing VCOs for monolithic integration is always desirable but most challenging. It has to achieve high-frequency operation with reasonable power consumption. In addition, the phase noise performance is also important. Finally, small chip area is essential to monolithic system integration.

In recent years, the CMOS LC-tank oscillators have shown an excellent phase noise performance with low power consumption because of a relatively high quality factor. However, the limited tuning range and large chip area have become critical drawbacks in LC VCOs. On the other hand, the ring VCOs exhibit several attractive features such as the wide frequency tuning range, the ease of integration with digital CMOS process, and the small chip area. Moreover, ring oscillators generate both in-phase and quadrature-phase outputs with an even number of delay cells.

The oscillation frequency of the ring oscillator is inversely proportional to the number of delay stages N. Employing fewer delay stages can also reduce the power dissipation, chip area and cost. The minimum number of stages for quadrature outputs is N = 2. Hence it is desirable to design a two-stage ring VCO. However, in order to satisfy Barkhausen's criteria, an additional phase shift is required in each delay cell.

Several novel delay cells have been proposed to compose the two-stage ring VCO [1][2], but much extra power is needed to provide an excess phase shift. The circuit described in [3] can achieve low power design, however the output signal swing is reduced in order to place the complex poles in front of the zero. Consequently, the phase noise performance of this two-stage ring VCO is relatively poor. In the following, a 1.8V 2.5-to-5.2GHz dual-input two-stage ring VCO is presented. It will show that the two-stage ring VCO possesses many attractive features such as low power dissipation, large output signal swing, and wide tuning range.

The structure of this paper is as follows. In Section 2, the proposed delay cell is discussed. In Section 3 we then describe the complete two-stage ring VCO. The experimental results are shown in Section 4. Finally, a conclusion is given in Section 5.

2. SHUNT-SHUNT FEEDBACK DELAY CELL

The circuit schematic of the proposed delay cell is depicted in Fig. 1. The excess phase shift is provided by the shunt-shunt feedback configuration including M3 to

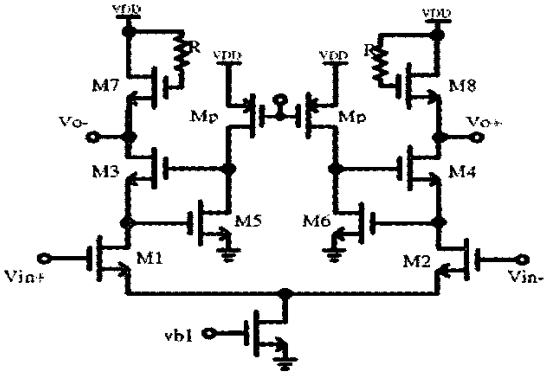

Fig. 1. Proposed delay cell

M6. Therefore, the loading device, containing a resistor and a NMOS, can be designed to exhibit the property of inductive peaking so that the ac small signal gain at the oscillation frequency and the output signal swing can be boosted. Although the total power dissipation seems to be increased due to the addition of two more current paths which are composed of M5, M6 and Mp's, the property of shunt-shunt feedback makes the required dc current associated with these two paths very small compared to that of the main signal paths.

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It is necessary to know the location of poles contributed by the shunt-shunt feedback configuration because it determines the amount of excess phase shift and hence the oscillation frequency. The circuit diagram and the corresponding small signal model shown in Fig.2 can be used to derive the location of poles in the

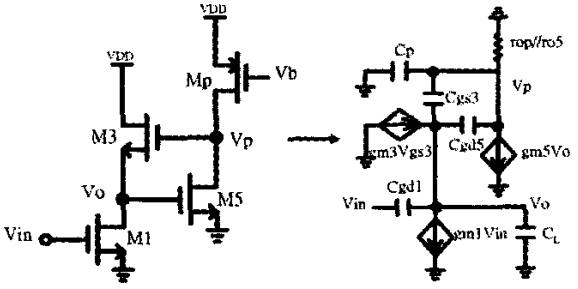

Fig. 2. Circuit diagram used to determine the poles in the feedback loop

feedback loop. By listing node equations, the transfer function from Vin to Vo can be derived as

$$F(s)=\frac{-(g_{m1}-sC_{gd})\cdot(1+s(C_p+C_1))}{s^2[(C_L+C_1)\cdot(C_p+C_1)-C_1^2)r_{op}]+s[(g_{m5}C_p+g_{m5}C_1)r_{op}]+g_{m5}(1+g_{m5}r_{op})} \quad (1)$$

where $g_m r_{op} >> 1$ is assumed.

It can be observed from equation (1) that the location of the poles associated with the feedback loop can be very far without consuming much power due to the nature of the shunt-shunt feedback.

The overall transfer function T(s) from the input to the output of the delay cell can be expressed as the product of two transfer functions $T_1(s)$ and $T_2(s)$, where $T_1(s)$ represents the part of overall transfer function providing an excess phase shift and $T_2(s)$ explains the inductive-peaking behavior resulting from the loading devices.

$$T(s) = \frac{v_o}{v_{in}} = -T_1(s)\cdot T_2(s) \quad (2)$$

$$T_1(s)=\frac{g_{m5}r_{op}\cdot((g_{m5}+\frac{1}{r_{op}})+sC_p)}{s^2[(C_q+C_{gd}+C_1)\cdot(C_p+C_1)-C_1^2)r_{op}]+s[(g_{m5}C_p+g_{m5}C_1)r_{op}]+g_{m5}(1+g_{m5}r_{op})} \quad (3)$$

$$T_2(s) = \frac{(1+C_{gs8}Rs)}{s^2C_{gs8}C_LR+s(C_L+C_{gs8})+g_{m8}} \quad (4)$$

3. TWO-STAGE RING VCO

The tuning method adopted in this two-stage ring VCO is the delay interpolation tuning as shown in Fig. 3. This tuning method can achieve wide tuning range and relatively linear voltage-to-frequency characteristic. In

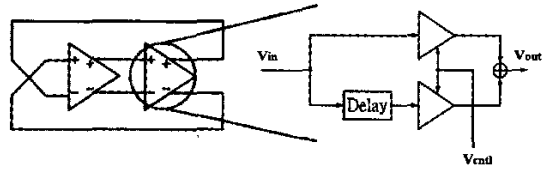

Fig. 3. Interpolation Tuning

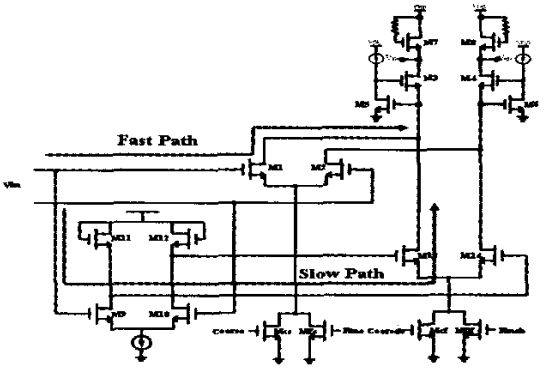

Fig. 4. Delay interpolation delay cell

addition, it is suitable for the fully differential operation in which the control lines of the VCO are also differential.

The circuit schematic of the complete delay stage is shown in Fig.4. The delay block shown in Fig.3 is implemented by M9 through M12. The fast and slow paths share the shunt-shunt feedback loop consisting of M3 to M6 and the inductive peaking loading devices containing M7, M8 and resistors. It should be noted that with the purpose of achieving both low jitter and wide capture range performance, modern PLLs and CDRs frequently use dual-loop architectures[4][5]. Hence the dual-input VCO is often desired. In order to decompose the VCO control line into coarse and fine tune inputs, the MOSs which are used to provide the tail current in each path are decomposed to two parallel MOSs. One is controlled by the fine tune input while the other is controlled by the coarse tune input. Finally, the current folding circuit [6] shown in Fig. 5 is used to alleviate the issue of limited voltage headroom. The current variation is performed through mirror arrangements driven by PMOS differential pairs M1-M2 and M3-M4.

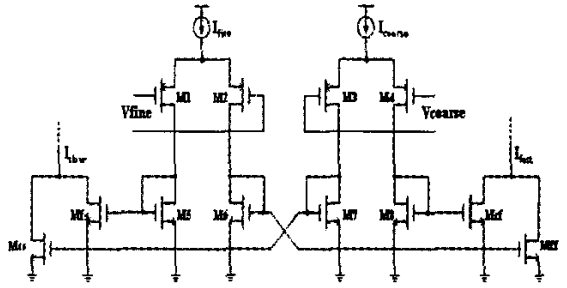

Fig. 5. Current folding circuit

4. EXPERIMENTAL RESULTS

The two-stage ring VCO is fabricated using 0.18 μm CMOS technology and the chip photo is shown in Fig.6. The VCO covers 0.6 x 0.4 mm^2 chip area. The external components in the testing board include a variable resistor, and some decoupling capacitors. The measured transfer characteristics of the VCO are shown in Fig.7

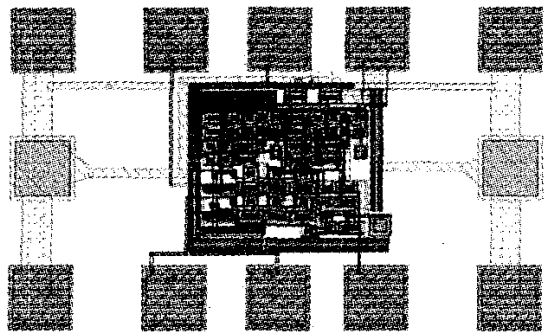

Fig. 6. Die photo of VCO

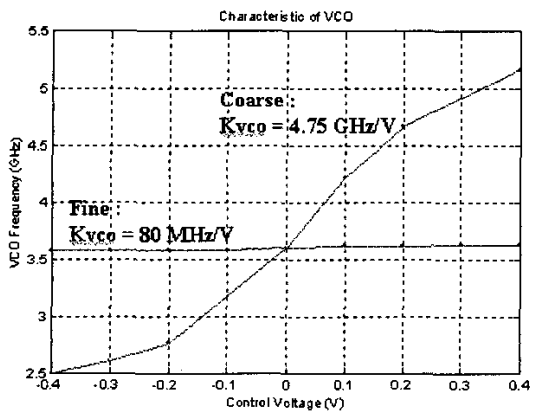

Fig. 7. Transfer characteristics of VCO

for both coarse and fine tuning. It can be seen that the gain of the coarse-tune control input is 4.75GHz/V, which is large enough to encompass process and temperature variations. On the other hand, the gain of the VCO with respect to the fine-tune control input is only 80MHz/V, which is quite small in order to reduce the VCO output jitter. The VCO has a wide operating frequency range from 2.5GHz to 5.2GHz which can be used in many applications. The overall tuning range of this two-stage ring VCO is about 74%..

Finally, the phase noise performance of the free-running two-stage VCO is measured as shown in fig.8.

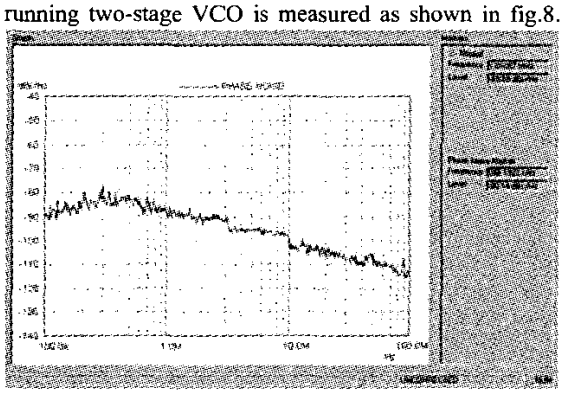

Fig. 8. Phase noise of VCO

Measured at 3.6GHz, it shows that the phase noise of the VCO is -90.1dBc/Hz at 1MHz frequency offset. The total power consumption of the two-stage ring VCO is only 17mW under 1.8V supply voltage.

The performance summary of the dual-input two-stage ring VCO is listed in Table 1.

Oscillator Type	Two stage ring VCO
Center Frequency	3.6 GHz
Tuning Range	74% 4.75GHz/V, 80MHz/V
Phase Noise	-90.1dBc/Hz @1MHz offset
I & Q Output	Yes
Power Dissipation	17mW
Chip Area	0.6mm x 0.4mm
Technology	CMOS 0.18 μ m with 1.8V supply voltage

Table 1. Performance summary

In order to evaluate the performance of different ring oscillator topologies, a figure of merit (FoM) provided by [7] is used to compare different designs. The performance comparison results are given in Table 2. It can be seen that the two-stage ring VCO presented here has better FoM compared to [8]-[10] and has the same FoM with the design in [6]. However, the supply voltage of our design is only 1.8V while the supply voltage in [6] has to be boosted to 2.5V to guarantee correct operation.

5. CONCLUSION

In this paper, a 1.8V 2.5-to-5.2GHz dual-input two-stage CMOS ring VCO is presented. A delay cell used in VCO adopts both inductive-peaking and shunt-shunt feedback circuit techniques to attain high gain, low power and wide bandwidth performance. By using interpolation tuning method, the VCO has a wide operating range of 74% with coarse-tune VCO gain of 4.75GHz/V and fine-tune VCO gain of 80MHz/V. At 3.6GHz, the phase noise of the VCO is -90.1dBc/Hz at 1MHz frequency offset. The two-stage ring VCO as presented in this paper occupies a 0.6mm x 0.4mm chip area in a 0.18μm 1P6M CMOS technology. The total power consumption of this chip is only 17mW under a 1.8V supply voltage.

	Proposed VCO	[6]	[8]	[9]	[10]
Center Frequency	3.6GHz	5GHz	5GHz	5GHz	1.56GHz
Tuning Range	74%	54%	24%	130%	12%
Phase Noise @ 1MHz offset	-90.1dBc/Hz	-88.2dBc/Hz	-88.3dBc/Hz	-82dBc/Hz	-97.4dBc/Hz
Supply Voltage	1.8	2.5	1.8	1.8	1.8
Power Dissipation	17mW	21mW	30.6mW	135mW	48.2mW
Technology	CMOS 0.18um	CMOS 0.18um	CMOS 0.18um	CMOS 0.18um	CMOS 0.18um
FoM	178.9	178.9	177.4	164.7	174.4

Table 2. Performance comparison

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