Analysis and Design for Asymmetrical Half-Bridge Forward Mode Converters

Yi-Hsin Leu, Chern-Lin Chen, *Member, IEEE*, and Tso-Min Chen

***Abstract*--Efficiency and soft-switching phenomena of asymmetrical half-bridge forward mode converters are seriously affected by circuit parameters. The design trade-off between the leakage and magnetizing inductance for practical applications is presented. The ZVS condition, duty cycle loss and hold-up time etc are utilized for deriving the optimal design rules. Experimental verification on a 5V/20A prototype is conducted and 86% efficiency is achieved.**

***Index Terms*—zero voltage switching, DC to DC converter, asymmetrical half- bridge converter.**

I. Introduction

IN traditional switched-mode power supplies, hard switching is detrimental to high-frequency operation, electromagnetic interference, and efficiency. Utilizing soft-switching technique, the switching loss can be eliminated. Voltage and current surge can also be minimized to allow high frequency operation. A ZVS-PWM converter operates with zero voltage switching for each switch at a constant frequency by utilizing some parasitic elements such as the junction capacitors, the body diodes of the MOSFETs and the leakage inductor of the transformer.

In recent years, research efforts on high efficient DC/DC converter has resulted in hundreds of literatures and countless topologies. Among them, the asymmetrical half-bridge forward mode converter has attracted a lot of attention for its simplicity and soft-switching performance [1-4]. In the literatures [2-4], the output inductor current i_{Lo} and magnetizing current i_m are often regarded as constant. In practical applications, these currents play a significant role of ZVS operations. In this paper, the variation of i_{Lo} and i_m is taken into account, and the operation principle of the converter is described in detail. Moreover, the design rules of significant circuit parameters for the studied converter can be derived from the ZVS condition, duty cycle loss and hold-up time etc. Finally, experimental results obtained from a prototype converter will be utilized to verify the soft-switching characteristics and design rules.

II. Circuit Description and Operation Analysis

Shown in Fig. 1 is a typical circuit diagram of the asymmetrical half bridge forward mode converter. The active switches Q_1 and Q_2 are driven alternately with a short deadtime interval when both switches are off. The transformer (T) has been replaced with an equivalent circuit showing the leakage and magnetizing inductance (L_l represents the leakage inductor include an additional external inductance and L_m represents the magnetizing inductance). C_1 C_2 and D_1 D_2 are the junction capacitors and the body diodes of the MOSFETs, respectively.

To presume that the circuit operates in CCM, and the capacitance C_b and C_o are large enough that the voltage across it can be regarded as constant. The capacitance C_r represents the equivalent loop-capacitance, which is the combination of the junction capacitance of the switches and the transformer intra-winding capacitance. One complete switching cycle is broken down into eight individual stages and the corresponding equivalent circuits of the converter in each of the topological stages are given in Fig. 2. The operation principle of the converter is described in the following and the key operational waveforms are in Fig. 3.

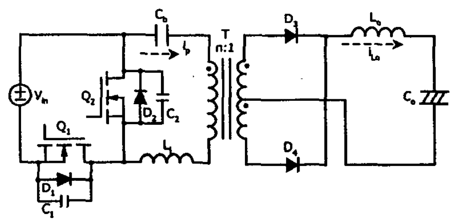

Fig. 1. The Asymmetrical Half-Bridge Forward Mode Converter

a) Stage 1 ($t_0\sim t_1$)

S_1 and D_3 were conducting and S_2 and D_4 were turned off. The reverse voltage across Q_2 is V_{in}. The voltage across transformer primary winding is clamped at V_{in}-V_c. The energy is transferred to the output through the transformer. The primary current is raised to $i_{LO}^+ / n + i_m^+$ linearly.

b) Stage 2 ($t_1\sim t_2$)

After Q_1 is turned off at t_1, primary current i_p is diverted from Q_1 to C_1 and C_2. As the result, the voltage across C_1 (V_{DS}) increases. This stage terminated at t=t_2 when voltage V_{DS} increases to V_{in}-V_c.

c) Stage 3 ($t_2\sim t_3$)

At t=t_2, the transformer primary winding voltage collapses to zero and rectifier diode D_4 starts to conduct. Now inductor L_l and capacitor C_r form a series resonant circuit. The voltage $V_{DS}(t)$ and the primary current $i_p(t)$ are expressed by:

$$i_p(t)=\left(i_m^+ + i_{LO}^+ / n\right)\cdot \cos[\omega_r(t-t_2)] \qquad (1)$$

Yi-Hsin Leu, Chern-Lin Chen, and Tso-Min Chen are with the Electrical Engineering Department, National Taiwan University, Taipei in 106 ROC (e-mail: clchen@cc.ee.ntu.edu.tw)

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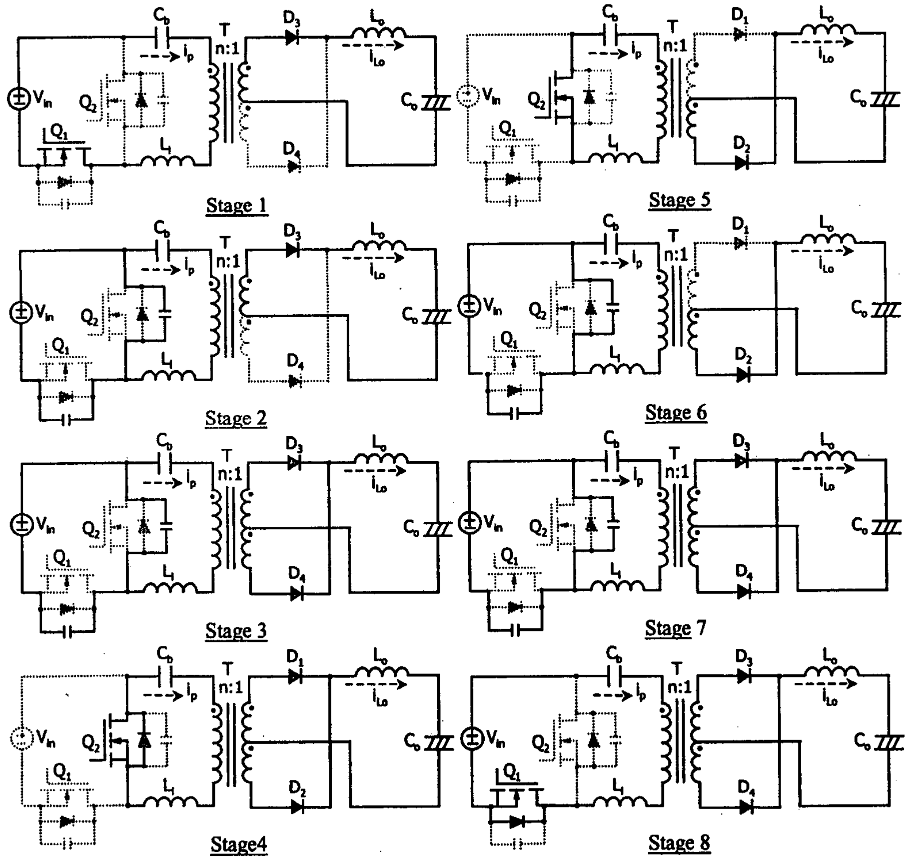

Fig. 2. Converter topological states

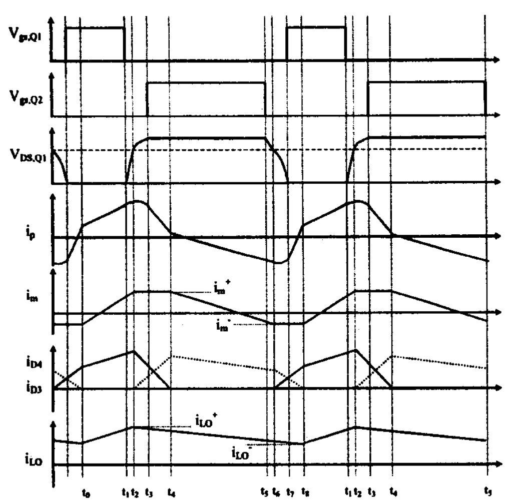

Fig. 3. Key operational waveforms of the converter

$$V_{DS}(t)=V_{in}-V_c+Z_r\left(i_m^+ + i_{LO}^+/n\right)\cdot\sin[\omega_r(t-t_2)] \quad (2)$$

where, $\omega_r = 1/\sqrt{L_l C_r}$, $Z_r=\sqrt{L_l/C_r}$

This stage ends when the voltage V_{DS} increases to V_{in}.

d) Stage 4 ($t_3 \sim t_4$)

At t_3, the voltage V_{DS} is equal to V_{in}, and the anti-parallel diode D_2 starts to conduct. In order to achieve ZVS for Q_2, the device should be turned on before i_p reverses direction. The primary current i_p is ramped down due to the negative voltage $-V_c$ applies to the leakage inductor. It can be found that:

$$i_p(t)=i_p(t_3)-\frac{V_c}{L_l}(t-t_3) \quad (3)$$

When i_p reaches $i_m^+ - (i_{LO}^+/n)$, the diode D_3 turns off. The short-circuited state of the transformer vanishes. The voltage across the L_m raises to $-V_c$. The time interval can be formulated as:

$$t_{43}=\frac{L_l}{V_c}\left[\frac{i_{LO}^+}{n}-i_m^+ + i_p(t_3)\right] \quad (4)$$

where $i_p(t_3)$ is the value of i_p at time t_3.

e) Stage 5 ($t_4 \sim t_5$)

During this interval, the energy is transferred to the load. This stage ends at $t=t_5$ when Q_2 is turned off.

f) Stage 6 ($t_5 \sim t_6$)

At t_5, the switch Q_2 is turned off. The capacitor C_1 and C_2 is charged and discharged by the primary current i_p and the voltage V_{DS} decreases. When the voltage reaches V_{in}-V_c, D_3 starts to conduct, i_{Lo} freewheels through both output rectifier diodes and the transformer voltage collapses to zero again.

g) Stage 7 ($t_6 \sim t_7$)

At t_6, L_l and C_r start to resonate. The voltage $V_{DS}(t)$ and the primary current $i_p(t)$ are described by:

$$i_p(t)=\left(i_m^- - i_{LO}^- / n\right)\cdot\cos[\omega_r(t-t_6)] \tag{5}$$

$$V_{DS}(t)=V_{in}-V_c+Z_r\left(i_m^- - i_{LO}^- / n\right)\cdot\sin[\omega_r(t-t_6)] \tag{6}$$

This stage is terminated at $t=t_7$ when voltage V_{DS} decrease to zero.

h) Stage 8 ($t_7 \sim t_8$)

When V_{DS} reaches zero, D_1 conducts and Q_1 turn on with zero voltage across it. Primary current i_p is ramped up due to the positive voltage V_{in}-V_c applies to the leakage inductor. It can be found that:

$$i_p(t)=i_p(t_7)+\frac{(V_{in}-V_c)}{L_l}(t-t_7) \tag{7}$$

When i_p reaches $i_m^- + (i_{LO}^- / n)$, the diode D_4 turns off. The short-circuited state of the transformer disappears, and the voltage across the L_m is V_{in}-V_c. The time of the interval can also be formulated as:

$$t_{87}=\frac{L_l}{(V_{in}-V_c)}\left[\frac{i_{LO}^-}{n}+i_m^- + i_p(t_7)\right] \tag{8}$$

where $i_p(t_7)$ is the value of i_p at time t_7.

III. ZVS Condition of the Switches

From (2) and (6), in order to achieve the ZVS of the switches Q_2 and Q_1, the energy stored in L_l should satisfy the following equations.

$$L_l\left(i_m^+ + i_{LO}^+ / n\right)^2 \ge C_r V_c^2 \tag{9}$$

$$L_l\left(-i_m^- + i_{LO}^- / n\right)^2 \ge C_r (V_{in}-V_c)^2 \tag{10}$$

In practical implementation, the voltage V_c is smaller than V_{in}-V_c, while the duty cycle is limited below 0.5. Otherwise, the primary current $i_p(t_2)$ is larger than $i_p(t_6)$. Therefore, the ZVS condition of Q_1 is stricter than Q_2.

Equations (9) and (10) indicate that the energy stored in L_l should be larger than the energy stored in C_r for ZVS operation. There are two ways to augment the energy stored in L_l. The first is to adjust a small magnetizing inductance of the transformer (without an additional external inductance) for increasing the peak value of the magnetizing current. In order to obtain zero-voltage resonant transition switching, the amplitude of the magnetizing current must be larger than twice the load current contributions to the primary inductor current [5]. Unfortunately, the conduction and switching turn-off losses will increase as the primary current is raised. Another method is to increase the leakage inductance of the transformer for augmenting the energy in leakage inductance [6]. From (4) and (8), the duty loss of the switches is proportional to the leakage inductance. A large leakage inductance will bring about the expense of reduced hold-up time and increased temperature of the transformer.

Therefore, in order to obtain high efficiency and meet the commercial specifications, the trade-off between the leakage and magnetizing inductance for practical applications should be designed. The design considerations of the main parameters of the circuit will be described below.

IV. Design Guidelines and An Example

A. Design Guidelines

The design rules of significant circuit parameters for the studied converter can be derived from the ZVS condition, duty cycle loss and hold-up time etc. They are briefly listed as follows.

a) Choose the maximum duty cycle D_{max}.

With a large D_{max}, the transformer turn ratio can be reduced. By the way, the conduction loss in the primary and ringing on the secondary can be reduced. In practical design, D_{max} should be chosen such that there is enough margins to respond to load disturbances or duty cycle loss. Otherwise, the D_{max} should extreme strict below 0.5 of asymmetrical half bridge forward mode converter.

b) Determine the transformer turn ratio.

Assume the primary and secondary duty cycle is quite close due to the leakage inductance is neglected. Thus, the turn ratio can be determined as:

$$n=2D(1-D)\frac{V_{in}}{V_o} \tag{11}$$

The calculation does not take the duty loss into consideration. The calculated value by equation (11) is always smaller than the desired. The realistic value gotten by adding two or three turns of the calculated value.

c) Set the maximum flux density B_{max}.

The mean value of the transformer magnetizing current $I_{m(DC)}$ is determined from the condition for zero average current through C_b:

$$I_{m(DC)}=\frac{2}{n}D(1-D) \tag{12}$$

The dc magnetizing bias current is proportional to the output load current. Taking the $I_{m(DC)}$ into consideration, the maximum flux density $B_{(+pk)}$ in operation can be formulated as:

$$B_{(+pk)}=\left[\frac{V_o}{4A_eN_s}+\frac{I_o(1-2D)L_m}{A_eN_pn}\right]\cdot 10^8 \tag{13}$$

The maximum value of L_m can be derived as following equation.

$$L_m \le \left[B_{max}\cdot 10^{-8}-\frac{V_oT_s}{4A_eN_s}\right]\cdot\frac{A_eN_pn}{I_o(1-2D)} \tag{14}$$

d) Choose the ZVS range to calculate the minimum value of L_l.

To simplify design, the output inductor current ripple can be set as: $i_{LO,pk-pk} = i_{LO}^{+} - i_{LO}^{-} = 0.5 I_o$. If the ZVS range is chosen, the leakage inductance can be determined.

$$L_l \geq C_r (V_{in} - V_c)^2 / \left[\frac{I_o}{n}(2D - 0.25) + \frac{V_{in} D(1-D)}{2 L_m f_s} \right]^2 \qquad (15)$$

e) Choose the maximum value of L_l to meet the hold-up time.

The relationship between the hold-up time and the input voltage can be formulated as:

$$\frac{1}{2} C_{bulk} \left[V_{in(normal)}^2 - V_{in(\min)}^2 \right] = P_o \cdot t_{hold-up} \qquad (16)$$

where, C_{bulk} is the bulk capacitor.

When setting the hold-up time and choosing the bulk capacitor, we can obtain the minimum operational input voltage, $V_{in(min)}$.

Taking the hold-up time into consideration, the leakage inductor should restrict as:

$$L_l \leq \frac{n^2 V_o T_s}{8 I_o} \left[\sqrt{1 - \frac{4 n V_o}{2 V_{in(normal)}}} - \sqrt{1 - \frac{4 n V_o}{2 V_{in(\min)}}} \right] \qquad (17)$$

f) Select the appropriate value of the L_m and L_l.

B. Experimental Example

The specifications of the experimental converter are listed below:

input voltage: $V_{in(normal)}$=390 V
output voltage: Vo=5 V
output current: I_o=20 A
maximum duty cycle: D_{max}=0.3
switching frequency: f_s=60kHz
hold-up time: $t_{hold-up}$=50ms
bulk capacitor: C_{bulk}=220uF
maximum flux density: B_{max}=3000 Gauss
ZVS range: 10-20 A

Using the above-motioned rules, the experimental converter was constructed using the following components:

1) Q_1,Q_2: 2SK2842 (Toshiba);
2) C_r: 486pF
3) Transformer core: Philips EQ30;
4) Primary: 25 turns (Litz wire)
   Secondary: 1 turns (Litz wire);
5) Output diodes (D_3,D_4) :
   S30SC4M (SBD, IR parts, V_F=0.55 V);
6) Magnetizing inductance 500uH;
7) Leakage inductance should satisfy as:23.9uH<=L_l<=35uH. In the experimental converter, we chose 25uH.

Fig. 4 shows the experimental waveforms on key components. The waveforms were taken under the condition of V_{in}=390 V, V_o=5 V and output power of 50W (5 V/10 A). From the experiment, the drain-to-source voltage of Q_1 (V_{DS}) goes down to zero before the switch is turned on. Also, the key operational waveforms of theoretical analysis in Fig. 3 can be verified by the experimental results. The overall efficiency was measured under different load condition, as shown in Fig. 5. When at full load, the efficiency was 86.1% for the nominal line.

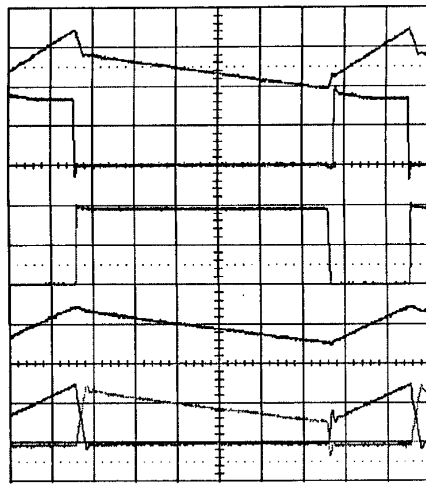

Fig. 4. Experiment waveforms on the key components

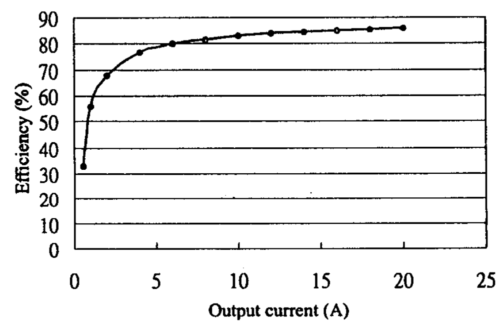

FIG. 5. EFFICIENCY VS OUTPUT CURRENT

V. CONCLUSIONS

In this paper, the variation of the output and magnetizing current is taken into account for getting the operation principle of the asymmetrical half-bridge forward mode converter more exactly. In practical applications, circuit parameters affect the efficiency and soft-switching phenomena of converter. Although a smaller magnetizing inductance or a larger leakage inductance is effective to augment the energy stored in leakage inductor for ZVS operation, other problems are induced by them. In this paper, the design trade-off between the leakage and magnetizing inductance for practical applications is also presented. The design rules are derived from taking the ZVS condition, duty cycle loss and hold-up time into consideration for practical design.

A 5 V/20 A off-line prototype converter is built according to the design guidelines and 86% efficiency is achieved of full load.

REFERENCES

[1] P. Imbertson and N. Mohan, "Asymmetrical Duty Cycle Permits Zero Switching Loss in PWM Circuits with No Conduction Loss Penalty," IEEE Trans. Industry Applications, Vol.29, No.1, Jan./Feb. 1993, pp. 121-125.

[2] W. Shi and J. Xu, "Active Clamp Dual-end Converter," Electronics Letters, Vol. 34, No. 18, Sep. 1998, pp. 1715-1717.

[3] R. Oruganti, P. C. Heng, J. T. K. Guan, and L. A. Choy, "Soft-Switched DC/DC Converter with PWM Control," IEEE Trans. Power Electronics, Vol. 13, No. 1, Jan. 1998, pp. 102-114.

[4] S. Korotkov, V. Meleshin, R. Miftahutdinov and S. Fraidlin, "Soft-Switched Asymmetrical Half-bridge DC/DC Converter: Steady-State Analysis: An Analysis Of Switching Processes," TELESCON, 1997, pp. 177-184.

[5] P. Henze et al., "Zero Voltage Resonant Transition Switching Power Converter," U.S. Patent, No. 5,057,986, Oct. 1991.

[6] J. Wittenbreder, "Zero Voltage Switching Pulse Width Modulated Power Converters," U.S. Patent, No. 5,402,329, Mar. 1995.K. Elissa, "Title of paper," unpublished.