

An OFDM WLAN Baseband Receiver with Space Diversity

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Abstract—In the paper, we present the design and implementation of a baseband receiver with space diversity for IEEE 802.11a OFDM wireless local area network (WLAN). The single-antenna OFDM receiver has been implemented in a single chip. To improve the system performance, we adopt two antennae and apply maximal ratio combining (MRC) for attaining space diversity. We then implement an MRC-based IEEE 802.11a WLAN baseband receiver using two receiver ICs and an FPGA. Actual measurements demonstrate that under several different channel conditions the space diversity receiver outperforms the original single-antenna receiver by up to 8 dB in SNR.

I. INTRODUCTION

Recently, WLAN has received more and more attention in both academia and industry. Basically WLAN systems are designed to provide high-speed indoor links between portable devices and fixed networks. One major effect that deteriorates the performance of wireless communication is multipath fading. Conventional solution to the multipath fading involves time-domain adaptive equalizers, which consume huge amount of hardware. The orthogonal frequency-division multiplexing (OFDM) technique overcomes the fading effect with low-complexity frequency-domain equalizers (FEQ). In addition, OFDM utilizes the bandwidth more efficiently than conventional single-carrier communication systems. Therefore OFDM has been used in the IEEE 802.11a WLAN standard.

To further increase the transmission rate, multiple-antenna techniques can be combined with the OFDM technology. In this paper, we design and implement an OFDM baseband receiver that achieves space diversity by using two baseband receiver chips (one for each antenna) and a signal processing module built in field-programmable gate array (FPGA). The contents of this paper are as follows. Section 2 briefly describes the operation of the baseband receiver IC, including its timing synchronization, carrier frequency synchronization and equalization. In Section 3, we introduce the technique of space diversity, which includes transmit diversity and receive diversity. We discuss only the receiver diversity and show the comparison between two combining methods: selection combining (SC) and maximum ratio combining (MRC). In Section 4, we will give a description of the design of the complete OFDM baseband receiver with space diversity and the measurement results. Finally, a conclusion is given in section 5.

II. BASEBAND OFDM RECEIVER CHIP DESIGN

Fig. 1 depicts the block diagram of the OFDM baseband receiver IC that has been designed and implemented. The receiver IC, as well as the A/D converter, operates at 20MHz. In the beginning, the receiver finds the symbol boundary by the delay correlator and the correlator bank. At the same time, it also estimates the coarse carrier frequency offset (CFO) according to the phase in accumulated delay correlation output values. Once the coarse CFO is estimated it is immediately compensated in the time domain by an oscillator generating a sinusoidal wave with the same frequency as the coarse CFO but in the opposite direction. The remaining CFO, however, is tracked and compensated in the frequency domain. The baseband receiver IC also estimates the channel gain and correct the channel effect in the frequency domain using a frequency-domain equalizer. In the following we will briefly describe these operations.

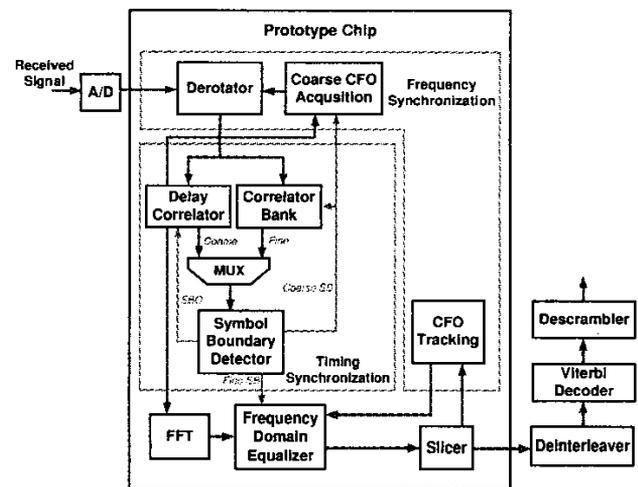


Fig. 1. The block diagram of the OFDM baseband chip.

A. Timing Synchronization

An 802.11a packet starts with ten identical short preamble symbols and then they are followed by two and a half long preamble symbols [1]. As soon as the automatic gain control

(AGC) block has settled, the symbol boundary detector in the baseband receiver starts to determine the correct FFT window. This task is divided into coarse symbol boundary detection and fine symbol boundary detection. Because of the repetitive characteristic of the short preamble segment, the receiver estimates the coarse symbol boundary by means of delay correlation with a delay matching to the length of one or several short preamble symbol. The coarse symbol boundary is detected at the falling edge of the delay correlation (loss of periodicity). In [2], the fine symbol boundary is detected by finding the first path of the channel impulse response (CIR) with an additional FFT operation. In this chip we estimate the CIR in the time domain by a bank of correlators matched to the ensuing long preamble symbol. With the first path of the CIR, the receiver sets the FFT window accordingly to minimize inter-symbol interference (ISI).

B. Frequency Synchronization

As carrier frequency offset (CFO) between the transmitter and the receiver always, the orthogonality between different subcarriers can be destroyed and inter-carrier interference (ICI) introduced. In addition, the phase of the received signal will be rotated by a quantity proportion to the CFO and the time index. Within one OFDM symbol, the phase rotation is 1.44 degree with 1-KHz CFO, and according to [1], the maximum CFO between the transmitter and the receiver can be as large as 232.2 KHz. Hence, CFO is a significant issue that needs be tackled.

In the proposed chip, frequency synchronization is accomplished in two steps: coarse CFO acquisition and CFO tracking. We exploit the fact that CFO is proportional to the phase of the delay correlation to estimate the coarse CFO. The residual frequency offset in the compensated signal can still incur phase rotation in the frequency-domain data. In the ASIC, another PLL is used to track the phase error by compensating in the time domain.

C. FFT and FEQ

We select the radix-2² algorithm in order to reduce the number of the complex multiplications per output sample. The reason is that it has the same multiplicative complexity as the radix-4 algorithm and still retains the regular butterfly structure of radix-2 algorithm. Another operation related to frequency-domain signal processing is FEQ. In the indoor environments, we assume that the channel fades slowly. Therefore, we can apply the channel gain estimated from the long preamble signal to the following OFDM symbols in the same packet without adaptation. The least squares method is adopted in the estimation of channel gains from the long preamble symbols.

D. Channel Decoder and Design Summary

Since we implement only the inner receiver in this chip, the error-correcting code decoder is not implemented. In the following simulation, we collect the output bit streams of the slicer and decode these data using a software decoder. The Viterbi algorithm is chosen as the channel decoder because its

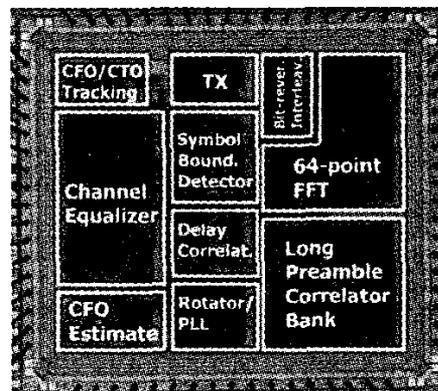


Fig. 2. Die photograph of the OFDM receiver chip ($4102 \times 4600 \mu\text{m}^2$).

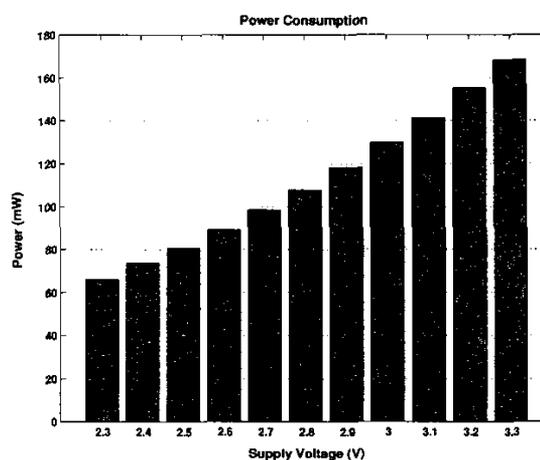


Fig. 3. Power consumption of the OFDM receiver chip.

complexity will not grow exponentially as the number of data bits increases.

The OFDM receiver ASIC is fabricated in a $0.35 \mu\text{m}$ CMOS process and is packaged in a 68-pin CLCC package. It is a cell-based design with several customized memory blocks (mostly delay buffers) to reduce not only the chip power consumption but also the active area. The transistor count is 429659, which is approximately 100K gates and the layout size of the chip including the pad ring is $4102 \mu\text{m} \times 4600 \mu\text{m}$. Fig. 2 shows the photograph of the chip and Fig. 3 shows the power consumption at different supply voltages.

III. SPACE-DIVERSITY RECEIVER DESIGN

Space diversity is used to increased the overall received SNR by utilizing multiple antennae. The antennae are arranged with sufficient spacing such that the channels are assumed independent. Because there are more independent paths between the transmitter and the receiver through proper diversity algorithms, the probability of occurrence of deep fades in all the diversity channels is significantly decreased. So the

performance can be highly improved as the number of diversity increase. Various space diversity techniques have been researched recently [3][4][5][6][7][8][9]. Generally speaking, there are two broad categories of space diversity:

- Transmit diversity: such as delay diversity, space-time trellis codes, space-time block codes, and so on.
- Receive diversity: such as selection combining (SC), maximum ratio combining (MRC), equal gain combining (EGC), and so on.

We focus only on receive diversity because it is much easier to implement with the existing receiver chip. In the following we discuss properties of some most popular combination technique for receive diversity such as SC, EGC, and MRC and make a comparison among these methods:

A. Selection Combining

SC is the simplest technique which just chooses the largest SNR in each symbol interval. However, the SNR is usually difficult to estimate, so most systems use the total power of signal and noise instead of SNR. In other words, we choose the signal with the highest received power. Since the other insignificant signals are completely ignored, we need only one receiver chains. It is an attractive characteristic because we the hardware complexity will not be increased by much. Although SC is quite easy to implement, it is not the optimal combining technique because it discards the information from all but one antenna.

B. Maximum Ratio Combining

In MRC, the received signal from different antennae are rotated so that they are co-phased, weighted proportionally by the magnitude of the channel gain, and finally summed. Conceptually speaking, if the magnitude of the channel gain is larger, the corresponding signal suffers less channel-fading effect and becomes more reliable. In one word, MRC can perform much better than SC because it collect the information from all the antennae and weight the signal by the optimal coefficients. However, the performance somewhat degrades if there exists channel estimation errors and frequency offset [6].

C. Equal Gain Combining

In EGC, the received signal from different antennae are rotated to be co-phased, and then combined. In other words, all the signal branches are weighted equally. EGC is usually used in case the magnitude of channel gain is not convenient to estimate. In general, EGC performs slightly worse than MRC because it lacks the information about the magnitude of channel gain, which contains the reliability in the subcarrier.

We compare the performance of different combining schemes through computer simulation. For simplicity, we only consider the case of 2-antenna diversity receiver. We use the same architecture of synchronization blocks and the FFT block. QPSK modulation with 1/2 rate convolutional code is

used and the number of OFDM symbols is set to 50 per packet. We also take the average of the packet error rate over several static channels with the same RMS delay spread. Fig. 4 shows the simulation results of packet error rates using different diversity techniques under multipath fading channel. It is clear that the MRC receiver with 2-antenna diversity outperforms 1-antenna receiver by about 8 to 9 dB. The performance of EGC receiver is slightly worse than MRC receiver. In addition, the SC receiver with 2-antenna diversity only outperforms the single-antenna receiver by less than 2 dB. No matter what kind of diversity technique is used, the curve with two antennae is steeper than the one with one antenna. It is because the probability of signals at the same subcarrier from two antennae are both deep faded is much less. Since the magnitude of the channel gain can be estimated by the receiver chip, it is not difficult to realize the MRC technique. As a result, we determine to adopt MRC technique for the implementation of the baseband space diversity receiver.

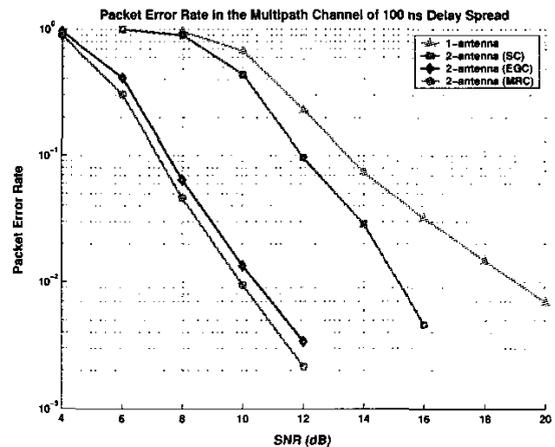


Fig. 4. The packet error rates with 2-antenna diversity of different combining schemes.

IV. HARDWARE IMPLEMENTATION AND MEASUREMENT RESULTS

For the sake of simplicity, we implement the space diversity receiver with only two antennae. Fig. 5 illustrates the architecture of the space diversity receiver. We reuse the block of the coarse symbol boundary detector, the fine symbol boundary detector, the coarse frequency estimation loop, and FFT in the chip, and implement the other circuits, including the CFO tracking loops, the frequency domain equalizer and combination circuit, and the slicer, using an FPGA.

Fig. 6 shows the photograph of the space diversity receiver hardware. We have also implemented the diversity receiver in FPGA simulator environment to verify the functionality of the design. From the simulation results, we can see that although the signal from one of the antennae is in deep fade, the diversity receiver can still get the correct data by combining it with signal from the other antenna. Fig. 7 shows the packet error rate of the space diversity receiver in different Rayleigh fading channels. The practical measurement result

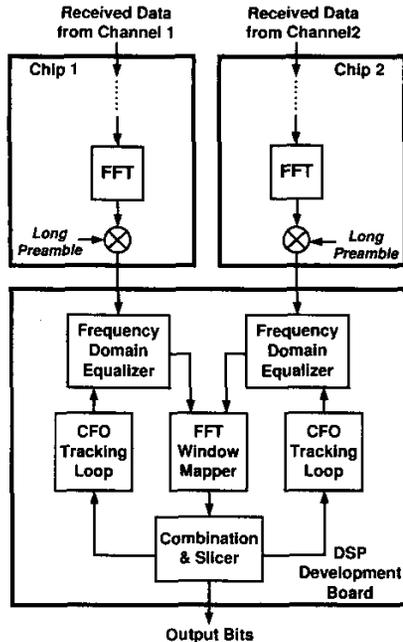


Fig. 5. Block diagram of the OFDM baseband receiver with space diversity.

degrades about 1 dB compared from the simulation. Although the hardware requirement of the space diversity receiver is approximately twice as large as that of single-antenna receiver, it outperforms the single-antenna receiver by about 8 dB in SNR.

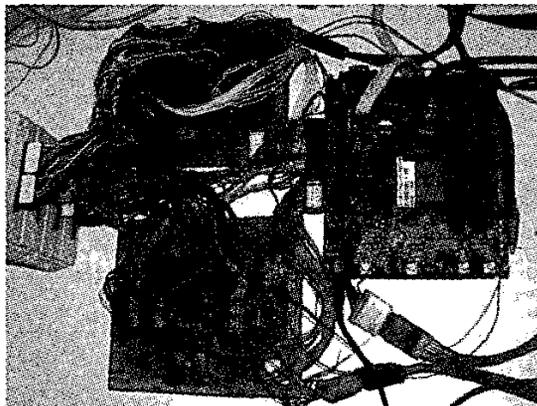


Fig. 6. Photograph of the OFDM baseband receiver with space diversity.

V. CONCLUSION

In the paper, we present the design and implementation of a baseband receiver with space diversity for IEEE 802.11a OFDM WLAN. This system includes two single-antenna OFDM receiver chips and an FPGA board that executes MRC as an approach to attain space diversity. Actual measurements demonstrate that under several different channel conditions

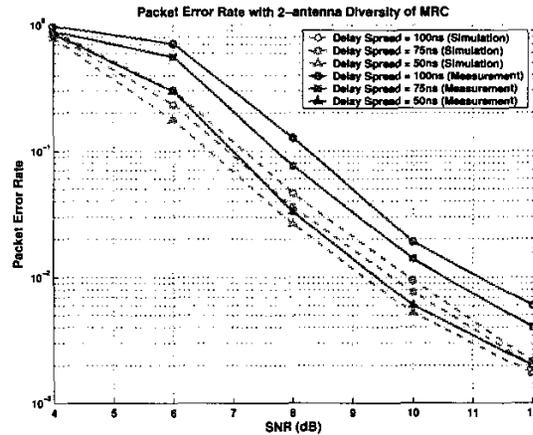


Fig. 7. Packet error rates of the 2-antenna diversity receiver using MRC under channels with different delay spread.

the space-diversity receiver outperforms the original single-antenna receiver by up to 8 dB in SNR.

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