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A Low Power 5Gb/s Transimpedance Amplifier with Dual Feedback Technique

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Abstract-This paper presents the design and implementation of a 5Gb/s transimpedance amplifier (TIA) with dual shunt-shunt feedback technique to enhance the circuit performance. Measured bandwidth is 4.9GHz and measured transimpedance gain is 60 dB Ω. The chip consumes only 8mW at 1.8V supply voltage and occupies 650μm×500μm in a 0.18μm CMOS process.

I. Introduction

The recent growth in the optical fiber communication industry has resulted in high demand for low-cost high-performance optical front ends. One of the critical components of the optical fiber receiver front end is the transimpedance amplifier. A TIA requires high transimpedance gain, high bandwidth, low input impedance, and low power consumption. However, the power consumption trade off with gain and bandwidth product. In this paper, the proposed dual shunt-shunt feedback network used to improve this trade off.

II. TIA architecture

The complete architecture of the proposed TIA is depicted in Fig. 1. It consists of a bias network, core amplifier, and the output buffer.

A. Core amplifier

The core amplifier, depicted in Fig. 1, has to provide a sufficient voltage gain so as to increase the TIA's bandwidth and make its Z_{21} very close to R_F. In this amplifier, the cascode common source amplifier can eliminate the Miller capacitance effect. However, large capacitance due to photodiode's parasitic effect makes the design more difficult. In order to minimize the power dissipation, the inductive peaking technique [1] is utilized in this circuit, since it does not occupy additional voltage headroom and can improve the speed effectively.

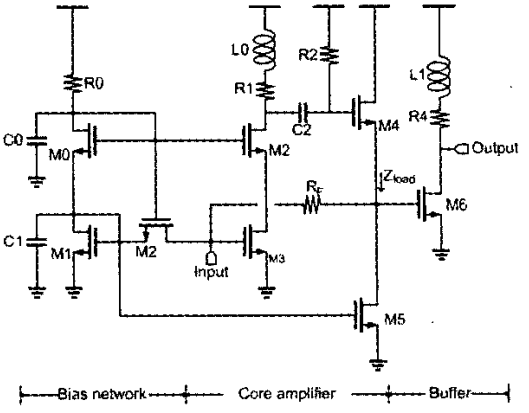


Fig. 1 The proposed TIA

One of the dual shunt-shunt feedback networks in the proposed core amplifier is composed of the MOS transistors $M_2 \sim M_4$, AC couple capacitor C_2, and feedback resistor R_F. Assume the amplifier exhibits a mid band gain A_0 and one pole at ω_0, then its transfer function is given by Equation (1).

$$A(s) = \frac{A_0}{1 + s/\omega_0} \tag{1}$$

The transfer function of a TIA can be given as

$$\frac{V_{out}}{I_{in}}(s) = -\frac{A_0 R_F}{\frac{R_F C_{PD}}{\omega_0} s^2 + (R_F C_{PD} + \frac{1}{\omega_0}) s + A_0 + 1} \tag{2}$$

where it is assumed that $A_0 >> 1$, and C_{PD} is the photo diode capacitance. Usually, it is a typical second order system. The denominator of a second-order transfer function is expressed as $s^2 + 2\xi\omega_n s + \omega_n^2$, then ξ, the "damping factor," must be equal to $\sqrt{2}/2$ for critical damping. Rewriting (2), we have

$$\frac{V_{out}}{I_{in}}(s) = -\frac{A_0 R_F}{s^2 + \frac{R_F C_{PD} + 1/\omega_0}{R_F C_{PD}/\omega_0} s + \frac{(A_0 + 1)\omega_0}{R_F C_{PD}}} \tag{3}$$

When $\xi = \sqrt{2}/2$, then

$$\omega_0 \approx \frac{2A_0}{R_F C_{PD}} \tag{4}$$

Thus, the -3dB bandwidth of the core amplifier must

be chosen equal to twice the closed-loop bandwidth of the first-order TIA to ensure a critical-damped response. With the above condition for critical damping, the -3dB bandwidth of the TIA is

$$\omega_n = \sqrt{\frac{(A_0+1)\omega_0}{R_F C_{PD}}} \approx \frac{\sqrt{2}A_0}{R_F C_{PD}} \qquad (5)$$

From equation (2) and (5), we have to choice R_F carefully to trade off between transimpedance gain and bandwidth. In our TIA, we take the R_F equals 1kΩ for 60dB transimpedance gain in bandwidth better than 5GHz without photo diode capacitance loading.

Between the first stage and the source follower, a capacitor (0.8p) for ac coupling is connected. This is because we need large bias current in the first stage to provide sufficient voltage gain but will results in a lower dc level. If we apply dc couple between the two stages, the output dc level of the source follower will be too low to turn on the buffer transistor. The bias resistor of the source follower is realized by a PMOS operating in the triode region.

For the cascaded circuits, they usually have a pole at each stage output due to loading circuit. In our TIA circuit, there is a pole in the output of the core amplifier. If the loading impedance Z_{load} is large, this pole will become dominated and decrease circuit bandwidth. In order to eliminate this effect on core amplifier's bandwidth, a second shunt-shunt feedback network is incorporated in the output of the core amplifier. This feedback network is composed of the MOS transistors M_1 ~M_2 and M_5, resistor R_F, and capacitor C_1. The transistor M_2 is operated in triode region. Assume the capacitor C_1 is larger than the parasitic capacitance of the MOS transistors, C_{gs} and C_{gd}. The on resistance of M_2 is R_{on2}, and r_{o5} is the output resistance of M_5. The loading impedance of the core amplifier can be written as

$$Z_{load} \approx \frac{1+sC_1(R_F+R_{on2})}{s^2C_1C_{gs6}(R_F+R_{on2})+s\left(C_1+C_{gs6}+\frac{C_1(R_F+R_{on2})}{r_{o5}}\right)+g_{m5}+\frac{1}{r_{o5}}} \qquad (6)$$

It induces a zero and if one properly chooses the value of C_1 and R_{on2}, the bandwidth can be extended by canceling a pair of zero and pole. On the other hand, capacitor C_1 short the AC signal to ground, the input signal will not go through transistor M_5 to the output. By this topology the bandwidth of the core amplifier can be enhanced without increasing power consumption.

B. Noise Optimization

To optimize the input-referred noise of a TIA, one must very carefully choose the size of the input device since it contributes most of the noise [2]. Consider the simplified noise model shown in Fig. 2.

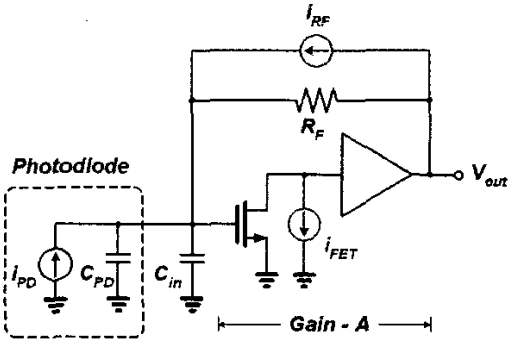


Fig. 2 Equivalent model for optimizing the input noise.

There are two main noise sources: the thermal noise current of the feedback resistor and the channel thermal noise current of input transistor. The expression for the input-referred current density is given by

$$\overline{i^2_{n,in}} = \frac{4kT}{R_F} + \frac{\overline{V^2_{nA,out}}}{R_T(s)^2} \qquad (7)$$

Where $V_{nA,out}$ represents the output noise voltage due to the core amplifier and we have

$$V_{nA.out} = \frac{-A(sR_FC_D+1)}{sR_FC_D+A+1} 4kT\gamma \frac{1}{\sqrt{g_m}} \qquad (8)$$

Substituting equation (8) into (7), we can derive the complete form of input-referred noise

$$\overline{i^2_{n,in}} = 4kT\left[\frac{1}{R_F} + \frac{\gamma}{R_F{}^2 g_m} + \gamma\omega^2\left(\frac{C_{PD}}{\sqrt{g_m}} + \frac{\sqrt{g_m}}{\omega_T}\right)^2\right] \qquad (9)$$

In (9), the second term can be neglected compared

with the first term, where ω_T , the unit gain frequency of a transistor, equals to gm/ (C_{gs} + C_{gd}). To optimize the spectral density of input-referred noise current, we should make $g_m = C_{PD} \cdot \omega_T$ or to choose the input transistor size such that C_{gs} + C_{gd} = C_{PD}. Although the above example tells us that when C_{gs} + C_{gd} = C_{PD}, the noise will be reduced to the minimum level. The transistor size will be quite large and makes it difficult to reach a high bandwidth. We have to choice the core amplifier architecture and circuit layout carefully for this trade off.

C. Output buffer

In order to drive the 50Ω impedance of the oscilloscope, the output buffer should have a high current driving ability. In some recent researches, the common-source type amplifier has become a better choice. First, the output dc level is determined independent of the input dc level thus will not suffer from smaller voltage headroom. Second, the output matching can be achieved by simply place a 50Ω resistor or two 100Ω resistor in parallel.

III. Experiment results

This work has been fabricated in 0.18 μm 1P6M CMOS process and the die photo is given in Fig. 3. To measure the frequency domain performance, the TIA chip is probe-tested with network analyzer. The measured transimpedance gain, Z_{21} is given in Fig. 4. The measured -3dB bandwidth is 4.9GHz and the midband transimpedance gain is 60dBΩ. The measured eye diagrams are given in Fig.5. The eye diagrams at 2.5Gbps, 3.125Gbps and 5Gbps when the input equivalent current equals 30uA respectively. Not only the first eye diagram fits in with the OC-48 mask very well but also widely open at the data rate of 5Gb/s.

IV. Conclusion

In this work, a 1.8V, 5Gbps low power transimpedance amplifier using dual shunt-shunt feedback technique is implemented on a standard 0.18um CMOS process. By this way, the circuit bandwidth can be enhanced and only has 8mW power consumption. The characteristics of this circuit are listed in table I.

Table I Performance summary

Process	0.18um CMOS
Supply Voltage	1.8V
Speed (bit/s)	5G
Trans. Gain (Ω)	1k
Sensitivity	20uA
Power Dissipation (mW)	8
Input-referred noise current	9pA/$\sqrt{Hz}$
Chip Area (μ m^2)	650 × 500

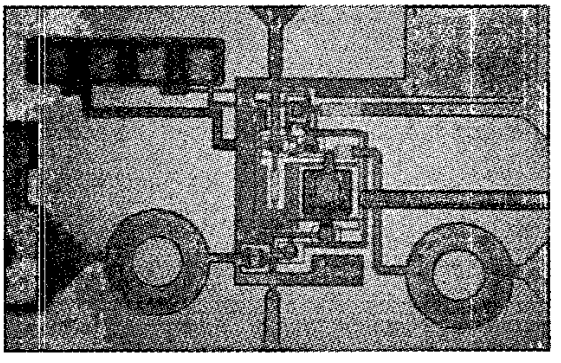


Fig.3 Die photograph of the TIA

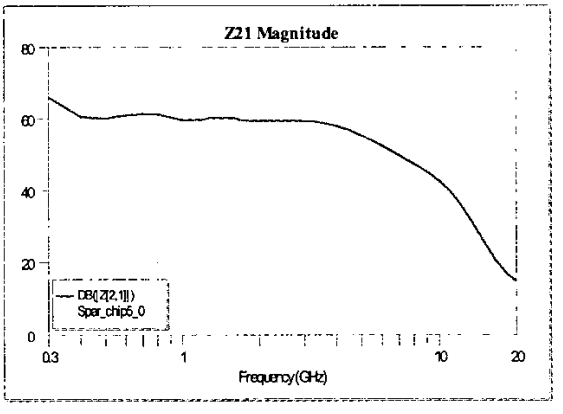
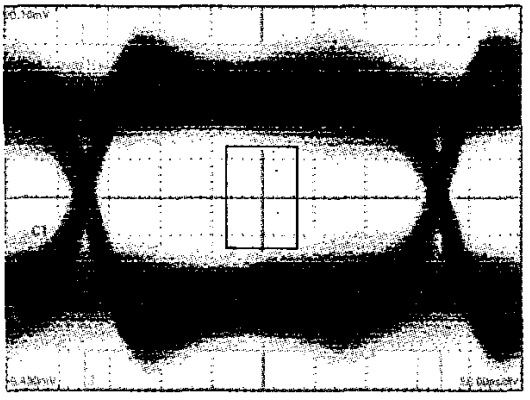
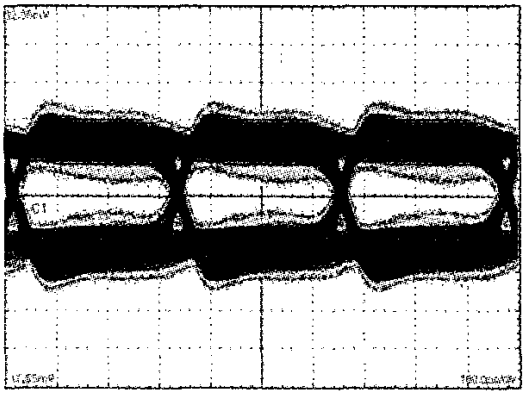


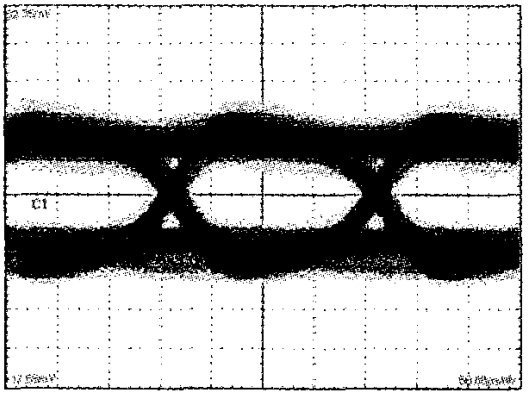
Fig.4 The measured transimpedance gain



(a) Eye diagram at 2.5Gb/s



(b) Eye diagram at 3.125Gb/s



(c) Eye diagram at 5Gb/s

Fig. 5 Measured eye diagrams

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