行政院國家科學委員會補助專題研究計畫成果報告

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※ 具有智慧型天線的寬頻 CDMA 基地站收發機之研製 ※

※ 子計畫三 —寬頻 CDMA 收發機中即時基頻信號模組之研製 ※

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計畫類別：□個別型計畫 ■整合型計畫

計畫編號：NSC－89－2219－E－002－036

執行期間： 89 年 8 月 1 日至 90 年 7 月 31 日

計畫主持人：闕志達

執行單位：國立臺灣大學電機學院電機系

中 華 民 國 90 年 10 月 23 日

行政院國家科學委員會專題研究計畫成果報告

寬頻 CDMA 收發機中即時基頻信號模組之研製

Design and Implementation of Real-time Baseband Signal Processor in Wideband CDMA Transceiver

計畫編號：NSC-89-2219-E-002-036

執行期限：89 年 8 月 1 日至 90 年 7 月 31 日

主持人：闕志達　　國立臺灣大學電機學院電機系

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一、中文摘要

本計畫主要提出一個基於 3GPP 所提出並由 ITU IMT-2000 標準所接受的建議書中的寬頻 CDMA (Wideband CDMA, W-CDMA)系統標準的上傳基頻收發機架構設計及晶片設計並驗證，此架構中並含有 RAKE 接收機及波束合成器以增加系統接收能力。寬頻 CDMA 之所以成為下一代行動通訊的關鍵技術，主要是提供了目前所不能兼顧的行動力和互動性，大幅增加使用者的移動性和傳送資料的頻寬。在此架構中，波束合成器利用波束搜尋器所得出的空間特徵，將由四組天線進入的輸入信號合併，由此可獲得 6 dB 在空間變化上的增益。另外在路徑變化上的增益可藉由 RAKE 接收機收集由多路徑而來的信號，再加上由通道估計器所得到的參數，進行最佳比例合成後得到。為了要測試所提出架構的可行性，無向量及向量通道均在所測試的模擬中使用。系統模擬結果顯示，本論文中提出的架構除了可以達到標準中的基本要求外，在不大幅增加系統的複雜度下，波束合成器更可大幅提昇接收的效能，例如在抗拒多使用者雜訊上。

關鍵詞：收發機、W-CDMA、RAKE、 beamforming、smart antenna

Abstract

This paper presents the architecture design, IC design and implementation of an uplink baseband transceiver for W-CDMA systems. The architecture is designed based on 3GPP Radio Access Network FDD mode specification. In addition, advance techniques such as beamforming and RAKE receiving are adopted. The beamformer uses spatial signature calculated by the beam searcher to combine input signals from four antennas and therefore a spatial diversity gain is introduced. Path diversity is provided by the RAKE receiver, which gathers four multi-path signals with the weights obtained from the channel estimator for maximum ratio combining. Scalar channel and vector channel models are both used in the simulation to verify the design. Both simulation and hardware emulation results show that the proposed architecture can indeed meet the specified requirement, and the advanced techniques, such as beamformer, really provide an enhancement in reception.

Keywords: Transceivers, W-CDMA, RAKE, beamforming, smart antenna

二、緣由與目的

隨著全球各國電信自由化的進展潮流及無線通訊技術的日益進步，無線通訊產業之競爭趨於白熱化，而產品類別更為多樣化，且市場需求大增。在電信國家型計劃中無線通訊分項之計劃以第三代無線通訊技術 IMT-2000 為主。因為國際電信聯盟(ITU)在 1999 年

決定 IMT-2000 (International Mobile Telecommunication 2000) 空中介面標準。預計在下世紀初期會有許多 IMT-2000 產品上市。在 IMT-2000 中利用寬頻 CDMA 技術的標準分別由歐、美、日三地提出三套相似的建議，其中皆採用利用可適性天線鎮列(adaptive antenna array) 與波束合成(beamforming)之技術，皆以 RAKE 接收器解決展頻訊號所遭遇的多路徑問題。本計劃採用歐洲 3GPP 所提出之 UTRA 建議，使用 QPSK 調變方式，利用樹狀結構的展頻碼來達成多傳輸速率的要求。

本計畫之目的在於以歐洲 ETSI 所提出之 W-CDMA 系統為範本發展一以 W-CDMA 技術相容之基地台收發機中基頻信號處裡模組。此模組中包含發射機中之波束合成技術、展頻技術、接收機中之可適性波束合成技術、符誌時序同步技術、載波同步技術、展頻 RAKE 接收技術等等。前幾年度主要著重於研讀系統及設計系統架構為主要目標，而本年度則主要以系統效能及 IC 設計及製作及系統整合為主要重點。

三、結果與討論

(一)簡介

有關於 3GPP 所提出的 W-CDMA 建議可參考前年到告中之表一。另外關於本系統的大略功能已於前年報告中介紹，故今年僅提出最新的研究成果。接收機的部份為因應發送機的設計可由如圖一中的設計。其中由於在通訊中一直有 pilot 信號的傳送，因此可以有一個頻道估計器(Channel Estimator)如圖二來計算頻道的參數變化，可提供時脈回復以及之後的載波回復、波束合成、RAKE 接收機運作時的重要參考，以能成功的將信號還原回來，是本接收機中最重要的部份。在 PRACH 中要先偵測有 Random Access Request 發出，因此有另一個 RAQ 偵測器，一旦偵測到，則可根據預先所給定的參數來進行通訊，進入到 DPCH 的工作模式。在 PRACH 中的 message part 及在 DPCH 中的資料傳送結構用的都很相似，因此可以採用同樣的架夠來進行接收的動作。頻道估計器仍然是做頻道參數值的估計，所得的參數則給 RAKE 接收器及波束合成器來使用。另外由於相位偏差對展頻通訊的品質影響很大，因此在做處理前，應先將接收進來的信號相角轉正，如此之後的信號處理才不會有問題，因此載波回復(Carrier Recovery)電路(如圖三)即是為了此功能而設計的。RAKE 接收器由四路 Finger 所組成，可收集由不同四路而來多路徑的信號在經過時間對齊、相位轉正及加權相加後，可得到較高品質的信號以供偵測決定用。其架構如圖四所示。而在波束合成器部份則是用來將空間上的分量相加，以其能達到更強的訊雜比以增加通訊品質，如圖五。圖六為波束合成器的結果，可以將波束合成到對準欲接收的使用者方向，而可增加接收的訊噪比。圖七則為對於多使用者雜訊消除的情況，若在有波束合成器的情況下，在系統中同時傳送 64 kbps 的資料的情況下，系統中仍可容納三四十人同時使用。

(二)Fixed-Point 模擬結果

因為要將所設計的架構做成硬體，因此必需將原來用浮點數模擬的架構做 finxed-point 模擬，以得到在做成硬體時各區塊需要用到複雜度。表一為模擬之後決定的在特殊重要信號點所採用位元數。圖八為 Verilog 模擬之結果，其功能皆正常，如設計時所要求。

(三)IC 設計及製作

在此我們是利用 TSMC 0.35μm 的製程，利用部分 cell ensemble 部分 full custom 的方式來完成整顆晶片，其設計之規格如表一所示。晶片的 layout 如圖十一所示，主要分為左右兩大區塊,右邊為頻道估計器中最重要的 Matched Filter，為求晶片可以省電以及縮小其面積， 而以 full custom 的方式，採用 Latch File 的設計而不用一般 Flip Flop 當作移位暫存器的做法，使得晶片面積可以縮小，並且可以再沒有動作時減少其切換的動作以達到省電的功能，可以大幅降低其操作時需要的功率，以完成低功率的設計，其電路圖如圖九、圖十所示。圖十二為完成晶片佈局後的模擬，以 Timemill 軟體模擬得最高的工作頻率可到 50 MHz。

四、計畫成果自評

在本論文中，我們設計了一個 W-CDMA 上傳基地台的基頻信號處理器的架構。此架構中用頻道估計器來估計頻道的變化，以供 RAKE 接收器、載波回復電路和波束合成器的運作，使得之後的偵測信號的訊雜比可以大幅提高，增加通訊品質。目前已完成了系統架構的模擬、fixed-point 架構的模擬、Verilog 的模擬以及硬體的 Emulation (Aptix 系統)，以及晶片的設計及製作。由目前的驗證結果可以得知，的確可以利用所設計的關鍵性模組，在使用最少的硬體資源下，得到理想的系統效能，至於整個系統整合的部份，等到晶片由晶片設計中心送回後，即可和其它子計劃的模組相結合，其整合的部分可由圖十三所示，晶片的部分即為圖中 baseband 的部分，配合其他 RF/IF 的部分即為一完整的系統。

五、參考文獻

[1] F. Adachi, M. Sawahashi, and H. Suda,``Wideband DS-CDMA for Next-Generation Mobile Communications Systems," IEEE Communication Magazine, vol.36(9), pp.56--69, Sept. 1998.

[2] T. S. Rappaport, Smart Antennas for Wireless Communications: IS-95 and Third Generation CDMA Applications,Prentice Hall, NJ, 1999.

[3] K. Okawa, Y. Okumura, M. Sawahashi, and F. Adachi,"1.92 Mbps Data Transmission Experiments Over a Coherent W-CDMA Mobile Radio Link," VTC 98, vol.48(2), pp.1300--1304, 1998.

[4] M. Sundelin, W. Granzow, and H. Olofsson,``A Test System for Evaluation of the WCDMA Technology," VTC 98, vol.48(2), pp.983--987, 1998.

[5] L. Philips, N. Lugil, and J. Vanhoof,``A Baseband IC for 3G UMTS Communications," VTC 99}, vol.50(3), pp.1521--1524, 1999.

[6] A. Morrison, and B. S. Sharif,``A Space-Time Beamforming RAKE Receiver for Third Generation Wideband CDMA Base Stations," IEEE International Conference on Consumer Electronics}, pp.312--313, 1999.

[7] X. Mestre, J. F. Fonollosa, and G. Vazuqez, ``Uplink Beamforming for the FDD Mode of UTRA," VTC 99, vol.49(1), pp.867--871, 1999.

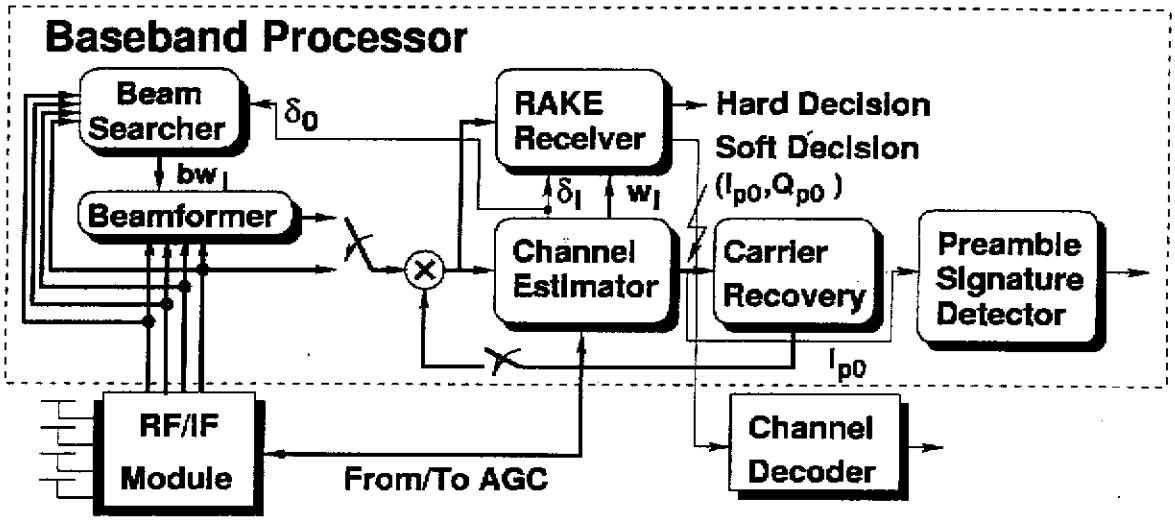
[8] K. H. Chang, I. S. Sohn, and K. S. Chang,``Chip-Level 2-D RAKE Receiver with Symbol-Level Searcher Beamforming," VTC 99, vol.50(2), pp.924--928, 1999.

[9] E. S. Shiu, and Y. O. Park, ``Design and Analysis of a Smart Antenna System for IMT-2000 W-CDMA," VTC 99, vol.49(3), pp.2109--2112, 1999.

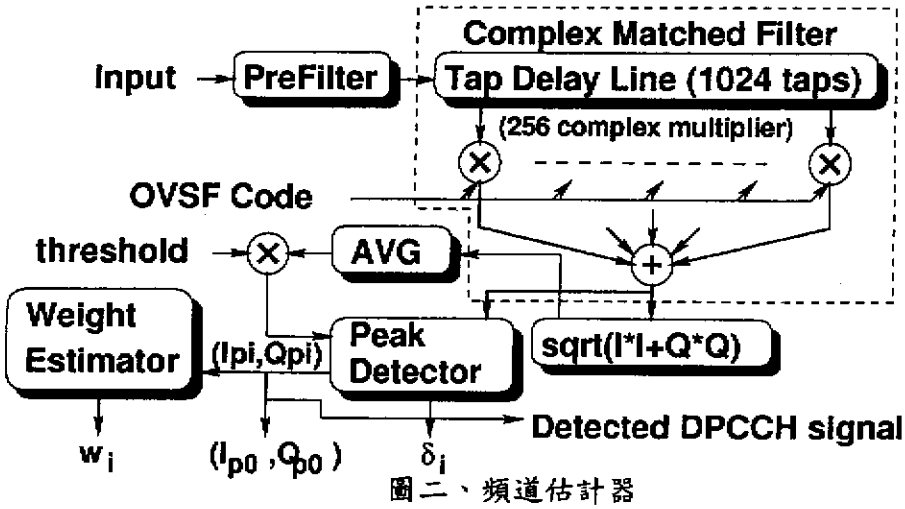
[10] 3GPP TSG RAN WG1, Physical Channels and Mapping of Transport Channels onto Physical Channels (FDD), TS 25.211 v3.4.0, October, 1999

[11] 3GPP TSG RAN WG1,Multiplexing and Channel Coding (FDD), TS 25.212 v3.4.0, October, 1999

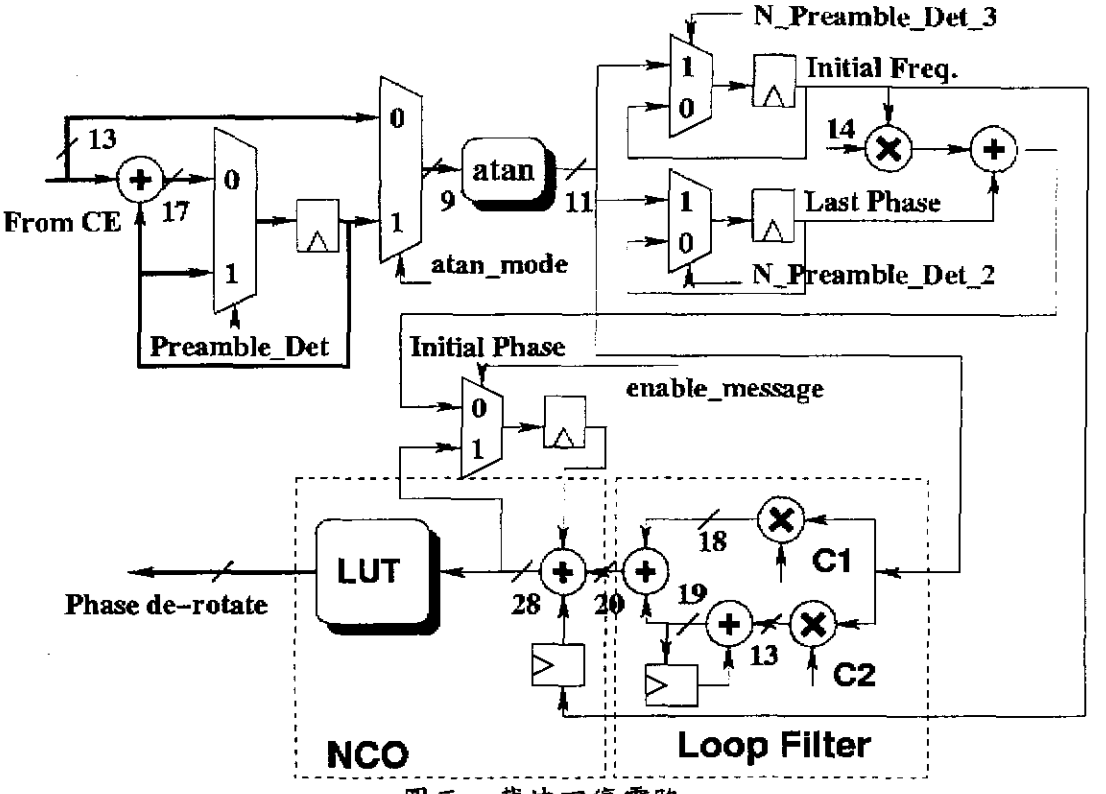
[12] 3GPP TSG RAN WG1,Spreading and Modulation (FDD),TS 25.213 v3.3.0, October, 1999
[13] 3GPP TSG RAN WG1,Physical Layer Procedures (FDD), TS 25.214 v3.4.0, October, 1999
[14] 3GPP TSG RAN WG4, UTRA (BS) FDD; Radio Transmission and Reception, TS 25.104 v3.4.0, October, 1999
[15] S. R. Saunders, Antennas and Propagation for Wireless Communication Systems,John Wiley & Sons, Inc., 1999.
[16] K. Pahlavan and A. H. Levesque,Wireless Information Networks}, John Wiley & Sons, Inc., 1995.
[17] W. C. Y. Lee, Mobile Communications Design Fundamentals, 2nd ed., John Wiley & Sons, Inc., 1993.
[18] J.K. Holmes,Coherent Spread Spectrum System, New York: Wiley, 1982.
[19] T. S. Rappaport,Wireless Communications: Principles and Practice, Prentice Hall, NJ, 1996.
[20] W. F. Egan,Phase-Lock Basics,John Wiely & Sons, Inc., 1998.
[21] S.-S. Jeng, G. Okamoto, and G. Xu,``Experimental Evaluation of Smart Antenna System Performance for Capacity Improvement," GLOBECOMM '97, vol.1, pp.369--373, 1997.
[22]S.-S. Jeng, Okamoto G.T., G. Xu, H.-P. Lin, and Vogel W.J.,``Experimental Evaluation of Smart Antenna System Performance for Wireless Communications," IEEE Transactions on Antennas and Propagation, vol.46(6), pp.749--757, June 1998.



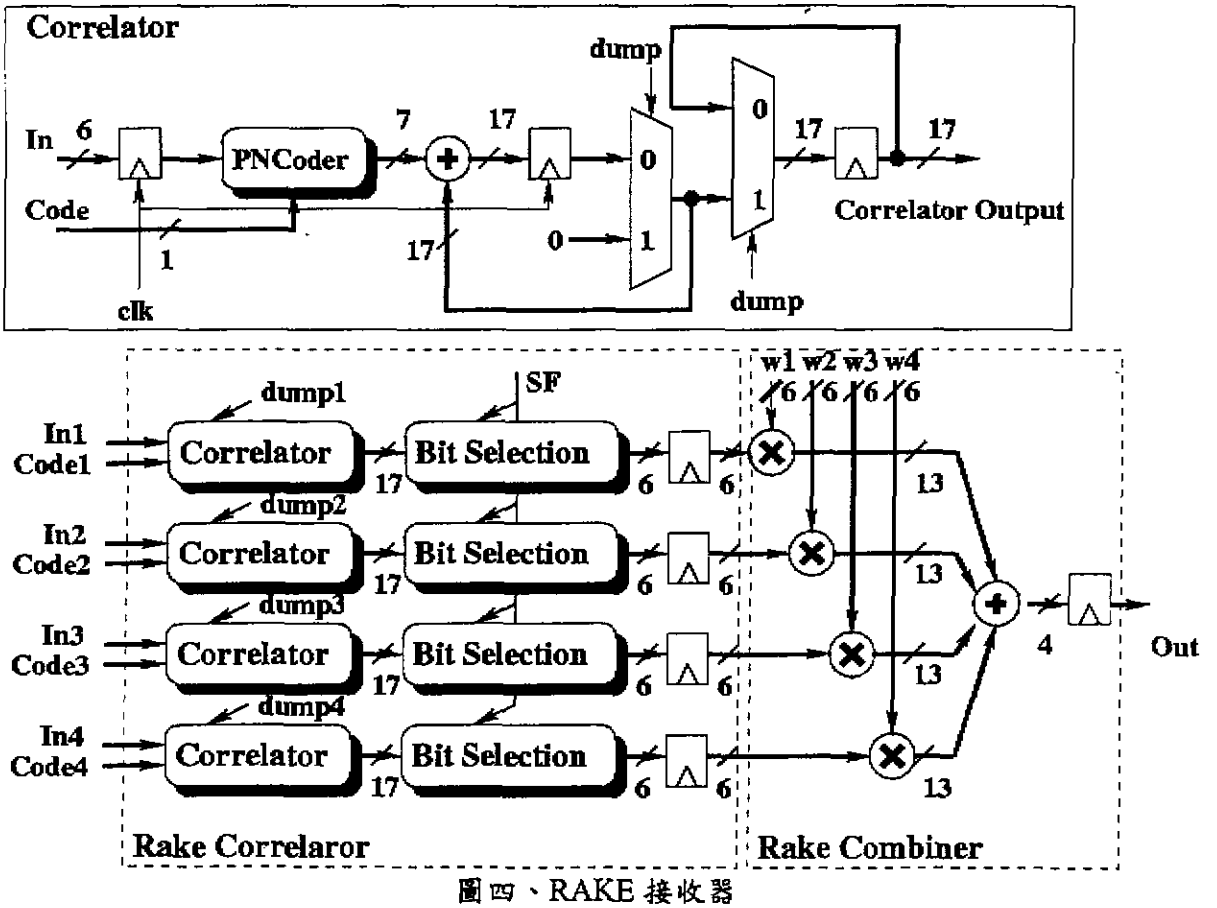
圖一、接收機總圖



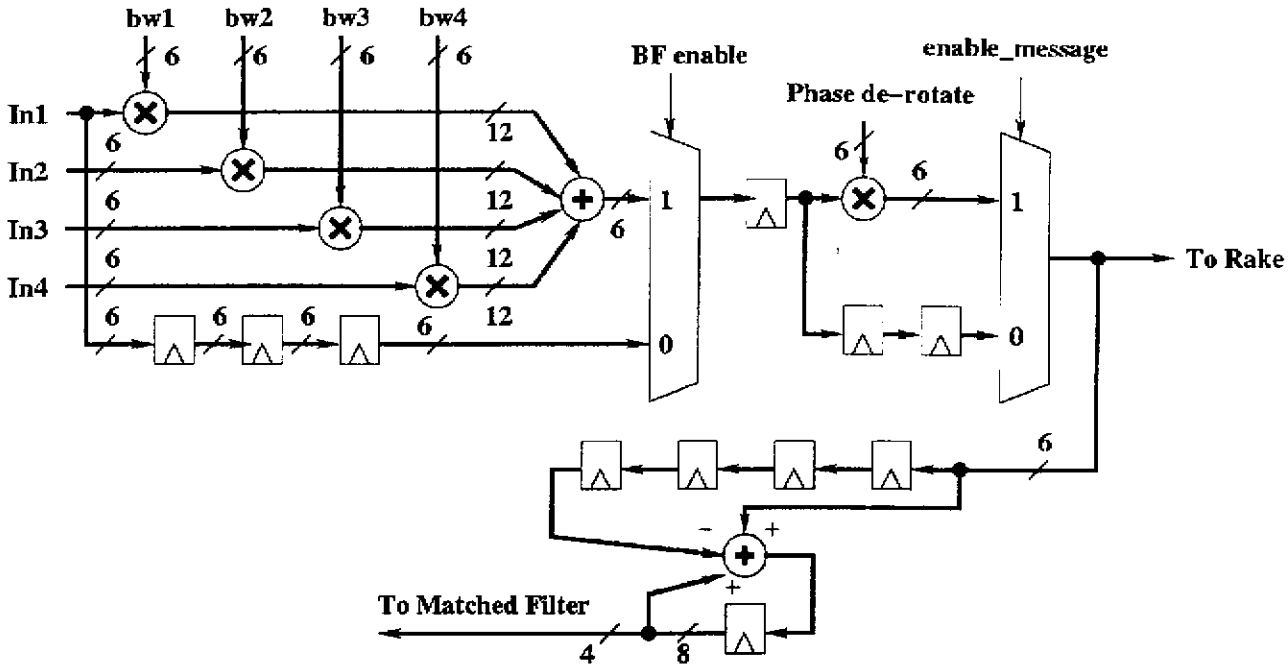
圖二、頻道估計器



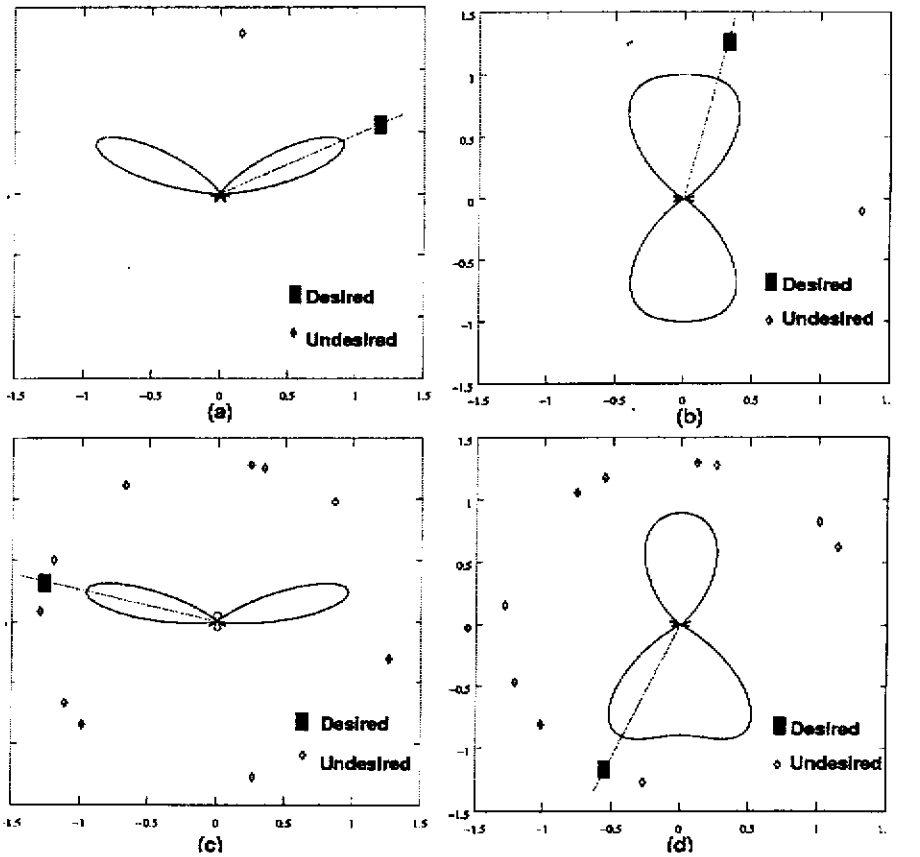
圖三、載波回復電路



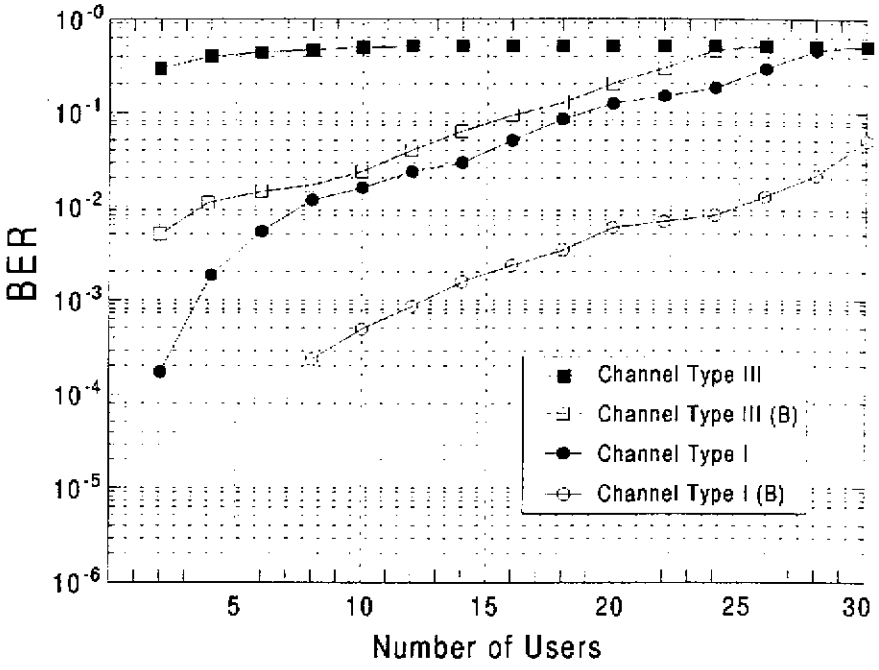
圖四、RAKE 接收器



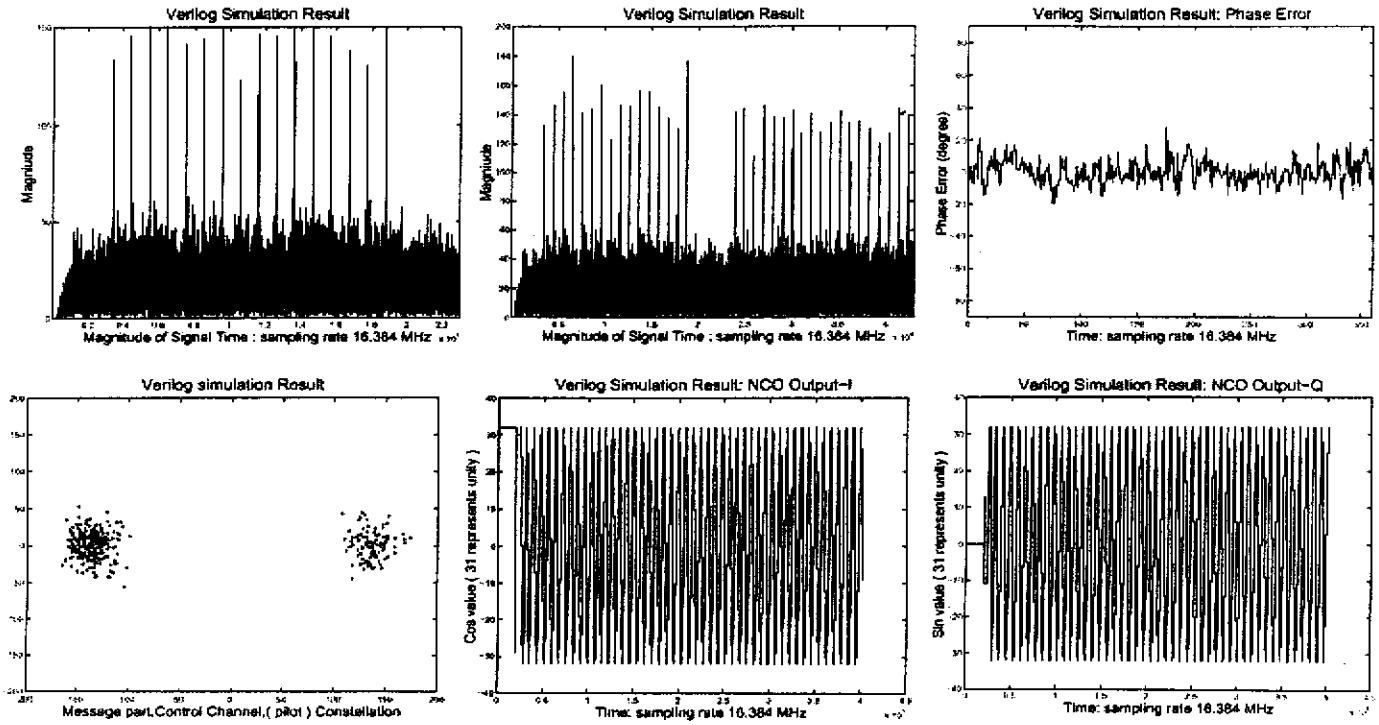
圖五、波束合成器



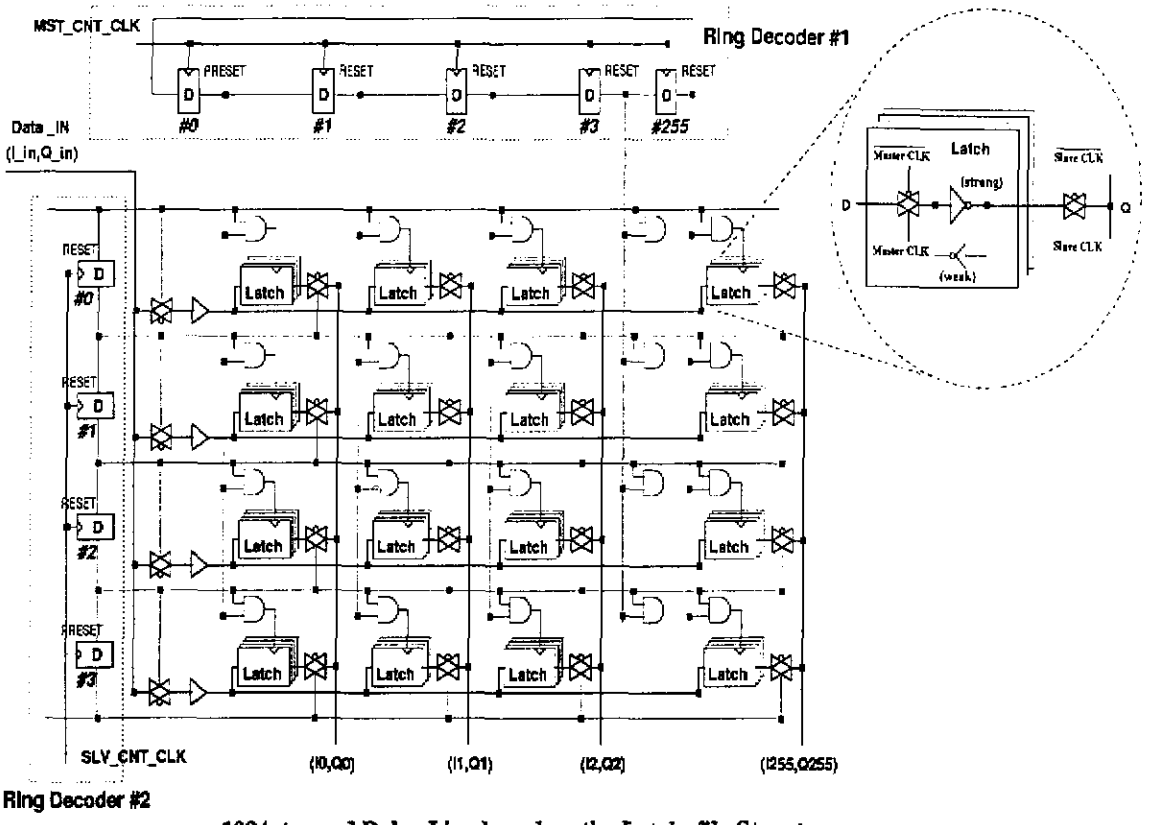
圖六、波束合成器將方向對到使用者



圖七、波束合成器消除多使用者雜訊

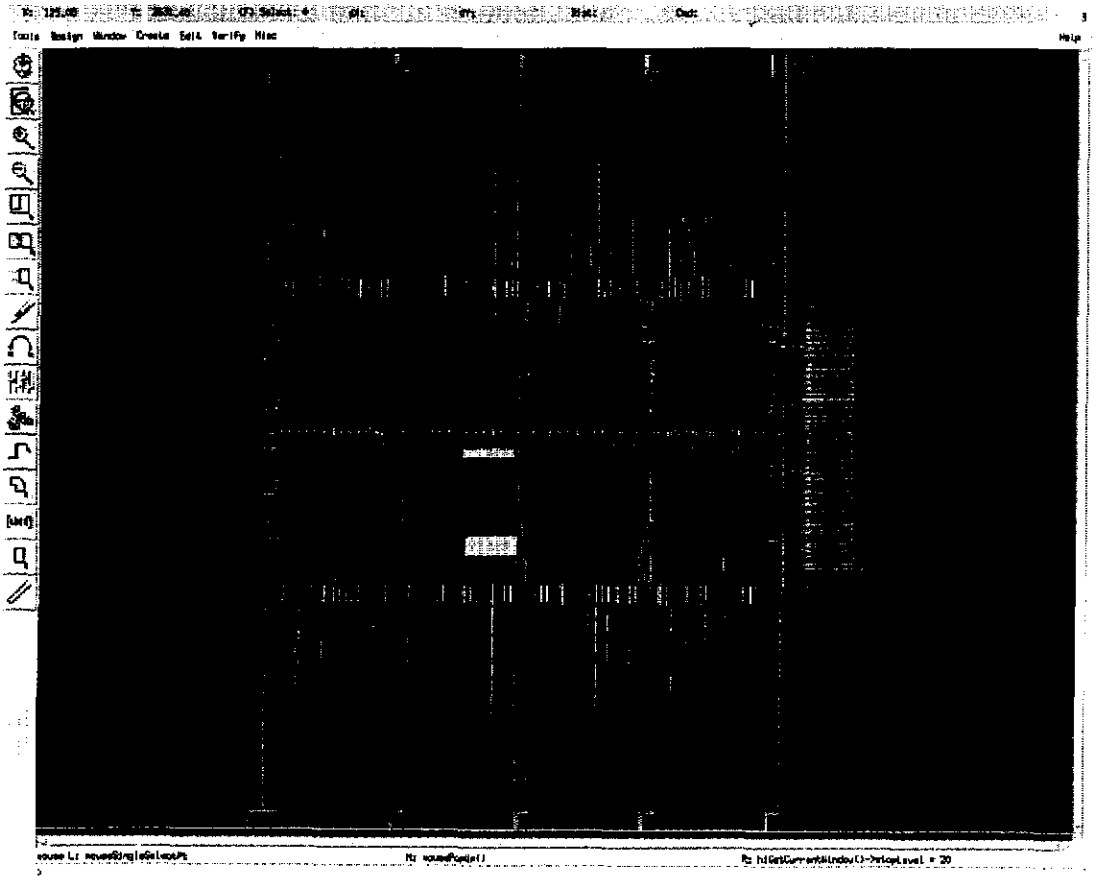


圖八、Verilog 模擬結果

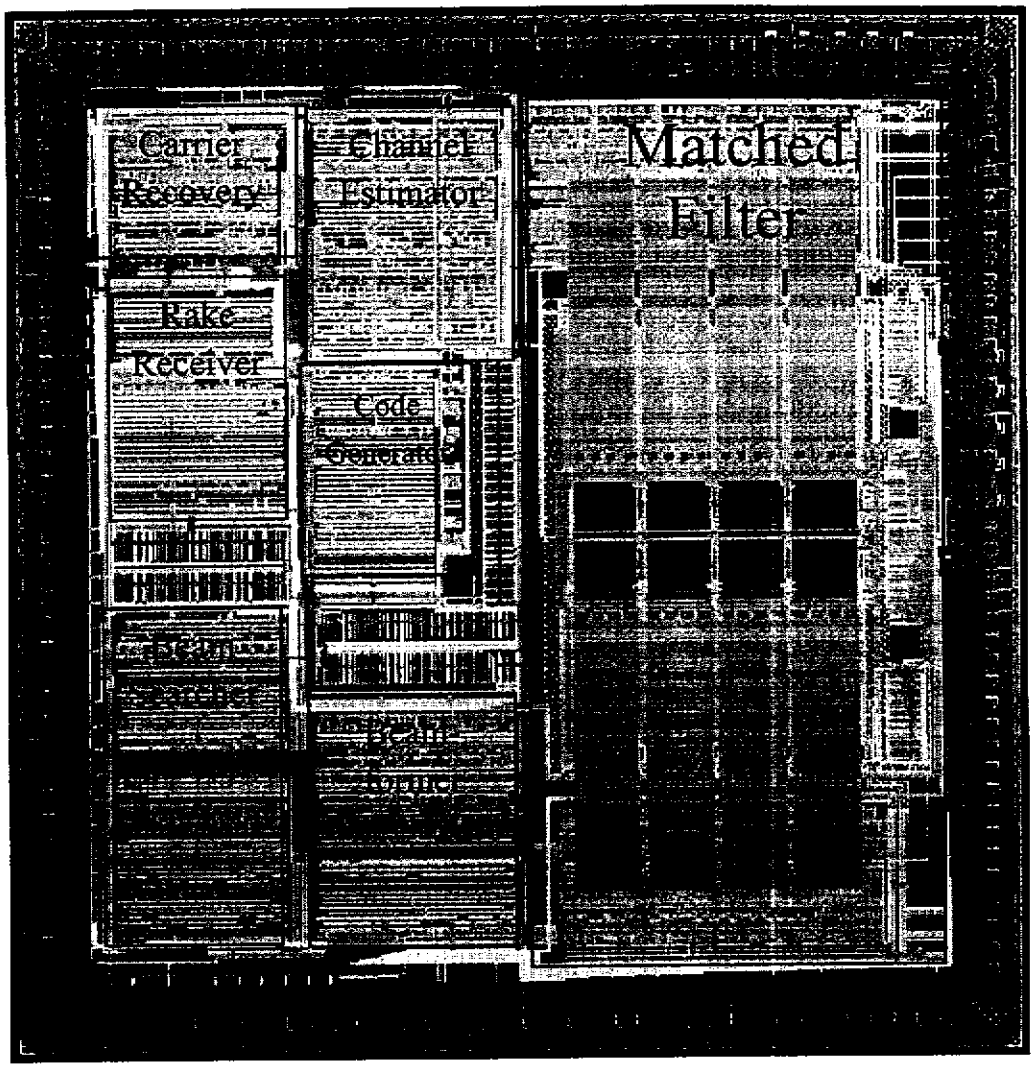


1024-tapped Delay Line based on the Latch-file Structure

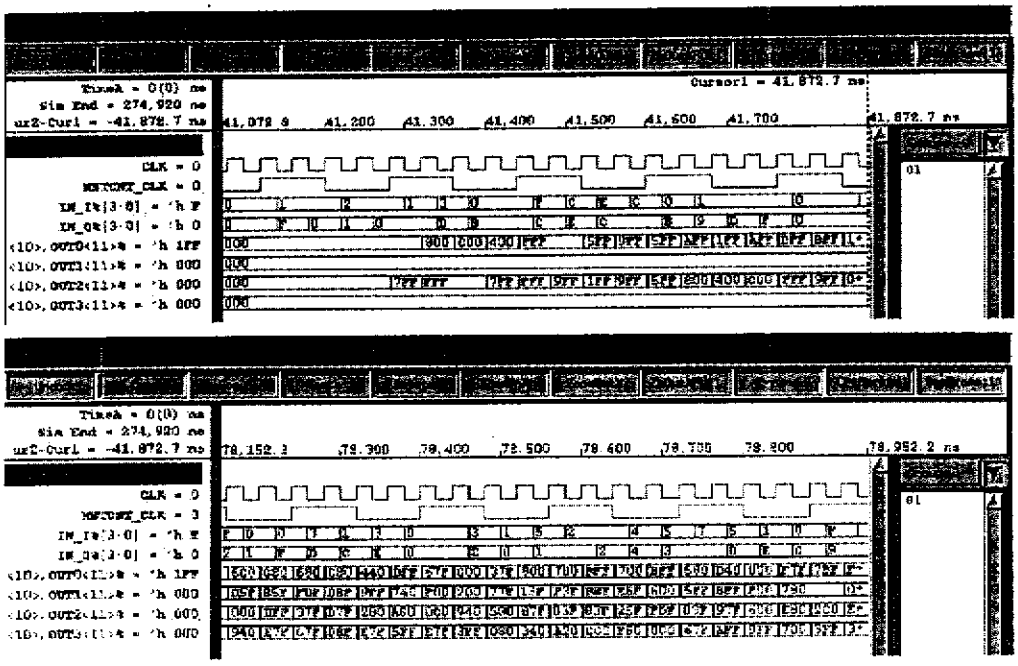
圖九、LatchFile 電路圖



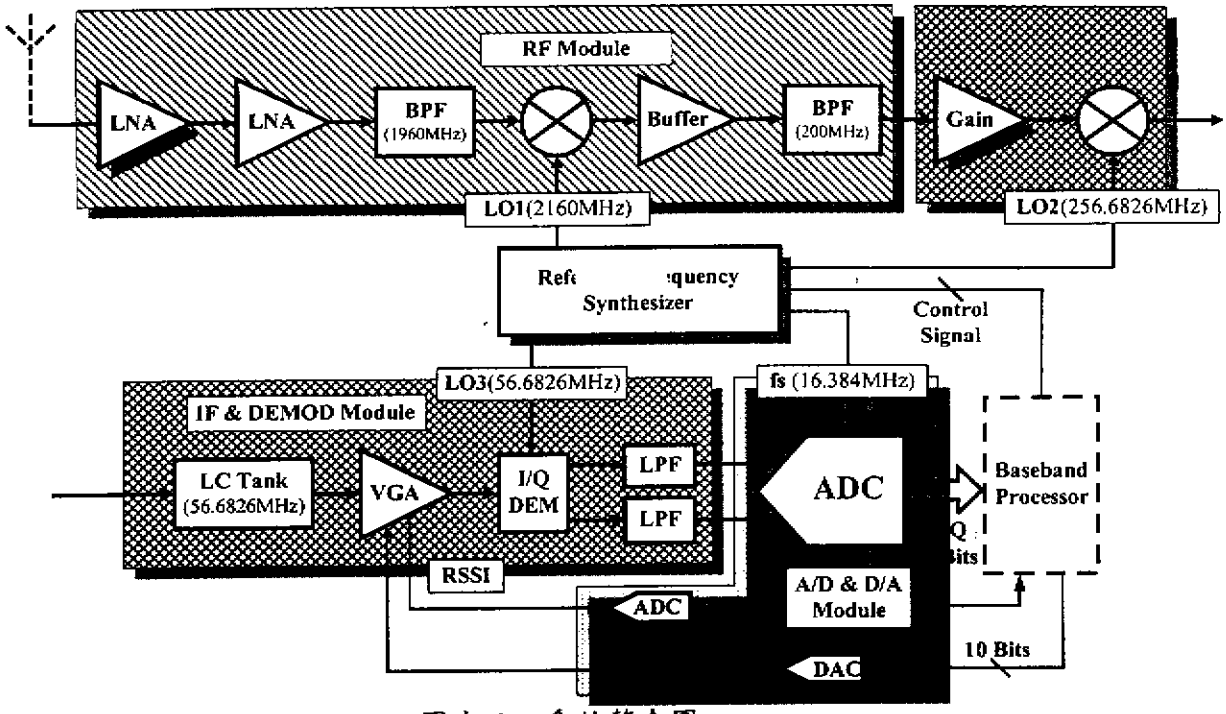
圖十、LatchFile 佈局圖



圖十一、晶片佈局圖



圖十二、Timemill 模擬結果



圖十三、系統整合圖

Signal	Word Length
Beamformer Input	6
Beamformer Weight	6
Beam Searcher Input	6
Beamformer Output	6
NCO output	6
NCO ROM Address Input	8
Pre Filter Input	6
Matched Filter Input	4
Complex Multiplier	6
Atan ROM Input	9
Atan ROM Output	11
Rake Input	6

表一、各重要信號點選取位元數

使用製程	0.35um CMOS 1P4M
包裝種類	144 cqfp
晶片面積	6.5x6.9mm2
電機體/邏輯閘數	644856
最高工作頻率	50MHz

表二、晶片規格

Design and Implementation of an Uplink Baseband Receiver for Wideband CDMA Base Stations

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Abstract

This paper presents architecture design, FPGA implementation, and measurement results of a real-time signal processing circuit for WCDMA uplink baseband receiver. To enhance uplink performance, a four-element antenna array using spatial signature for beamforming (spatial diversity) and a four-finger Rake combiner gathering the most significant multi-path signals (path diversity) are integrated in the proposed receiver. Moreover, a low-complexity beamforming architecture using a correlator-based beam searcher, a decision-directed carrier recovery loop, and a matched-filter based channel estimator are also designed. Simulations are based on the standard Doppler-fading scalar channel models provided by 3GPP and an extension to vector channel models is also made for beamformer simulation. Simulation and hardware emulation results show that the proposed architecture not only meets the specified requirements but also achieves such performance with relatively low hardware complexity.

Index Terms

IMT-2000, WCDMA, Rake receiver, beamformer, diversity receiving.

I. Introduction

Nowadays, digital mobile communication systems are prevalent worldwide for providing data/voice services to mobile users. Nonetheless, current second generation systems are limited in the maximum data rate they can support. Third generation mobile communication (International Mobile Telecommunications-2000, IMT-2000) systems promise to provide more advanced services, such as broadband internet access, video telephony, and video conferencing, in addition to the voice and low-rate data services currently available. The third generation (3G) mobile communication systems are being developed to support a wide range of bearer services with low to high data rates: up to 144 kbps in vehicular, 384 kbps in outdoor low-mobility, and 2 Mbps in indoor environments. Furthermore, 3G systems will operate in various environments, e.g., urban and suburban areas, hilly and mountainous areas, and indoor environments. In other words, 3G mobile communication systems promise to simultaneously achieve two major goals in modern mobile communication: wide-area mobility and high-bandwidth interactivity.

Wideband CDMA (WCDMA), proposed by 3GPP (Third Generation Partnership Project), is one of the major proposals for ITU IMT-2000 RTT (Radio Transmission Technology) standards [1]. In the 3GPP proposal an uplink pilot channel is introduced to improve the system performance. With this sounding pilot signal, rather accurate channel estimation can be achieved. Such information about the channel facilitates implementation of several advanced receiving techniques that help increase the signal to interference and noise ratio (SINR) of the received signal. Since the performance of CDMA system is known to be interference-limited, the more the interference can be suppressed, the more capacity can be achieved.

Among these techniques, multi-user detection (MUD) [2] [3] exploiting the dedicated pilot channel of each user can be adopted for multiple access interference (MAI) elimination. Adaptive antenna array

[4] with a beamformer is another technique that uses pilot channel of each user to form an appropriate beam pattern with the main beam directed toward the desired user and nulls toward other interference sources. Other than the aforementioned interference suppression/cancellation techniques, the pilot channel also facilitates channel estimation required in two other CDMA receiver signal processing functions: Rake combining for diversity receiving in multipath fading channels and carrier recovery for correcting carrier phase/frequency error from local oscillator frequency mismatch and Doppler effect.

In addition, there exists a more sophisticated adaptive antenna architecture, called 2-D Rake receiver [5] [6] [7] [8] [9], which tries to exploit both the path diversity of Rake combiner and the spatial diversity of beamformer. In this architecture, one beamformer is used for each of the estimated incoming paths in a multi-path channel, thus the name 2-D Rake receiver. In a 2-D Rake receiver configuration, sophisticated algorithms are needed for estimating the weights of the beamformers. e.g., direction-of-arrival (DOA) estimation algorithm. These algorithms often involves complex matrix operations. Due to the high computation complexity they demand, matrix-operation-intensive beamforming algorithms and the 2-D Rake receiver architecture are seldom implemented in real-time hardware.

Recently, real-time high-data-rate CDMA system implementation has received much attention from researchers worldwide. In [10], 1.92 Mbps data transmission experiments over a coherent WCDMA mobile link were presented; the implemented receiver adopted antenna diversity reception, Rake combining, and concatenated channel coding to improve transmission performance. A large testbed with many discrete components was used for the receiver implementation in the experiments. In [11] [12], another testbed was constructed for evaluation of the WCDMA technology. In this testbed, the receiver employed again the Rake combining technique and channel coding for successful demonstration of wireless multimedia applications in the field. In [13], a testbed for real-time wireless WCDMA communication was presented. In this testbed, a source codec, a channel codec, and a RF/IF transceiver were implemented. The channel codec contained CDMA baseband processing and convolutional coder/decoder and was implemented using ten FPGA ICs, one for each block. In the baseband processing module, only a simplified correlator with code acquisition was used for demodulation, no diversity receiving techniques were implemented.

A baseband IC for 3G WCDMA communication systems was proposed in [14]. This baseband IC uses a reconfigurable WCDMA transceiver and an embedded microprocessor. The reconfigurable transceiver includes programmable filters, spreader/despreader, matched filter, and FFT hardware for acquisition. Another architecture for WCDMA baseband processing utilized the fact that in a base station, signals are to be processed in different rates: symbol rate, slot rate, and frame rate [15]. So three different engines were adopted for each type of processing. With such general-purposed architecture, different algorithms or CDMA standards can be tested. However, as with most software-based receiver implementation, hardware complexity is higher and circuit optimization for some specific algorithms is not possible.

In this paper, a low-complexity adaptive baseband receiver architecture for uplink WCDMA systems based on 3GPP Radio Access Network (RAN) FDD mode specification [16] [17] [18] and its FPGA implementation are presented. This architecture includes a beamformer that utilizes the spatial signature [19] [20] of the desired signal estimated by the correlator-based beam searchers. The beamformer weights are generated by simple arithmetic manipulation of the spatial signature, and thus the proposed architecture can avoid matrix operations and greatly reduce needed hardware complexity, while still providing a spatial diversity gain. Path diversity receiving is achieved by the Rake combiner, whose weights are derived from the multi-path information obtained by the channel estimator.

The rest of this paper is organized as follows. A system overview of WCDMA proposal and introduction to important uplink channels are given in Section II. System architecture design for the proposed uplink receiver is discussed in Section III. Section IV describes the adopted channel models and the simulation results of the proposed receiver architecture. Then, Section V presents FPGA hardware design and measurement results. Finally, conclusions are given in Section VI.

II. System Overview

The 3GPP RAN specification [16] [17] [18] is based on the code-division multiple access (CDMA) scheme using the direct-sequence spread spectrum technique. The adopted chipping rate is 3.84 Mcps and services with bit rates up to 2 Mbps can be provided. The system uses two levels of spreading: *channelization* and *scrambling*. The former is to uncouple data channels assigned to a particular user by spreading each data channel with a distinct channelization code. In order to support variable data rates, orthogonal variable spreading factor (OVSF) Walsh codes are chosen for channelization codes. The latter spreading is aimed at distinguishing users in one cell. The scrambling codes are complex-valued, and they can be either long codes or short codes.

In 3GPP WCDMA standard, there are three important types of uplink physical channels, Physical Random Access Channel (PRACH), Dedicated Physical Data Channel (DPDCH), and Dedicated Physical Control Channel (DPCCH). PRACH is shared among all User Equipments (UE) in one cell, and the slotted aloha scheme is adopted by the UEs to make random access requests. Figure 1 depicts the random access frame structure and the access slot arrangement. Once the random access request of an UE has been successfully received by the base station (BS), the BS will issue a random access grant message to that UE. This grant message contains essential information for the UE to commence communication with the BS through DPDCH and DPCCH.

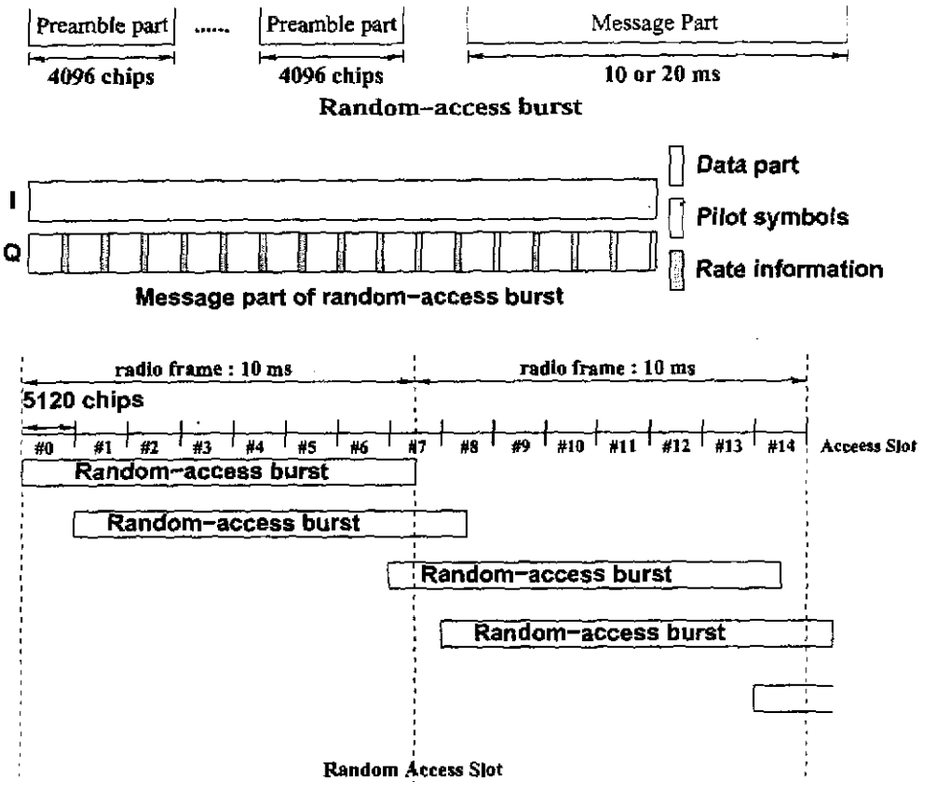


Fig. 1. PRACH frame structure.

Two types of dedicated physical channels (DPDCH and DPCCH) are assigned by the BS to a UE upon granting its random access request. The DPCCH is a control channel, containing pilot signal, Transport Format Combination Indicator (TFCI, data rate information about the current DPDCH frame), Feedback Information (FBI) bits, and Transmission Power Control (TPC) bits. The DPDCH consists of information bit stream from the upper layers and the number of DPDCHs assigned to a particular UE can be more than one according to the services it requests. Figure 2 shows the frame structure of the two dedicated physical channels. Note that the frame structure is similar to that of

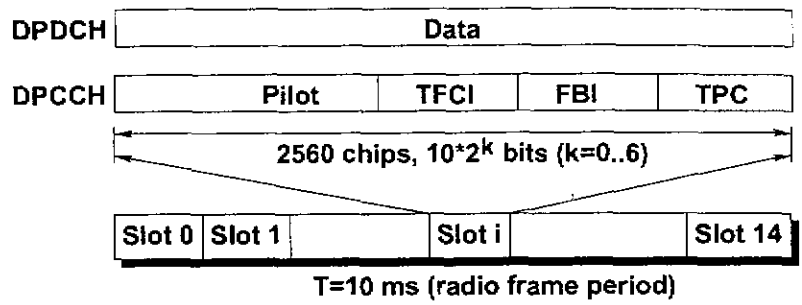


Fig. 2. DPDCH and DPCCH frame structure.

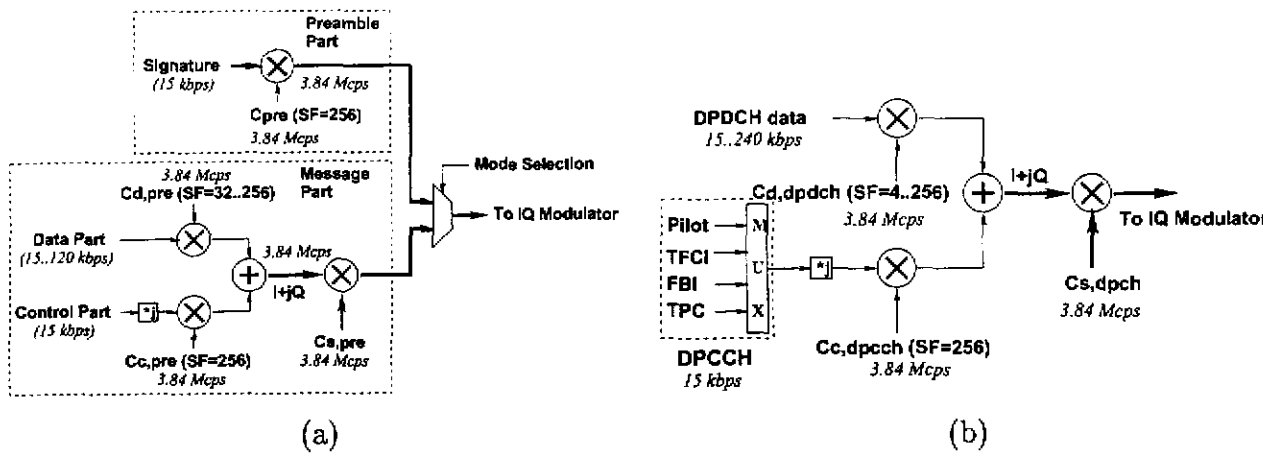


Fig. 3. Transmitter models for (a) PRACH and (b) DPCH.

the message part in PRACH. The spreading factor (SF) of the DPCCH is fixed at 256, while that of the DPDCH can be set to $256/2^k$, where k is an integer from 0 to 6. In other words, the spreading factor ranges from 256 to 4 and the DPDCH physical bit rate runs from 15 kbps to 960 kbps.

III. System Architecture

A. Transmitter

Figure 3(a) illustrates the PRACH transmitter model. To construct the preamble part, a preamble code (**Cpre**), with a spreading factor of 256, spreads the selected signature at a chipping rate of 3.84 Mcps. Until a grant message is issued, the message part will not be transmitted. The message part consists of a data part in the in-phase (I) channel and a control part in the quadrature-phase (Q) channel. They are spread by **Cd,pre** and **Cc,pre** channelization codes, respectively. The two channels are then combined and scrambled by the complex-valued scrambling code (**Cs,pre**).

Figure 3(b) is the DPCH transmitter, and the two dedicated physical channels are allocated in I and Q channels in the same way as the data part and the control part of PRACH. Note as in the message part of PRACH, the DPDCH and DPCCH signals are spread by respective real-valued OVSF codes (**channelization**) and then they together are scrambled by a complex-valued scrambling code (**scrambling**). Moreover, note that depending on the requested services there can be a maximum of six DPDCHs with six distinct channelization codes while there is always only one DPCCH.

B. Receiver

Figure 4 shows the proposed baseband receiver architecture. A four-element antenna array is adopted in the proposed uplink receiver. The baseband receiver takes eight input signals (I and Q channels per antenna element) from the RF/IF module and generates hard decisions or soft decisions for the

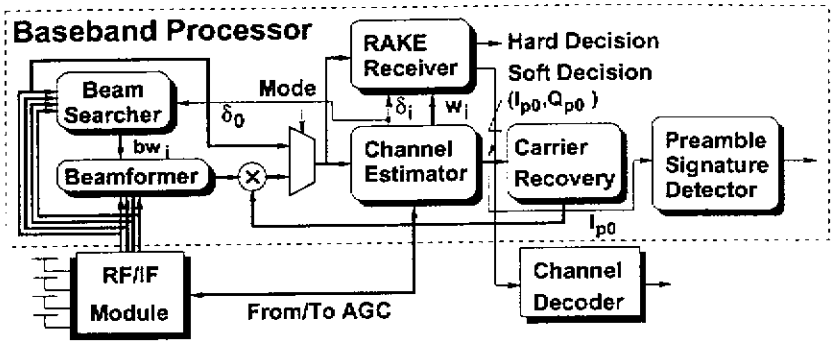


Fig. 4. Proposed WCDMA baseband receiver architecture for PRACH and DPCH.

optional channel decoder. A single baseband receiver architecture can be used for signal detection of all three uplink physical channels mentioned above due to the similarity in transmission scheme of the PRACH message part (data and control part) and the DPCH (DPDCH and DPCCH).

During the preamble of PRACH, the channel estimator is responsible for estimating channel characteristics. A MUX controls whether the input signal of the channel estimator comes from a particular antenna element (during the PRACH preamble) or from the beamformer output (during the PRACH message part and DPCH). A complex matched filter is employed to compute the channel delay profile and the delays (δ_i) and phasors (I_{pi}, Q_{pi}) of significant paths within one symbol period are then estimated by other blocks in the channel estimator. The channel estimation process begins by first passing continuously the I-channel matched filter output of the most significant peak (I_{p0}) to the preamble signature detector to search for a random access request. Once a random access request is identified, the beam searcher then estimates and sets up the beamformer weights (bw_i). Meanwhile, the carrier recovery block keeps track of the phasor of the most significant peak (I_{p0}, Q_{p0}) and estimates the average frequency offset. Note that, in this initial channel estimation phase, the beamformer and the Rake receiver are turned off, and the carrier recovery loop is kept open.

After initial channel estimation, the receiver obtains an approximate configuration of the beamformer, the carrier recovery loop, and the Rake combiner. During receiving the PRACH message part and the DPCCH/DPDCH signal, the beamformer in the proposed receiver begins to operate with these estimated weights (bw_i). In addition, a phase de-rotate block is placed after the beamformer to close the carrier recovery loop and the MUX now points to the lower branch. Following beamforming and carrier phase/frequency correction, the Rake receiver demodulates information bits in the I channel (data part of the PRACH message part and DPDCH) using maximal ratio combining (MRC) [21]. Meanwhile, the channel estimator, the carrier recovery block, and the beam searcher continuously tracks channel fluctuations through detecting pilot signals in the Q channel (the control part of the PRACH message part or DPCCH).

B.1 Channel Estimator

The channel estimator consists of a pre-filter, a complex matched filter, a peak detector, and a weight estimator as shown in Figure 5. With four-sample-per-chip sampling at the baseband receiver input, the pre-filter is used to accumulate four consecutive samples and the accumulated running sum is sent to the complex matched filter. The complex matched filter despreads the input signal, and the peak detector then locates the largest four peaks within one symbol period. To avoid false detection, all peaks with magnitude less than a pre-determined threshold are discarded. The phasor values of these four legitimate peaks are then fed to the weight estimator that calculates the weights (w_i) for the Rake combiner according to

$$w_i \propto b_{pi} \cdot (I_{pi} - jQ_{pi}), \quad i = 0, 1, 2, 3, \tag{1}$$

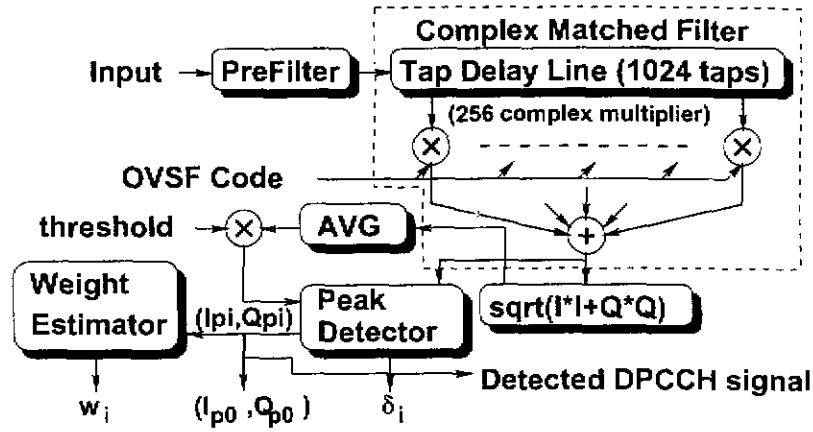


Fig. 5. Block diagram of the proposed channel estimator.

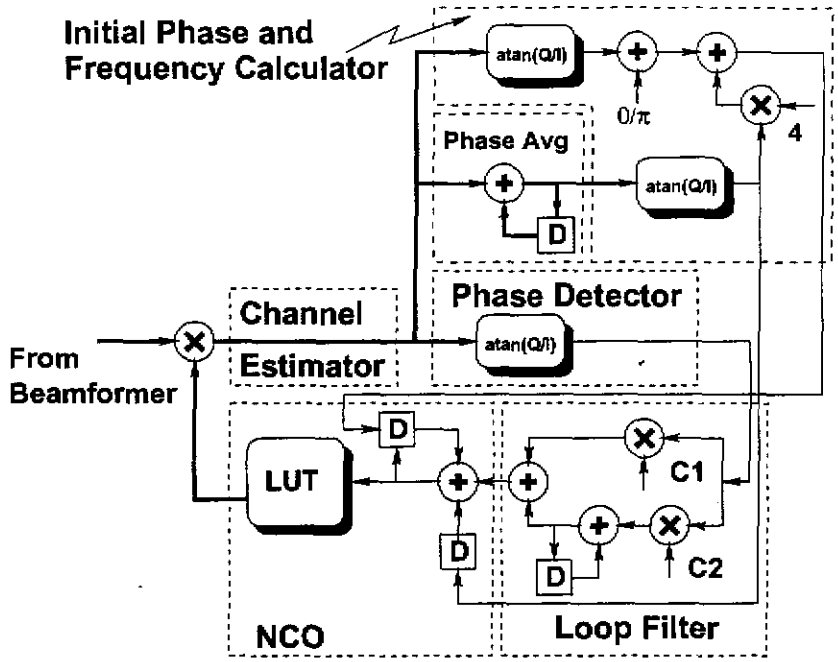


Fig. 6. Carrier recovery circuit.

where b_{pi} is the polarity of the current pilot bit.

B.2 Carrier Recovery Loop

Due to fading and local oscillator frequency mismatch, the phase of the incoming signal must be compensated appropriately. A carrier recovery phase-locked loop (Figure 6) is adopted in the proposed receiver. The loop operates in two modes: acquisition mode and tracking mode. In the acquisition mode, which happens during the reception of the PRACH preamble part, an average of the phase difference between two consecutive symbols is calculated and used as an estimation of the frequency offset. In the tracking mode, enabled during the PRACH message part and DPCCH/DPDCH reception, the whole carrier recovery loop begins to operate.

The phase detector calculates the phase of the most significant peak in the matched filter output (I_{p0}, Q_{p0}) supplied from the channel estimator. The loop filter is a conventional proportional-and-integrate type and a numerical-controlled oscillator (NCO) is adopted in this digital phase-locked loop [22]. In the carrier recovery circuit, the initial phase/frequency calculator operates only once during the PRACH preamble, while the phase detector and the loop filter operate at symbol rate and the

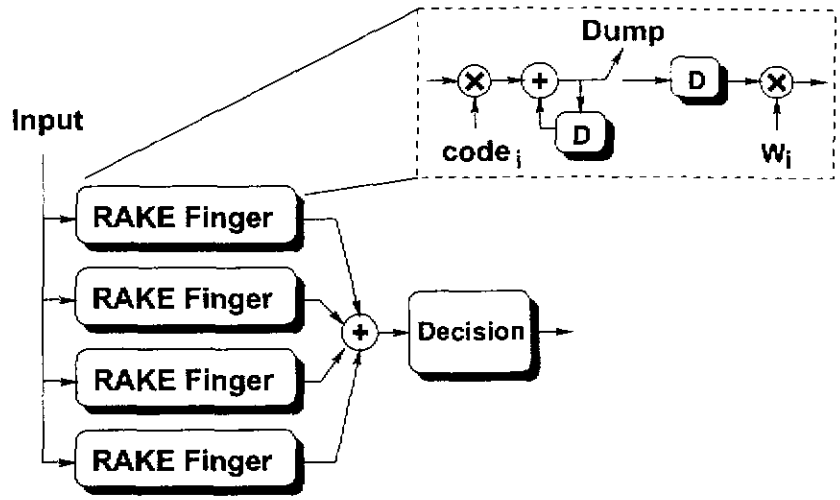


Fig. 7. Rake receiver.

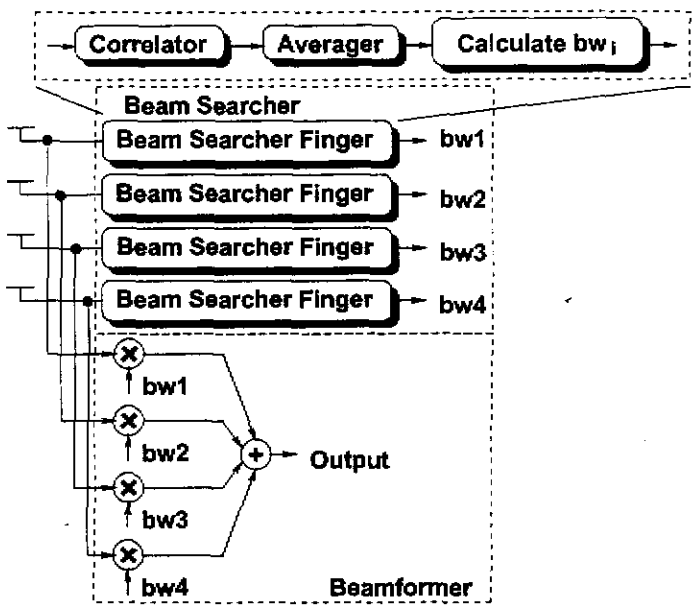


Fig. 8. Block diagram of the beamformer and the beam searcher adopted in the proposed receiver.

NCO outputs a de-rotation phasor at sample rate.

B.3 Rake Receiver

Figure 7 shows the block diagram of the Rake receiver in the proposed receiver. For maximum ratio combining the proposed receiver uses four fingers with weights computed by the channel estimator. Four PN-code correlators, with respective delays computed by the channel estimator, are employed to despread the incoming sample-rate signal into four despread symbol-rate data. By aligning these despread data from all four fingers with the I-axis and then weighted summing the aligned data, one obtains a soft-decision output with optimal SNR [21]. Note that although four fingers are shown here, the actual number of enabled fingers can be adjusted according to the channel condition.

B.4 Beamformer and Beam Searcher

In addition to path diversity exploited by the Rake receiver, spatial diversity receiving can be achieved using an antenna array with some beamforming algorithm [4]. Figure 8 shows the proposed

beamformer and beam searcher architecture. The beam searcher consists of four identical elements, one for each antenna. Each of them utilizes a complex pilot-PN-code despreader (correlator) timed by the most significant peak timing (δ_0) to estimate the relative magnitude and phase of the pilot contained in the baseband signal from each antenna. Since the four antennas are only $\lambda/2$ apart (λ is the wave length of the carrier), the four despread outputs of the pilot contained in a particular path are of the same magnitude, yet with quite different phases. However, in a multi-path fading environment, these four correlator output phasors make up the *spatial signature* of the vector channel pertaining to the transmitter with the pilot PN-code [19] [20].

As in the Rake receiver, these four complex baseband signals can be constructively combined if only they can all be aligned to a certain reference before they are summed. Thus the beamformer weights (bw_i) are first initialized to the complex conjugate of the spatial signature obtained during PRACH. To provide robustness against impulsive channel distortion, the beamformer weights are updated using moving average of the complex conjugate of the estimated spatial signature and are given by

$$bw_i^{\text{new}} = (1-\alpha)\cdot bw_i^{\text{old}} + \alpha\cdot(I_{b,pi} - jQ_{b,pi}), \qquad i = 0,1,2,3, \tag{2}$$

where α is a small positive constant and $(I_{b,pi}, Q_{b,pi})$ is computed by the ith beam searcher using the pilot PN-code correlator (despreader) on the complex-valued baseband signal from the ith antenna. an average of spatial signature is used for computing the beamformer weights. The beamformer then uses these weights to combine the four complex-valued baseband signals from the antenna array, effectively steering the antenna beam pattern toward the desired direction.

IV. Simulation Results

In this section, we will present results of the proposed receiver architecture simulation, including those using floating-point arithmetic and fixed-point arithmetic. The 3GPP WCDMA transmitter output signal is passed through a channel model, and then the channel output is fed to the proposed WCDMA receiver. The channel model used is based on a four-ray Doppler fading test channel specified in the 3GPP standard [23]. The relative speed between the transmitter and the receiver is 120 km/h, moreover, a carrier frequency offset of 200 Hz (0.1 ppm relative to the 2 GHz RF frequency) and an input SNR of -6 dB are assumed.

A. Floating-Point Functional Simulation

A.1 PRACH Preamble Part

The reception of WCDMA signal in the base station begins with detection of the PRACH preamble sent by a UE. Therefore we first feed some PRACH preamble frames to the proposed receiver. The simulation results of this test are illustrated in Figure 9. Horizontal axis of all figures are in T_s, the sampling interval. Figure 9(a) depicts the matched filter output, which clearly shows periodic peaks. The signs of these peaks, as shown in Figure 9(c), can then be matched against the preamble signature. The signature matching result is shown in Figure 9(b) and at the end of the simulation a RAQ (Random Access Request) is detected (Figure 9(d)).

A.2 Carrier Recovery Loop

Figure 10 shows the simulation results of the carrier recovery loop working in the tracking mode during receiving the message part of a PRACH frame. The detected complex-valued output symbols are plotted in Figure 10(a). It is clear that the detected symbols are limited to two clusters (BPSK) since the carrier recovery loop has been initialized with values acquired during preamble detection. It can also be seen that the phase error converges to within a small range around zero (Figure 10(b)) and the carrier recovery loop is in phase lock with a 200-Hz offset frequency specified in the channel model.

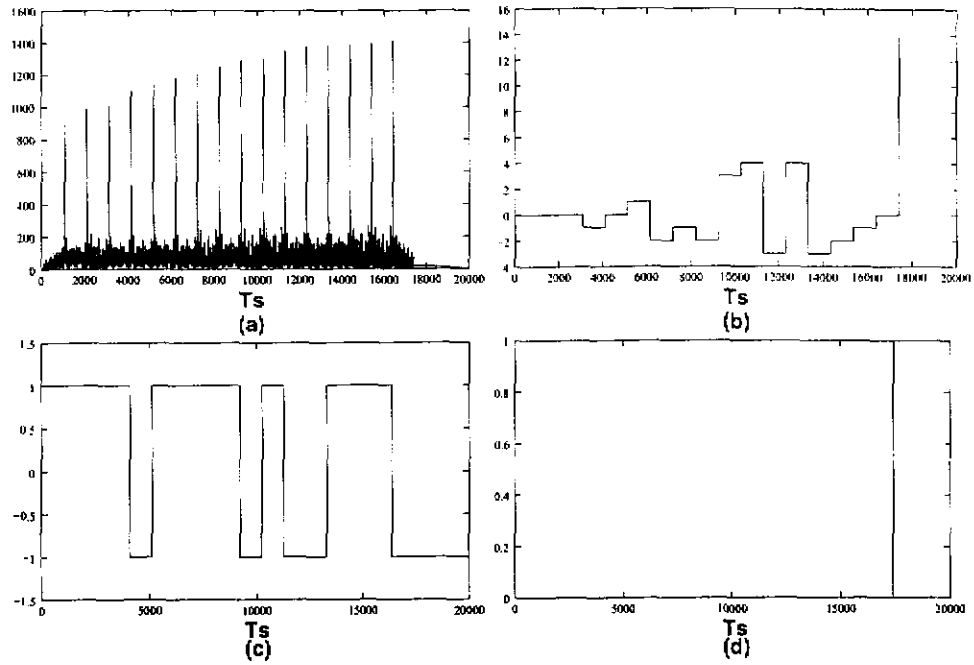


Fig. 9. PRACH preamble detector simulation results. (a) Output magnitude of the matched filter in the channel estimator. (b) Preamble signature detector correlator output. (c) Signs of the largest peak at the matched filter I-channel output (I_{p0}). (d) Preamble detection signal waveform indicating a random access preamble is detected.

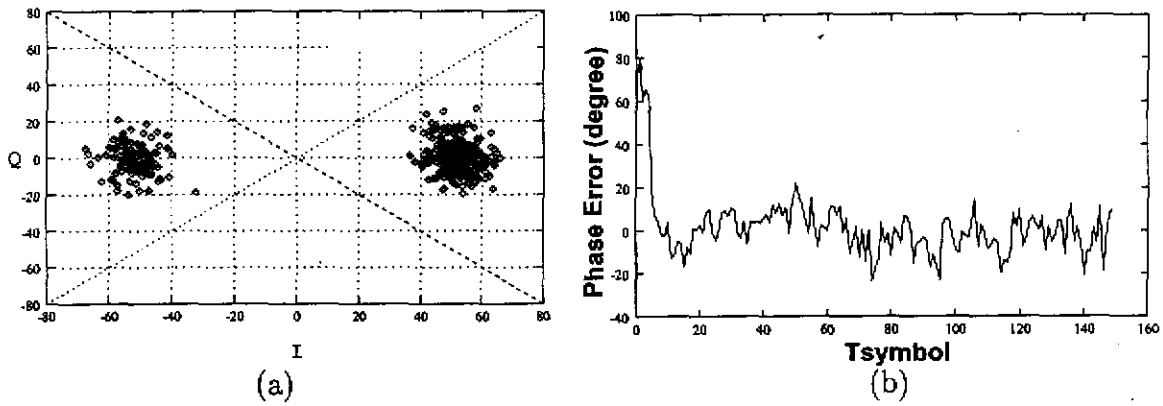


Fig. 10. PRACH message part detection: (a) I-Q plot of the detected output symbols and (b) detected phase error.

A.3 Beamformer

To verify the function of the proposed beam searcher and beamformer, we simulate a multi-user scenario and use a vector channel extended from the original scalar channel model. The outputs of this vector channel are then used as the four complex-valued baseband inputs of the beam searcher and the beamformer. Two cases are simulated: one with only one interfering user and the other with ten. In both cases perfect power control among users is assumed. The simulation is performed under the assumptions that all users have four paths and are traveling at 120 km/h [23]. All four paths of a user are from different angles of a predetermined angle spread (20 degree as suggested in [2] for urban cells), and the frequency offset is 0.1 ppm and the input SNR is -6 dB.

Figure 11 illustrates the equivalent antenna pattern according to the beamformer weight setting found by the beam searcher during PRACH preamble detection. It is clear that in all four cases the beamformer always forms an antenna pattern with the main lobe pointing toward the desired user,

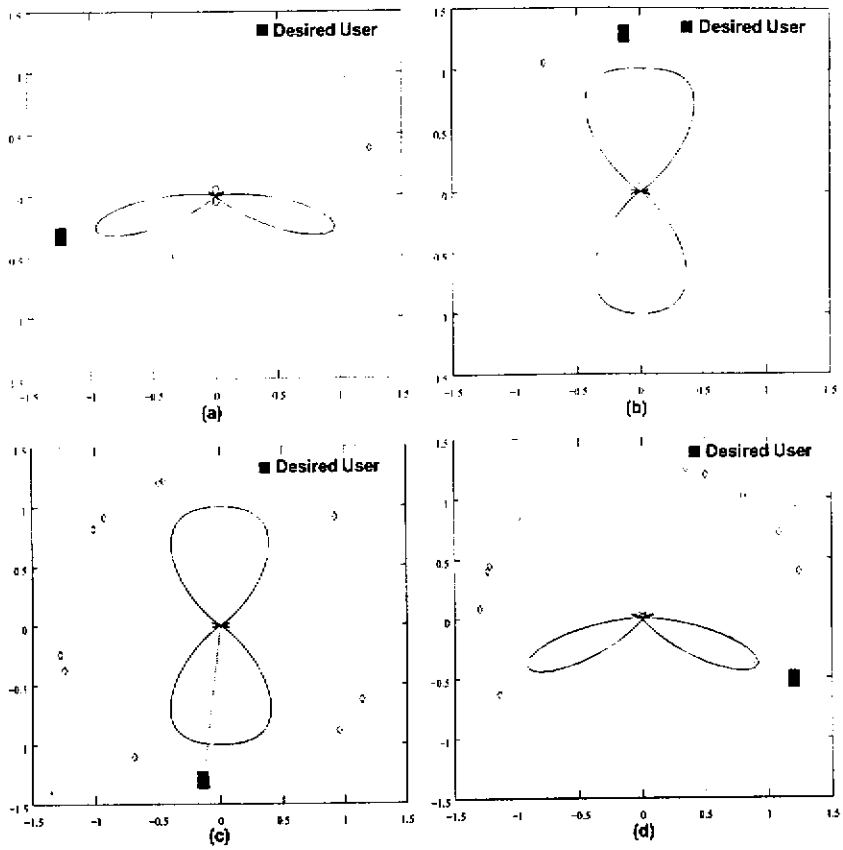


Fig. 11. Simulated antenna patterns of the beamformer. (a)(b) One desired user and one interfering user. (c)(d) One desired user and ten interfering users.

which effectively achieves spatial diversity receiving and greatly reduces multiple access interference (MAI) level.

Figure 12 illustrates the effectiveness of suppressing multiple-access interference (MAI) with the technique of beamforming. In a simulation with two users: one desired and one interferer. The peak magnitude of the matched filter output with beamformer enabled (Figure 12(b)) increases about four folds when compared with when the beamforming is turned off (Figure 12(a)). In another simulation with ten interfering users, the result without beamforming (Figure 12(c)) shows that the matched filter in the channel estimator fails, i.e., no peak can be detected during the message part. On the contrary, with the aid of the proposed beamformer, the receiver can detect pilot signal of the desired user's PRACH message part owing to the 6-dB diversity gain and MAI suppression (Figure 12(d)). Furthermore, note that the magnitude of the detected peaks fluctuate due to the fast fading assumption of the desired user (a 223-Hz Doppler frequency).

B. Fixed-Point Simulation

Two goals are to be achieved through fixed-point simulation of the proposed receiver: 1) to reduce the hardware cost by using the minimum word length for each signal in the receiver; 2) to maintain the overall performance. In other words, through fixed-point simulation we can evaluate the influence on the system performance brought about by the quantization noise introduced when making finite the word length of crucial signals in the receiver. Since it will take excessively long simulation time if the bit error rate is used as the performance index, we thus use the output SNR as a gauge of the system performance [24]. The output SNR in our simulation is defined as

$$SNR = 10 \log_{10} \frac{\mu^2}{\sigma^2}, \tag{3}$$

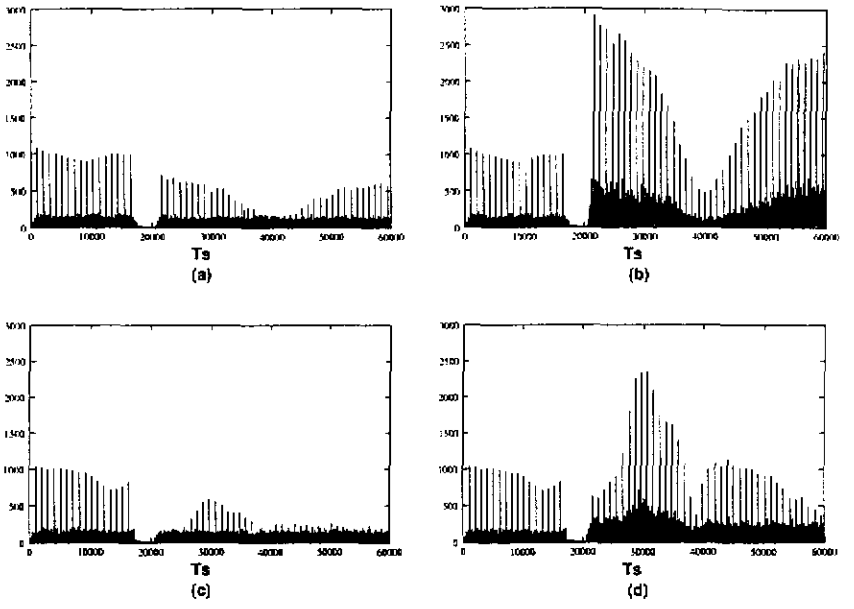


Fig. 12. Matched filter outputs with and without beamforming. (a) one interfering user without beamforming, (b) one interfering user with beamforming, (c) ten interfering users without beamforming, and (d) ten interfering users with beamforming.

TABLE I

SIGNAL WORD LENGTH USED IN THE PROPOSED WCDMA RECEIVER ARCHITECTURE.

Signal	Word Length	Signal	Word Length
Beamformer Input	6	Pre Filter Input	6
Beamformer Weight	6	Matched Filter Input	4
Beam Searcher Input	6	Complex Multiplier	6
Beamformer Output	6	Atan ROM Input	9
NCO Output	6	Atan ROM Output	11
NCO ROM Address Input	8	RAKE Input	6

where

$$\mu = \frac{1}{n}\sum_{k=1}^{n} |I_{p0,k}|, \tag{4}$$

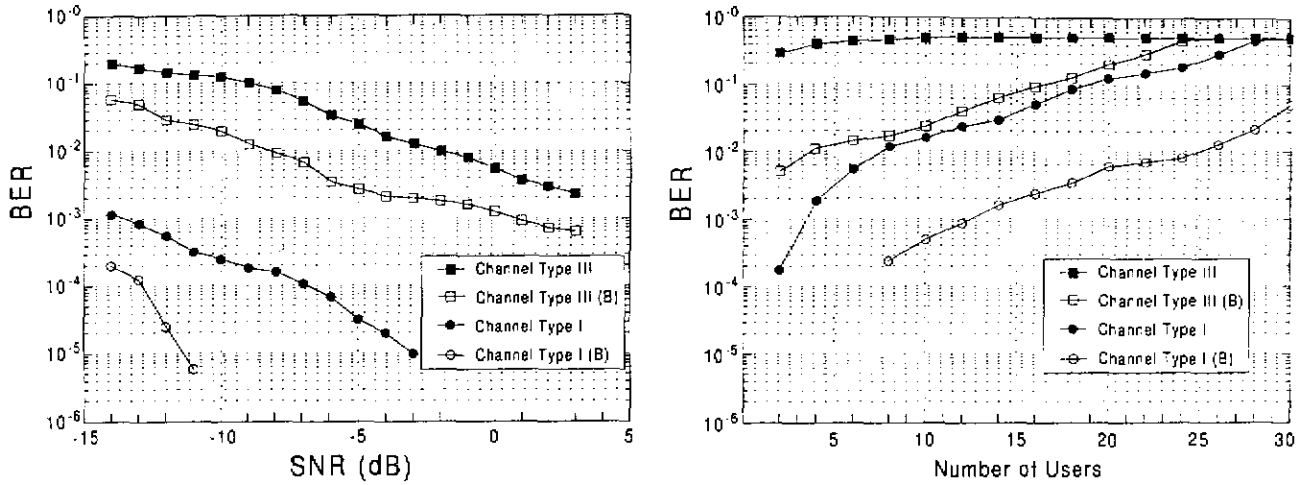
$$\sigma^2 = \frac{1}{n-1}\sum_{k=1}^{n} |I_{p0,k}|^2 - \mu^2, \tag{5}$$

where $I_{p0,k}$ is the I-channel component of the most significant peak in the complex matched filter output when the kth symbol is being estimated by the channel estimator.

In the fixed-point simulation, crucial receiver signals adopt various combinations of possible word length. After careful examination of the simulation results, we then decide the most appropriate word length of some signals in the proposed receiver. The are listed in Table I list the word length of major signals adopted in the proposed WCDMA receiver architecture.

C. Receiver Performance Simulation

The conditions used in the receiver performance simulation are identical to those in the previous beamformer simulation, i.e., 120-km/h four-path multipath fading channel, 20-degree angle spread, and 0.1-ppm frequency error. All users use a spreading factor of 64, which is equivalent to a channel bit rate of 60 kbps. However, in this simulation we do not assume perfect power control since the



(a) (b)

Fig. 13. System performance simulation results under two multipath fading channels with and without beamforming: (a) BER v.s. SNR and (b) BER v.s. the number of interfering users. Type-I channel is a two-ray 3-km/h Doppler fading channel; and type-III channel is a four-ray 120-km/h Doppler fading channel. The curves labeled with (B) refer to the cases with the beamformer turned on.

effect of multiple-access interference is to be investigated. In the MAI simulation, the desired user is under Doppler fading and its power can go as low as -10 dB relative to that of the interfering users and the SNR used is 0 dB. In addition, we also simulated the cases using another slow-fading two-path channel specified in the 3GPP standard [23]. Following the terminology in the standard, the slow-fading two-path and the fast-fading four-path fading channels are named type-I and type-III, respectively.

The simulated performance under different noise and multiple-access interference levels are illustrated in Figure 13. Note that the curves labeled with (B) correspond to the cases with the beamformer turned on. From the Figure 13(a), it is clear that the proposed receiver provides a satisfactory uncoded receiver performance (BER on the order of 10^{-2}) at SNR around -10 db (about 8-dB Eb/No with a processing gain of 18 dB) for the worst-case type-III channel.

Figure 13(b) exhibits another performance enhancement introduced by beamforming. Again, with the help of beamforming, the system performance is greatly enhanced and up to about 30 users can be accommodated in the slow-fading two-ray type-I test channel (BER on the order of 10^{-2}). For the worst-case type-III test channel (120-km/h, four-ray), approximately 10-15 interfering users can be tolerated even though the desired user's power can be as low as -10 dB relative to that of the interfering users.

V. FPGA Implementation

To verify the feasibility of the proposed low-complexity uplink baseband receiver architecture for WCDMA base station, we implement the architecture using several FPGA ICs. In this hardware emulation, four 100K-gate FPGA devices (EPF10k100A) are used. In order to route the signals among the FPGAs in a fast and flexible way, an emulation board with field-programmable interconnection capability (Figure 14) is adopted. On this emulation board, connections between the components are programmable. In addition, an on-board clock buffer is included for low-skew clock distribution.

A. Circuit Design Considerations

By far the largest module of the proposed receiver is the complex-valued matched filter in the channel estimator. Due to the large spreading factor used in the preamble and pilot bits (256), the tap delay lines in the matched filter require a very large number of registers. Unfortunately, registers implemented

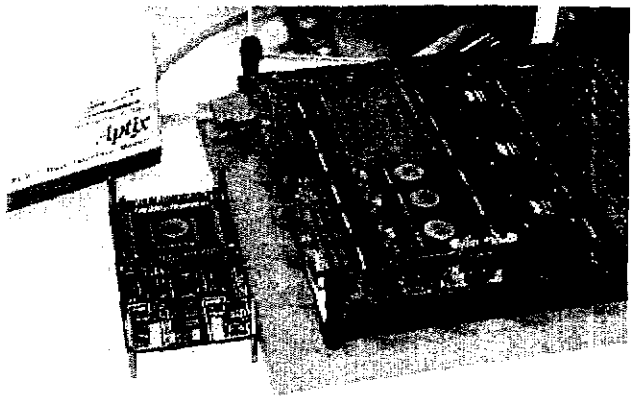


Fig. 14. Emulation environment for receiver implementation.

in an FPGA take up much resource and make the utilization of the FPGA quite poor. Even though implementing the delay lines using the SRAM block in the FPGA is also possible, nontheless this approach greatly limits the speed of the matched filter and thus is not adopted.

Proper pipelining is also necessary since the whole system is partitioned into four FPGA chips and inter-device communication generates long delay and timing uncertainty. With proper pipelining, not only the clock skew problem can be solved but also the system speed can be increased. The operation speed of the emulated WCDMA receiver is 15.36 MHz, four times the 3.84-MHz sample rate. In other words, the FPGA receiver implementation can achieve the speed required by the 3GPP WCDMA standard. Due to a resource limitation of FPGA chips, the beamformer and the beam searcher were not implemented in the hardware emulation. However, the emulation results serve as a solid foundation for future application-specific integrated circuit (ASIC) implementation of the whole WCDMA receiver. The receiver was mapped to four FPGA chips with about 50% hardware used for the complex-valued matched filter in the channel estimator. The rest of the channel estimator and the carrier recovery loop circuit make up 20% of the FPGA hardware, while the phase de-rotator, pre-filter, digital AGC, and the Rake combiner occupy about 30% of the hardware.

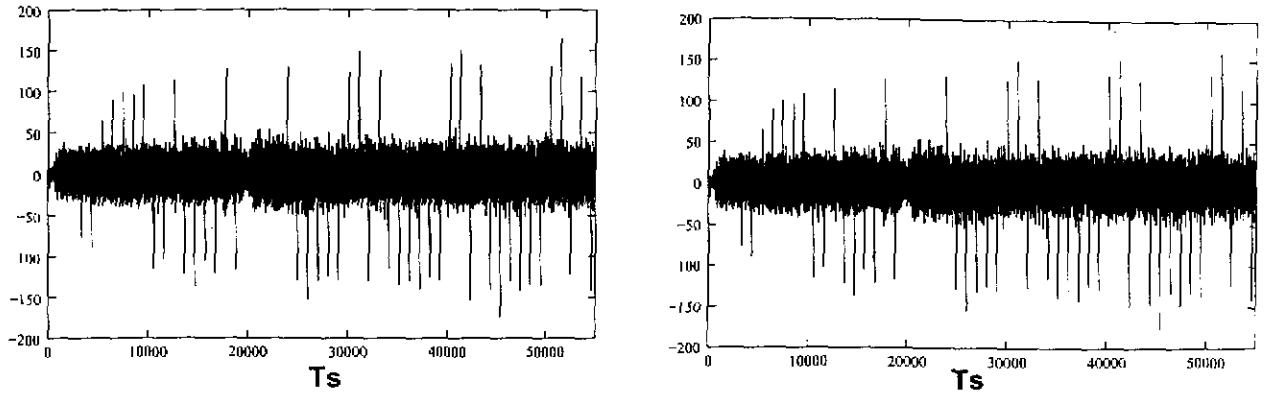
B. Measurement Results

B.1 Matched Filter

In Figure 15, both verilog simulation result and logic analyzer measurements of the receiver implemented in FPGAs are shown. The experiment is for receiving the preamble part and the message part of a PRACH frame. The horizontal axis is the time index in sample intervals (T_s). The curves shown are the despread I-channel output of the matched filter. Note that the two curves are identical since all signals are digitally processed, thus no degradation is introduced by the mapping from the verilog design to the FPGA implementation. In the curves, there are periodical peaks, each 1024 samples (256 chips) apart. The first 16 peaks indicate the 16 preamble symbols of the PRACH preamble part. Note that the signs of these 16 peaks (- - + + + + + - - + - - - - + -) are exactly the reverse of the 16-bit signature of the PRACH preamble (due to initial phase difference between the transmitter and the receiver) and that the peaks' amplitude fluctuate (due to a lack of carrier synchronization and fading).

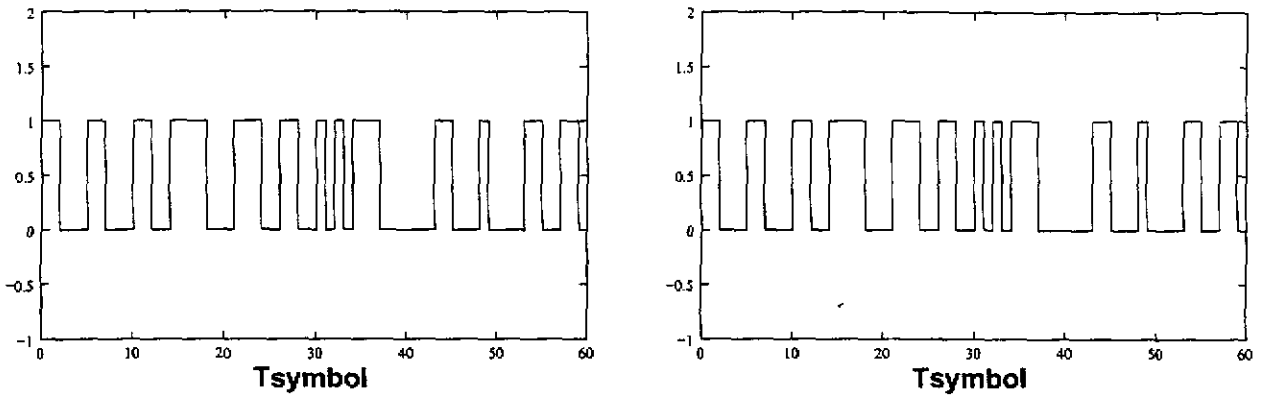
B.2 Detected Data

Figure 16 depicts a segment of demodulated hard-decision output stream. Again both the verilog simulation and the FPGA emulation measurement results are shown and they are identical. In our emulation, due to the memory limitation of the logic analyzer, only less than 63000 samples (about 61 symbols with a spreading factor of 256 and four samples per chip) can be emulated. The FPGA-



(a) (b)

Fig. 15. Comparison of simulation and emulation results of the complex matched filter outputs during the preamble and the message part of a PRACH frame. (a) Verilog simulation results and (b) logic analyzer measurements.



(a) (b)

Fig. 16. Comparison of simulation and emulation results of receiver decision outputs during the message part of a PRACH frame. (a) Verilog simulation results and (b) logic analyzer measurements.

implemented receiver is able to detect without error all the emulated bits in a PRACH message part under a single-user Raleigh Doppler fading channel with 200-Hz frequency offset and 0-dB SNR.

VI. Conclusions

In this paper, an uplink baseband receiver architecture conforming to the 3GPP RAN FDD-mode WCDMA standard is proposed. This architecture includes a beamformer using correlator-based beam searcher, a four-finger Rake combiner, a matched-filter-based channel estimator, and a carrier recovery loop. Simulations were conducted based on two Doppler-fading multipath channel models specified in the 3GPP standard document. Moreover, in order to test the advanced features provided by the proposed beamformer, vector channel models derived from the scalar channels described in the standard were also used. The simulation results showed that the proposed beamforming receiver architecture can accommodate up to 15 users with 60-kbps channel bit rate at a frequency offset of 200 Hz (0.1ppm of the RF carrier frequency), an SNR of 0 dB, a speed of 120 km/h, and the desired user's power as low as -10 dB relative to that of the interfering users. In addition, the beamformer is a linear combiner with its weights generated by a low-complexity correlator-based beam searcher, making the proposed receiver architecture much less complicated than the traditional direction-of-arrival-based beamforming approach.

FPGA emulation of the proposed architecture was also conducted. The emulation can operate at a sample rate of 15.36 MHz, as fast as that specified by the standard. Moreover, the measured results show identical performance to those obtained in the circuit simulation, verifying the feasibility of the proposed architecture. Therefore, we believe that the proposed architecture serves as a solid foundation for future cost-effective application-specific integrated circuit (ASIC) implementation of the baseband processing circuit in a WCDMA base station receiver.

REFERENCES

[1] 3GPP TSG RAN WG1. *Physical Channels and Mapping of Transport Channels onto Physical Channels (FDD)*, TS 25.211 v3.4.0, October, 1999

[2] S. Verdú, *Multiuser Detection*, Cambridge University Press, 1998.

[3] D. Koulakiotis and A. H. Aghvami, "Data Detection Techniques for DS/CDMA Mobile Systems: A Review," *IEEE Personal Communications*, Vol. 7, No. 3, June 2000, pp. 24-34.

[4] T. S. Rappaport. *Smart Antennas for Wireless Communications: IS-95 and Third Generation CDMA Applications*. Prentice Hall, NJ, 1999.

[5] A. Morrison, and B. S. Sharif, "A Space-Time Beamforming RAKE Receiver for Third Generation Wideband CDMA Base Stations," *IEEE International Conference on Consumer Electronics*, pp. 312–313, 1999.

[6] X. Mestre, J. F. Fonollosa, and G. Vazuqez, "Uplink Beamforming for the FDD Mode of UTRA," *VTC 99*, vol. 49(1), pp. 867–871, 1999.

[7] X. Mestre. M. Najar, and J. F. Fonollosa, "Joint Beamforming and Channel Estimation for Pilot-Aided WCDMA Systems," *ICCASPP 2000*, vol. 5, pp. 2577-2580, 2000.

[8] K. H. Chang, I. S. Sohn, and K. S. Chang, "Chip-Level 2-D RAKE Receiver with Symbol-Level Searcher Beamforming," *VTC 99*, vol. 50(2), pp. 924–928, 1999.

[9] E. S. Shin, and Y. O. Park, "Design and Analysis of a Smart Antenna System for IMT-2000 W-CDMA," *VTC 99*, vol. 49(3), pp. 2109–2112, 1999.

[10] K. Okawa, Y. Okumura, M. Sawahashi, and F. Adachi, "1.92 Mbps Data Transmission Experiments Over a Coherent W-CDMA Mobile Radio Link," *VTC 98*, vol. 48(2), pp. 1300–1304, 1998.

[11] M. Ewerbring, J. Farjh, and W. Granzow, "Performance Evaluation of a Wideband Testbed Based on CDMA," in *VTC 97*, vol. 2, pp. 1009-1013, 1997.

[12] M. Sundelin, W. Granzow, and H. Olofsson, "A Test System for Evaluation of the WCDMA Technology," *VTC 98*, vol. 48(2), pp. 983–987, 1998.

[13] H. Park, *et al.*, "Implementation and Performance Analysis of Programmable Test Beds for Real-Time Wireless W-CDMA," *ISCAS 99*, vol. 4 pp. 386-389, 1999.

[14] L. Philips, N. Lugil, and J. Vanhoof, "A Baseband IC for 3G UMTS Communications," *VTC 99*, vol. 50(3), pp. 1521–1524, 1999.

[15] M. Suzuki, M. Kawabe, and N. Doi, "A Proposal of New Architecture for W-CDMA Baseband LSI," *VTC 99*, vol. 49(3), pp. 1540–1544, 1999.

[16] 3GPP TSG RAN WG1, *Multiplexing and Channel Coding (FDD)*, TS 25.212 v3.4.0, October, 1999

[17] 3GPP TSG RAN WG1, *Spreading and Modulation (FDD)*, TS 25.213 v3.3.0, October, 1999

[18] 3GPP TSG RAN WG1, *Physical Layer Procedures (FDD)*, TS 25.214 v3.4.0, October, 1999

[19] S.-S. Jeng, G. Okamoto, and G. Xu, "Experimental Evaluation of Smart Antenna System Performance for Capacity Improvement," *GLOBECOMM '97*, vol. 1, pp. 369–373, 1997.

[20] S.-S. Jeng, Okamoto G.T., G. Xu, H.-P. Lin, and Vogel W.J., "Experimental Evaluation of Smart Antenna System Performance for Wireless Communications," *IEEE Transactions on Antennas and Propagation*, vol. 46(6), pp. 749–757, June 1998.

[21] T. S. Rappaport, *Wireless Communications: Principles and Practice*, Prentice Hall, NJ, 1996.

[22] W. F. Egan, *Phase-Lock Basics*, John Wiely & Sons, Inc., 1998.

[23] 3GPP TSG RAN, *Base Station Conformance Testing (FDD)*, TS 25.141 v3.3.0, October, 2000.

[24] J. K. Holmes, *Coherent Spread Spectrum System*, New York: Wiley, 1982.