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CMOS four-quadrant multiplier using triode transistors based on regulated cascode structure

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Indexing terms: CMOS integrated circuits, Multiplying circuits

A new CMOS four-quadrant multiplier consisting of two MOS transistors operated in the triode region with regulated cascode structures is introduced. This circuit employs the essential property that MOS transistors are bi-directional (or symmetric) devices. Simulation results show that for supply voltages of ±3V, this circuit has <1% linearity error for a differential input range up to ±1.8V. Total harmonic distortion (THD) with a 1.8V (peak) input signal at either input terminal with a ±1.8V DC voltage at the other terminal is less than 1%. The simulated -3dB bandwidth of this multiplier is ~17MHz.

Introduction: Recently, researchers have focused on realising triode transconductor-multiplier circuits based on the regulated cascode (RGC) [1] structure of MOS transistors [2– 7]. However, the RGC-structure triode multipliers reported to date require a core of four MOS transistors operated in the triode region [3, 6]. In this Letter, we propose the use of only two triode MOS transistors with the RGC structure to implement the multiplier that has a much simpler configuration than those of [3, 6] by using the inherent property that MOS transistors are bi-directional (or symmetric) devices. Additionally, all the MOS transistors of this multiplier do not require individual wells and thus a saving of chip area results.

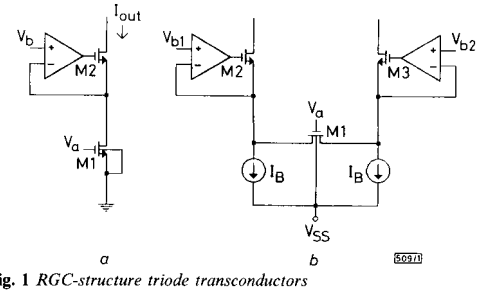

Fig. 1 *RGC-structure triode transconductors*

a Well-known RCC structure [3, 4]
b Modified bi-directional RGC structure

Design principle: Fig. 1*a* shows the schematic diagram of a CMOS triode transconductor [3, 4], based on the well known RGC structure [1]. In this circuit, the differential amplifier forces the drain of M1 to follow V_b. If $V_b < V_{Dsat} = V_a - V_T$, M1 will operate in the triode region so that I_{out} is linearly proportional to V_a, with a transconductance that is linear in V_b. As was shown in [3], four of these transconductors can be combined with a current mirror to form a four-quadrant multiplier. A similar multiplier is also described in [6] by introducing level shifters into the RGC circuits. Note that those RGC-structure triode multipliers require a core of four MOS transistors operated in the triode region to create four-quadrant multiplication. The general arrangement of the proposed CMOS four-quadrant multiplier is illustrated in Fig. 2. The principle of this multiplier can be recognised as follows. First, the RGC-structure triode transconductor of Fig. 1*a* can be modified into Fig. 1*b* to allow bi-directional current flow through M1. Then, two of these modified bi-directional RGC-structure triode transconductors are connected in series to form the circuit of Fig. 2, where DA3, M5 and IB3 are the shared common portion of these two RGC-structure circuits. From Fig. 2, it is clear that both M1 and M2 can conduct currents in either direction depending on the voltage polarity of V3 and V4. Suppose that both M1 and M2 operate in the triode region; then

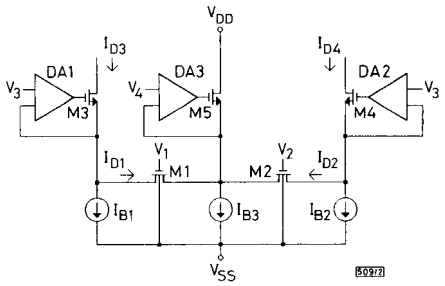

Fig. 2 *General arrangement of proposed CMOS four-quadrant multiplier*

$$I_{d3} = I_{B1} + I_{d1} = I_{B1} + 2K_1[(V_{GS1} - V_{T1})V_{DS1} - \frac{1}{2}V_{DS1}^2] \quad (1)$$

and

$$I_{d4} = I_{B2} + I_{d2} = I_{B2} + 2K_2[(V_{GS2} - V_{T2})V_{DS2} - \frac{1}{2}V_{DS2}^2] \quad (2)$$

It is evident that M1 and M2 have the same drain and source voltages. Thus $V_{DS1} = V_{DS2}$ and $V_{T1} = V_{T2}$. Now, let $K_1 = K_2 = K$ and $I_{B1} = I_{B2} = I_B$. The output current I_{out} can then be written as

$$I_{out} = I_{d3} - I_{d4} = I_{d1} - I_{d2} = 2K(V_1 - V_2)(V_3 - V_4) \quad (3)$$

Therefore a four-quadrant multiplier is obtained. Note that the body (or substrate) terminals of M1 and M2 must connect to V_{SS} to allow bi-directional currents. Hence, they need not be fabricated in individual wells, which results in a saving of chip area. Conceptually, the core structure of this multiplier is very similar to the transconductor proposed in [5]. However, the currents of M1 and M2 in [5] are forced to be unidirectional, although currents in MOS transistors can flow bi-directionally. By contrast, this new CMOS triode multiplier, inspired by [3, 5, 6], expands the concept of [5] into a four-quadrant multiplier by applying the bi-directional property of MOS transistors. Accordingly, most of the features of [5] are preserved in this multiplier, such as the reduced effects of V_T mismatch and substrate noise, the suitability for low supply voltage operation, and the very large bandwidth. While preparing this Letter, a low voltage CMOS four-quadrant multiplier that also uses an analogous structure to Liu [8] was found. However, note that the circuit of Liu has a problem of unequal voltage-shifting in its unity-gain buffers due to the unavoidable V_T mismatch effect when all *n*MOS devices share the same bulk (connected to V_{SS}). Fortunately, this limitation is greatly reduced in our circuit, owing to the RGC structures. To guarantee triode operation of transistors M1 and M2, the following constraints should be satisfied:

$$\max(V_3, V_4) < \min(V_1, V_2) - V_T \quad (4)$$

where V_T is the bulk dependent threshold voltage of M1 and M2.

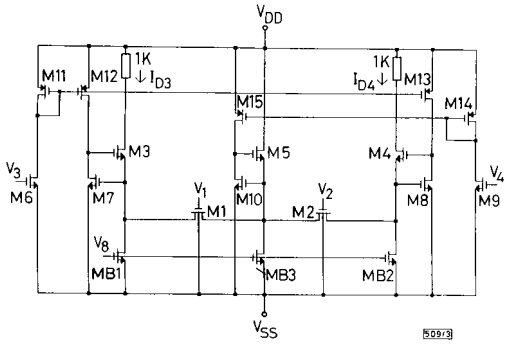

Fig. 3 *CMOS implementation of proposed four-quadrant multiplier*

Circuit implementation and simulation results: The complete circuit diagram of the proposed multiplier is shown in Fig. 3, where M9 – M18 form the three differential amplifiers in Fig. 2 according to [3] and the output current I_{out} is converted to an output voltage V_{out} through the connection of two 1kΩ load resistors. This circuit has been simulated using PSpice with a level II model of a standard 2μm CMOS process. The width-to-length ratios of all transistors used in the simulation are listed in Table 1. All simulations were performed with supply voltages of ±3V V_B = 0V, and with all *n*MOS transistors sharing the same bulk, connected to V_{SS}. Fig. 4 shows the DC transfer curves for this multiplier. Similar curves were obtained by interchanging V_1-V_2 and V_3-V_4. This circuit has < 1% nonlinearity error over a ±1.8V differential input range. For a 10kHz differential input signal having a 1.8V peak amplitude applied to V_1 and V_2 (common mode level set to 2.1V), with V_3-V_4 held constant at 1.8V, the output voltage had a THD of 0.064%. When the same signal was applied to V_3 and V_4 (common mode level set to –1.3V), the output voltage had a THD of 0.60%. The simulated –3dB bandwidth was about 17MHz. Note that the input range of V_3 and V_4 in Fig. 3 is limited to $V_{TO} < \min(V_3, V_4)$ and $\max(V_3, V_4) < \min(V_1, V_2) - V_T$ for proper operation, where V_{TO} is the threshold voltage of M6 (M9) and V_T is the threshold voltage of M1 (M2). However, at the expense of additional power dissipation and circuit complexity, this limitation can be relaxed by inserting level shifiers, as adopted in [5, 6], to reduce the lower limit on the input range of V_3 and V_4.

Table 1: Width-to-length ratios of transistors in Fig. 3 used for simulations

Transistors	M1–M2	M3–M5	M6–M10	M11–M15	MB1–MB3
W[μm]/L[μm]	10/50	100/5	10/10	50/5	10/10

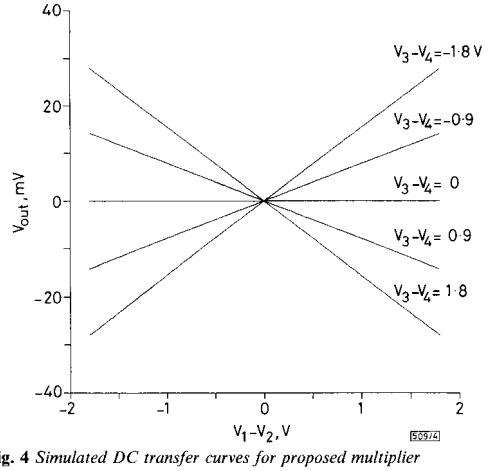

Fig. 4 *Simulated DC transfer curves for proposed multiplier*

Conclusions: Based on the very popular RGC circuits and the inherent bi-directional property of MOS transistors, a new CMOS four-quadrant multiplier is introduced. This multiplier, using only two MOS transistors, operated in the triode region with RGC structures to realise four-quadrant multiplication. Simulation results have been given to demonstrate its feasibility. This multiplier has a simple configuration and is expected to be suitable for low voltage applications.

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Two-stage neural network scheme for postfabrication circuit tuning

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Indexing terms: Integrated circuits, Tuning

A two-stage system of simple identical neural networks for postfabrication tuning of electronic circuits is proposed. The first stage selects the tuning parameters and the second stage estimates the corresponding tuning level of each tuning parameter. Convergence and accuracy are shown to be superior to those of a single stage of similar complexity.

Introduction: In electronic circuit manufacturing, postfabrication tuning is often required to bring the circuit performance up to specification. Tuning can be considered as a repair process whereby one or more of the circuit parameter values is altered to improve circuit performance. A repair operator, judging from the display of the performances, has to answer two questions: which parameters should be tuned, and how much tuning is required for each. The tuning process is highly empirical and depends on the experience of the operator. The employment of expert systems and machine learning has been proposed [1, 2]. In this Letter, a neural network based computer-aided method of tuning circuits is proposed that aims to minimise dependency on the human judgment. This approach will be particularly valuable when multiple tuning parameters are involved. Experimental results show that a single-stage backpropagation neural network suffers a long convergence period but does not produce an acceptable proportion of correct output classifications. Therefore, a two-stage network is proposed. The input to the neural networks includes a set of performance measurements such as frequency responses. The outputs from the respective neural networks are the selection of tuning parameters