# Low Jitter Butterworth Delay-Locked Loops

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**Abstract**

The low jitter Butterworth delay-locked loops (DLLs) are presented in this paper. The proposed Butterworth DLLs can suppress both the jitters generated by the input noise and the voltage-controlled delay line (VCDL) noise without stability considerations. Theoretically, the proposed Butterworth 2nd-order DLL and 3rd-order one could reduce the rms jitter due to the VCDL by a factor of $\sqrt{2}$ and 2, respectively. In addition, a technique called dynamic bandwidth-adjusting scheme (DBAS) is adopted to shorten the lock time without compromising the jitter performance. The conventional DLL and the proposed ones are simultaneously fabricated at the same die in a CMOS 0.35-um one-poly four-metal process. Compared with the conventional DLL, the measured rms jitters of the proposed DLLs can be improved by a factor of 1.40 and 1.95, respectively, with an input frequency of 125MHz. The maximum power consumption of the proposed DLLs is 32mW.

## I. Introduction

Modern CMOS techniques can not only integrate many digital circuits into a system, but also raise the operating clock frequency of the digital systems. However, the higher operating clock will decrease the timing margin for high-performance digital systems. As the timing margin is tight, the timing skews and jitters would make it difficult to synchronize among IC modules. For a conventional DLL, its loop behavior can be usually characterized by a 1st-order lowpass transfer function. The input jitter can be attenuated by 20dB/decade outside the loop bandwidth. Thus, one can narrow the loop bandwidth of a conventional DLL to decrease the influence of the input jitter [1]. However, to narrow the loop bandwidth can not reduce the jitter caused by the VCDL in the conventional DLL [1]. The proposed Butterworth DLLs could suppress the jitters due to both input noise and the VCDL noise without stability considerations.

## II. The proposed Butterworth DLLs

Fig. 1 shows the architecture of the proposed 2nd-order Butterworth DLL. A VCDL, which is the same one in the conventional DLL, is divided into two equal parts, i.e., VCDL1 and VCDL2 in Fig. 1. The first loop of Fig. 1 is similar to that in conventional DLL, but the generated voltage controlled half the VCDL, i.e., VCDL1. The middle signal, *CLKmid*, is inverted to compare with the output of the VCDL2. The transmission gate is used to match the delay of the inverter in Fig. 1. The generated voltage controlled half the VCDL, i.e., VCDL2. It results in the 2nd loop. The linear model of the proposed 2nd-order Butterworth DLL can be shown in Fig. 2. The transfer function can be expressed as

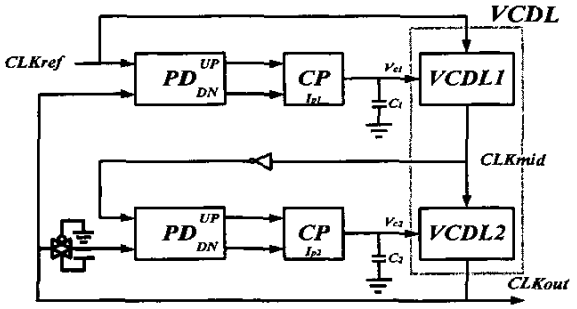



Fig. 1 The proposed 2nd-order Butterworth DLL

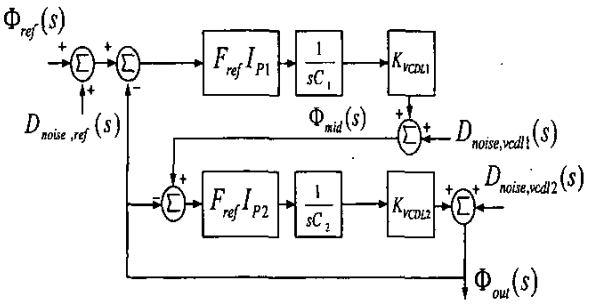



Fig. 2 Linear model of the proposed 2nd-order Butterworth DLL

$$\frac{\Phi_{out}(s)}{\Phi_{ref}(s)} = \frac{W_{N_2} W_{N_1}}{s^2 + W_{N_2} s + W_{N_2} W_{N_1}} \quad (1)$$

,where $W_{N_i} = F_{ref} I_{pi} K_{vcdli} \frac{1}{C_i}$ for $i$=1,2. $W_{N_1}$ and $W_{N_2}$ are the loop gains of the first loop and the 2nd loop, respectively. Assume the charge pump currents and the gains of two VCDLs in Fig. 1 are matched, the quality factor $Q$ can be given as

$$Q = \frac{w_c}{W_{N_2}} = \sqrt{\frac{W_{N_1}}{W_{N_2}}} = \sqrt{\frac{C_2}{C_1}}, \quad (2)$$

,where $w_c$ is the corner frequency and ${w_c}^2 = W_{N_2} W_{N_1}$. The quality factor must be $\frac{1}{\sqrt{2}}$ to meet the 2nd-order Butterworth characteristic, which can achieve the maximally flat magnitude response in the passband. To have the same corner frequency as the conventional DLL, the relation of the capacitors used in Fig. 1 should be

$$C_1 = 2 \cdot C_2 = \frac{C}{\sqrt{2}} \quad (3)$$

,where C is the capacitor used in the conventional DLL.

Based on the similar procedures, the 3rd-order

Butterworth DLL could be also shown in Fig. 3. The 3rd-order Butterworth DLL consists of four loops. The VCDL, which is the same one in the conventional DLL, can be divided into 4 equal delay sections. The first phase detector is used to compare the phase between *CLKref* and *CLKout* as the conventional DLLs did. The second phase detector is used to detect the phase error between *CLK1* and *CLK3*, while the third phase detector is used to detect the phase error between *CLK2* and *CLKout*. Fig. 4 is the linear model of the proposed 3rd-order Butterworth DLL. The transfer function of the 3rd-order Butterworth DLL can be derived as

$$\frac{\Phi_{out}(s)}{\Phi_{ref}(s)} = \frac{W_{N_1}W_{N_2}W_{N_4}}{s^3 + W_{N_4}s^2 + (W_{N_2}\cdot W_{N_3})s + W_{N_1}W_{N_2}W_{N_4}} \quad (4)$$

,where $W_{N_i} = F_{ref}I_{pi}K_{vcdli}\frac{1}{C_i}$ for $i$=1-4. Assume the gain of the third loop and the fourth one are the same, i.e. $W_{N_3} = W_{N_4}$ . To meet the 3rd-order Butterworth polynomial, $s^3 + 2w_c s^2 + 2w_c^2 s + w_c^3$, the coefficients of the denominator in eqn. (4) should be

$$W_{N_1} : W_{N_2} : W_{N_3} : W_{N_4} : w_c = \frac{1}{2} : 1 : 2 : 2 : 1 \quad (5)$$

To have the same corner frequency as the conventional DLL, the capacitors' relation could be expressed as

$$C_1 : C_2 : C_3 : C_4 : C = \frac{1}{2} : \frac{1}{4} : \frac{1}{8} : \frac{1}{8} : 1 \quad (6)$$

,where C is the capacitor used in the conventional DLL. The parameters of the proposed DLLs are listed in Table I.

Unlike to use a higher-order loop filter to achieve a higher-order system, the proposed Butterworth DLLs do not have the stability considerations. Since the loop behavior of the proposed DLLs is the same as the higher-order Butterworth lowpass filter, the loop is stable. In addition, using a higher-order loop filter can only suppress the jitter caused by the input nose. However, the proposed Butterworth DLLs can reduce both the jitters generated by the input noise and the VCDL noise.

### III. Jitter analysis of the proposed Butterworth DLLs

Assume that the input noise, $D_{noise,ref}(t)$, is a stationary Gaussian band-limited noise with a null mean value and a uniform spectral density $N_{0,ref}/A_{ref}^2$ ($f^2$/Hz) in the frequency band (-B/2, +B/2). The output jitter, $D_{out,ref}(t)$, due to input noise is thus a stationary Gaussian noise with a null mean value and a power spectral density $S_{Dout,ref}(f)$ ($f^2$/Hz) from –B/2 to +B/2.. The standard deviation due to input noise can be derived as,

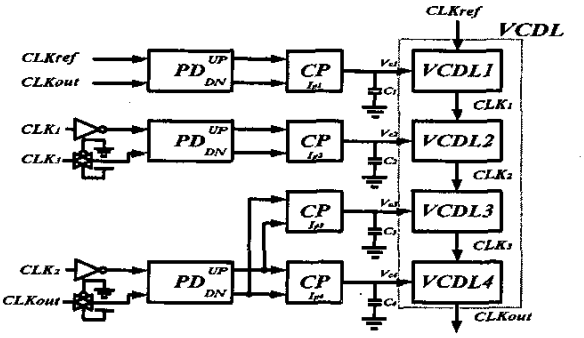



Fig. 3 The proposed 3rd –order Butterworth DLL

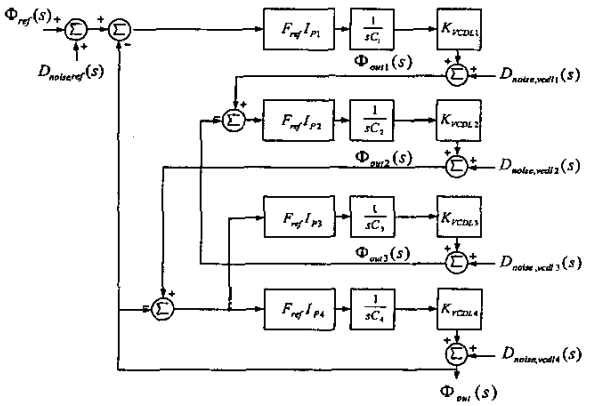


Fig. 4 Linear model of the proposed 3rd-order Butterworth DLL

Table I Design parameters of the proposed DLLs

| | | | |
|---|---|---|---|
| Frequency | | 125MHz | |
| Charge Pump Current | | 120uA | |
| VCDL gain | | 4.5ns/1.8V | |
| Filter Capacitor | 1st -order | C = 20pF | |
| | 2nd -order | $C_1$ = 14.14pF | $C_2$= 7.07pF |
| | 3rd -order | $C_1$= 10pF | $C_2$= 5pF |
| | | $C_3$= 2.5pF | $C_4$= 2.5pF |

$$D_{out,ref,rms}^2 = \frac{N_{0,ref}}{A_{ref}^2}\int_{-B/2}^{+B/2}\left|H_{ref}(j\cdot f)\right|^2 df \quad (7)$$

,where $H_{ref}(j\cdot f)$ is the input noise transfer function. Similarly, the standard deviation due to the VCDL noise can also be derived as

$$D_{out,vcdl,rms}^2 = \frac{N_{0,vcdl}}{A_{vcdl}^2}\int_{-B/2}^{+B/2}\left|H_{vcdl}(j\cdot f)\right|^2 df \quad (8)$$

, where $N_{0,vcdl}/A_{vcdf}^2$ ($f^2$/Hz) is the spectral density of VCDL noise and $H_{vcdl}(j\cdot f)$ is the VCDL noise transfer function, respectively. Thus, the total output noise can be expressed as

$$D_{out,total,rms}^2 = D_{out,ref,rms}^2 + D_{out,vcdl,rms}^2 \quad (9)$$

Assume $\frac{N_{0,vcdl}}{A_{vcdl}^2}\int_{-B/2}^{B/2} 1df = N_{vcdl} \cdot B$ and the interested noise bandwidth is much larger than the corner frequency of the noise transfer function, i.e. $B >> f_c$, the total output noise of the conventional DLL can be given as

$$D_{out,total,rms}^2 \approx \frac{N_{0,ref}}{A_{ref}^2}\pi \cdot f_c + N_{vcdl} \cdot B \quad (10)$$

,where $f_c$ is the corner frequency. The first term is proportional to the loop bandwidth of the DLL. The second term is independent of the loop bandwidth. The results are the same as that analyzed in [1].

Since the output noise contributed by each VCDL in the 2nd Butterworth DLL is identical and half of that of conventional DLL, i.e. $N_{vcdl1} = N_{vcdl2} = \frac{1}{2}N_{vcdl}$, the total output noise of the 2nd-order Butterworth DLL can be given as

$$D_{out,total,rms}^2 \approx \frac{N_{0,ref}}{A_{ref}^2}\frac{\pi \cdot f_c}{\sqrt{2}} + N_{vcdl2} \cdot B \approx \frac{N_{0,ref}}{A_{ref}^2}\frac{\pi \cdot f_c}{\sqrt{2}} + \frac{1}{2}N_{vcdl} \cdot B \quad (11)$$

Similarly, the output noise contributed by every VCDL in the 3rd-order Butterworth DLL is identical and it is equal to one-fourth of the VCDL in the conventional DLL, i.e. $N_{vcdl1} = N_{vcdl2} = N_{vcdl3} = N_{vcdl4} = \frac{1}{4}N_{vcdl}$. The total output noise of the 3rd Butterworth DLL can be given as

$$D_{out,total,rms}^2 \approx \frac{N_{0,ref}}{A_{ref}^2}\frac{2\pi \cdot f_c}{3} + N_{vcdl4} \cdot B \approx \frac{N_{0,ref}}{A_{ref}^2}\frac{2\pi \cdot f_c}{3} + \frac{1}{4}N_{vcdl} \cdot B \quad (12)$$

From eqns.(10)~(12), given the same corner frequency, $f_c$, the proposed Butterworth 2nd-order DLL and 3rd-order one can improve the jitter performance due to input noise by a factor of $\sqrt[4]{2}$ and $\sqrt{1.5}$, respectively, and improve the jitter preformance due to VCDL noise by a factor of $\sqrt{2}$ and 2, respectively.

## IV. Circuit description

In order to compare the performances of the conventional DLL and the proposed DLLs, the building blocks, such as the VCDL, the phase detector, and the charge pump circuit, are identical and their relative layout positions are also the same. They are described as follows:

### A. Voltage-controlled Delay Cell

The schematic of the delay cell used in this work is depicted in Fig. 5. It is composed of two identical inverters loaded with PMOS voltage-controlled varactors which can be immune from the substrate noise in a N-well process. The duty cycle distortion will become worse when many delay cells are cascaded to realize a VCDL with a relatively large delay time. From this point of view, the analog delay cell in Fig. 5 possesses a highly symmetrical property. For example, rising clock edge encounters a falling transition followed by a rising transition while passing the delay cell. On the other hand, a falling clock edge encounters a rising transition followed by a falling transition while passing the delay cell. Both of them are delayed by the amount of one rising-edge delay time plus one falling-edge delay time except that the sequence is different. Therefore, they are almost delayed by the same delay time. This helps to preserve the clock duty cycle when a VCDL with a relatively large delay time is used.

### B. Charge Pump

The charge pump circuit is shown in Fig. 6. A technique called dynamic bandwidth-adjusting scheme (DBAS) is adopted here to shorten the lock time without compromising the jitter performance. The reference current, $I_{CP}$, has two current sources, one is normally turned on, and the other is controlled by a lock detector (*LD*). When the loop is unlocked, LD is low and makes the bias current almost.

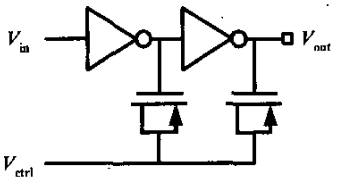



Fig. 5 The schematic of the delay cell

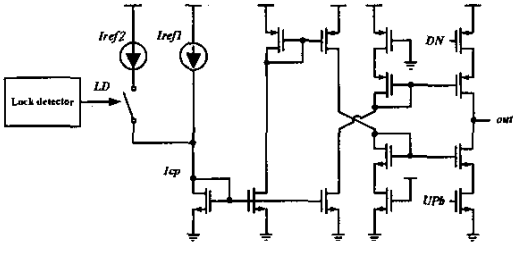



Fig. 6 The charge pump circuit

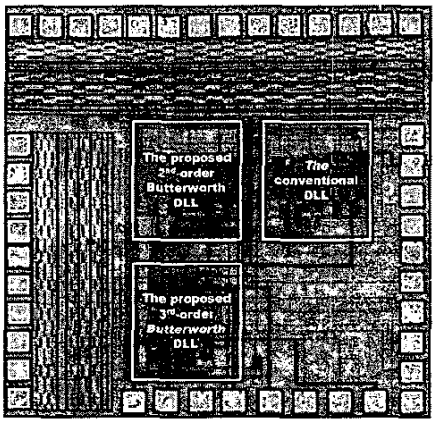
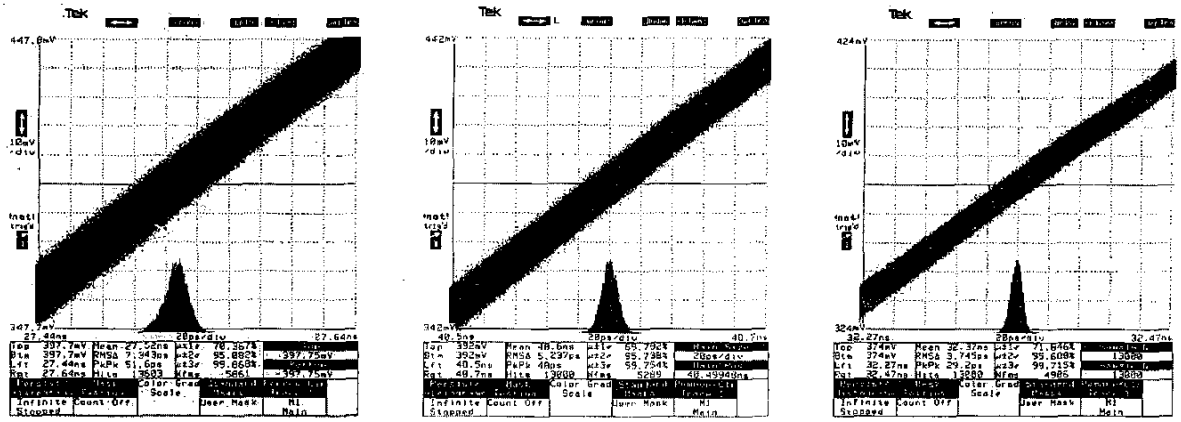



Fig. 7 Microphotograph of the chip



(a) The conventional DLL (b) The proposed 2nd-order Butterworth DLL (c) The proposed 3rd-order Butterworth DLL

Fig. 8 Jitter histograms @125MHz

doubled and it will widen the loop bandwidth to shorten the lock time. When the phase error is smaller than the lock window defined by the lock detector [2], LD goes High and narrow the loop bandwidth to improve the jitter performance.

C. Phase detector

In this work, the dynamic logic style PFD [3] is adopted to overcome the speed limitation and reduce the dead zone.

## V. Experimental results

Three DLLs have been fabricated at the same die in a 0.35um CMOS process as shown in Fig. 7 and the whole chip area is $1.44 \times 1.47\ mm^2$ including I/O pads. Assume the gain of the third loop and the fourth one are the same in the 3rd-order Butterworth DLL, the contol voltage of the third loop can be substituted by that of the fourth loop. Hence, the charge pump circuit and loop filter of the third loop can be omitted in Fig.3. Fig. 8 gives the measured jitter histograms. The measured peak-to-peak jitter of the conventional, the 2nd-order, and the 3rd-order DLLs is 51.6ps, 40.0ps and 29.2ps, respectively, with the input frequency of 125MHz. The measured rms jitter of the conventional, the 2nd-order, and the 3rd-order DLLs is 7.34ps, 5.24ps and 3.75ps, respectively. Compared with the conventional DLL, the measured rms jitters of the proposed DLLs can be improved by a factor of 1.40 and 1.95. If the most part of the output noise is mainly contributed by the VCDL and the input noise can be filtered by narrowing the loop bandwidth, the measured results are close to the analysis discussed above. The performance summary is listed in Table II.

## VI. Conclusion

In this paper, the proposed Butterworth DLLs can improve the jitters without stability considerations. Compared to the conventional DLL, the proposed Butterworth 2nd-order DLL and the 3rd-order one could reduce the noise due to VCDL by a factor of $\sqrt{2}$ and 2, repectively. In addition, the dynamic bandwidth adjusting scheme is also introduced in the proposed DLLs to achieve the shorter lock time without compromising with the jitter performance. The measured results also demonstrate the functionality of the proposed DLLs.


## Acknowledgement

The authors would like to thank National Chip Implementation Center, Taiwan, for chip implementation.


Table II Performance summary of the proposed DLLs

| | |
|---|---|
| Process | 0.35-um 1P4M CMOS process |
| Supply Voltage | 3.0~3.6V |
| Frequency Range | 100~140MHz |
| Power Consumption | 32mW @ 125MHz, 3.3V |
| PkPk jitter | 51.6ps @ 1st order, 125MHz |
| | 40.0ps @ 2nd order, 125MHz |
| | 29.2ps @ 3rd order, 125MHz |
| r.m.s. jitter | 7.34ps @ 1st order, 125MHz |
| | 5.24ps @ 2nd order, 125MHz |
| | 3.75ps @ 3rd order, 125MHz |
| Chip Area | $1.44 \times 1.47\ mm^2$ @ with I/O pads |

## References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[3] S. Kim, K. Lee, Y. Moon, D. K. Jeong, Y. Choi and H. K. Lim, "A 960-Mb/s/pin interface for skew-tolerant bus using low jitter PLL," *IEEE J. Solid-State Circuits*, vol. 32, no. 5, pp. 691-700, May 1997.