All Digital CDMA Upstream Transmitter and Baseband VLSI Design of Head-End Receiver for Upstream Cable Networks

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ABSTRACT

This paper presents an all digital DS-CDMA upstream transmitter and a head-end baseband receiver for upstream cable/HFC networks. The upstream transmitter supports frequency agility of the carrier, QPSK and QAM constellations up to 64QAM, variable symbol rates from 160kchip/s to 5.12Mchip/s increasing by power of two, and direct-digital up-conversion to achieve accurate amplitude and phase of modulation. The transmitter consists of pulse shaping filter, half-band filter, cascaded integrator-comb (CIC) filter, and inverse SINC filter. The all digital head-end baseband receiver supports programmable quadrature amplitude modulation up to 64QAM. Fast timing and carrier recovery algorithms are adopted for burst mode transmission. Code acquisition can be achieved within 2 symbols, and the carrier acquisition can be achieved within 31 symbols. All digital timing recovery is designed with ±200ppm symbol timing offset tolerance and the carrier recovery can compensate ±100ppm of carrier frequency offset.

1. INTRODUCTION

The cable television (CATV) industry is now geared toward providing two-way interactive communications over cable network. The broadband hybrid fiber coax (HFC) access network, evolved from the coaxial cable distribution network, is an emerging cable architecture for providing high speed residential video, voice telephony, data and other interactive services to subscribers. Broadcasting downstream to the subscribers is straightforward since CATV systems were originally designed for high fidelity downstream transmission. The channel is relatively good, and bandwidth is abundant.

On the other hand, upstream channel transmission is much more challenging. The band from 5 to 42 MHz used by upstream transmission is corrupted by large narrowband interference [2]. The presence of impulse noise, burst noise, narrow band interference, and micro-reflection in upstream cable networks calls for robust multi-access scheme that ensures reliable communication in the upstream channel services. Synchronous code-division-multiple-access (SCDMA), adopted in the DOCSIS 2.0, is robust to narrowband noise and offers a more efficient utilization of the upstream band than TDMA or FDMA [4].

An all digital CDMA upstream transmitter and a head-end receiver are presented in this paper. It is organized as follows. The transmitter architecture is shown in the next section. In Section 3, the fast timing and carrier recovery algorithms for burst mode transmission and head-end receiver architecture are described. The simulation results and system performance are demonstrated in Section 4. Finally, the conclusion is given in Section 5.

2. UPSTREAM TRANSMITTER

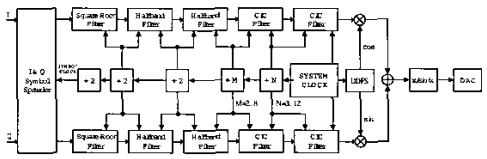

Figure 1: Block diagram of a frequency-agile transmitter

The block diagram of a frequency-agile transmitter is shown in Fig.1. The modulator consists of serial to symbol spreader, Nyquist pulse shaping filters, half-band filter, CIC filter, the quadrature mixer, and inverse SINC filter. This transmitter is compliant with DOCSIS2.0 and incorporates several features. First, it adopts an all-digital modulation architecture that has the advantages of more accurate phase and amplitude waveform than the traditional analog implementation does. Second, the architecture also implements the mixer in digital domain which can achieve frequency agility and perfect amplitude and phase matching characteristics.

A digital interpolation scheme is required to achieve the sampling rate conversion. The interpolation filters are implemented by one square-root filter, two half-band FIR filters, and CIC filters. The half-band FIR filters are hardware-efficient because half of the filter coefficients are zero. These two half-band filters, both of which have linear phase re-

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sponse, provide a factor of four times the sampling rate. The CIC filters are also hardware-efficient because they do not need any multiplier. Thus, it is suitable for high-sampling-rate conversion. The conversion rate of a CIC filter is limited to an integer value only, which doesn't affect the design of the interpolator. Its frequency response is given by:

$$H(z) = H_I^N(z) \cdot H_C^N(z) = \frac{(1 - z^{-RM})^N}{(1 - z^{-1})^N} = \left[\sum_{k=0}^{RM-1} z^{-k} \right]^N \quad (1)$$

where $H_I(z)$ and $H_C(z)$ are the transfer functions of the integration and comb parts of the CIC filter, N is the number of cascading stage, R is the interpolation rate, M is the number of delay elements in the comb and the integrator.

3. HEAD-END RECEIVER

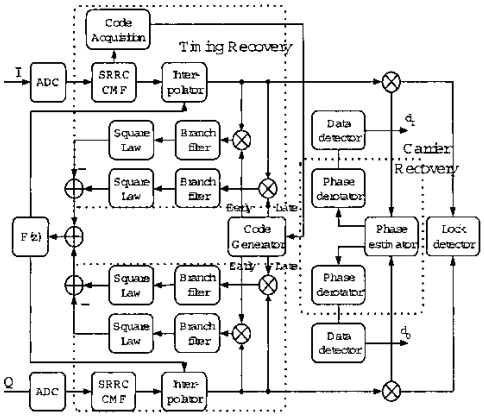

Figure 2: Receiver block diagram

The block diagram of the proposed all digital baseband receiver is show in Fig.2. It consists of a pulse-shaping filter, a timing recovery block, and a carrier recovery block. The ADC operates at constant clock because the head-end receiver works in a multi-user environment. Therefore, a interpolator-based digital timing recovery is designed in the head-end receiver to cope with timing offset. The recovered signals are obtained from the asynchronous samples solely by the digital timing recovery block. A match filter is also designed for fast code acquisition. Furthermore, the burst mode transmission necessitates fast timing and carrier recovery circuits to detect and relieve the carrier phase and frequency offset. The following illustrates these blocks in detail.

3.1 Timing recovery

The timing recovery blocks are separated into two parts, namely the code acquisition and the code tracking function. Fig.3 shows the block diagram for code acquisition. A matched filter is implemented for fast code acquisition by correlating the spreading code. The acquisition time, T_s, of a matched filter is $T_s = \frac{2M+1}{2} T_i \approx MT_i$, where M is the length of the spreading code used, T_i is the chip duration. T_s is within two symbols in our design. Calculating the square root, $\sqrt{I^2 + Q^2}$, in the matched filter is not easy

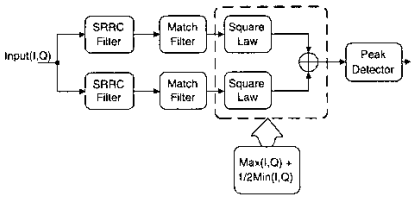

Figure 3: Code acquisition block diagram

to implement for code acquisition. Instead, an approximation method is used by calculating $\max(I, Q) + \frac{1}{2}\min(I, Q)$, which is more hardware efficient. The approximation error is shown in Fig.4 where the largest relative error is less than 12 percents, which acceptable in this design.

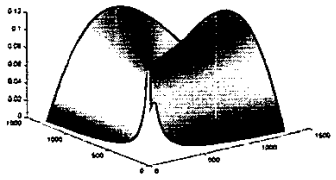

Figure 4: Square-root approximation error

After code acquisition, the residual timing error caused by clock frequency and phase mismatches is corrected by the code tracking loop. The block diagram is shown in Fig.5. The code tracking loop consists of interpolation filter, delay lock loop, and loop filter. These blocks are further illustrated in the following

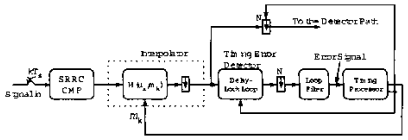

Figure 5: All digital timing recovery loop

3.1.1 *Interpolation filter*

A polynomial interpolation filter is employed to interpolate the values of the oversampled signal. The interpolation filter structure used in the transmitter design, such as CIC filter and half-band filter, is insufficient for the code tracking loop. This loop requires continuous interpolation ratios, including irrational numbers which are available in the polynomial interpolation filter. The coefficients are obtained by minimizing the quadratic error:

$$\int_0^1 \int_{-2\pi B}^{2\pi B} \left| e^{j\omega T_s \mu} - \sum_{n=-N}^{N-1} \left[\sum_{m=0}^{M} c_m(n) \mu^m \right] e^{-jn\omega T_s} \right|^2 d\omega d\mu \quad (2)$$

where B ,N, and M are the bandwidth, the tap number, and order of the interpolation filter respectively, μ is the tuning variable, and $c(m)$ are the coefficients of the filter.

The functional block diagram of Farrow's structure [3] of polynomial interpolator is shown in Fig.6. The polynomial

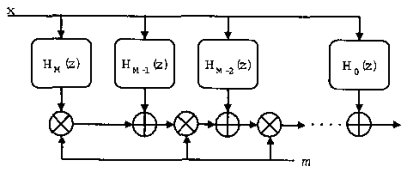

Figure 6: Farrow's structure for polynomial interpolator

interpolator can be realized as a bank of M parallel FIR filters where the output of the m-th branch is first multiplied by μ^m and then summed up. This structure is suitable for high-speed realization. The transfer function is

$$H(z,\mu) = \sum_{m=0}^{M} \mu^m \left[\sum_{n=-N}^{N-1} c_m(n) z^{-n} \right] \qquad (3)$$

The (M+1) FIR filters with fixed coefficients can be implemented efficiently in VLSI design. Only one value of μ must be distributed to the M multipliers that can be pipelined. In this design, N and M are chosen as 2 and 3 respectively to achieved required performance. The amplitude error in the passband is less than -40dB. Simulation result is shown in Fig.7.

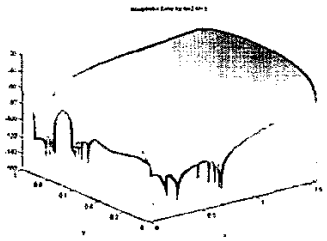

Figure 7: Simulation result of interpolator for N=2 M=3

3.1.2 Delay lock loop (DLL)

Coherent DLL is not suitable here because of two reasons. First, the carrier phase error must be recovered prior to code tracking. Since the system operates in the multi-user condition, the demodulation is difficult. Secondly, the input carrier is modulated by data, which implies that the data decision must be accomplished before the code tracking process. In contrast, neither of these factors is present in the non-coherent DLL.

The non-coherent DLL block diagram in this design is shown in Fig.8. It contains two energy detectors that are not sensitive to data modulation or carrier phase. In the DLL phase discriminator the signals in the I and Q branches are multiplied with $c\left(k+\frac{\Delta}{2}T_c\right)$ and $c\left(k-\frac{\Delta}{2}T_c\right)$ that are the early and late patterns of the estimated spreading code respectively. The error signal is derived by the correlation of signals from I and Q branches with the early pattern minus

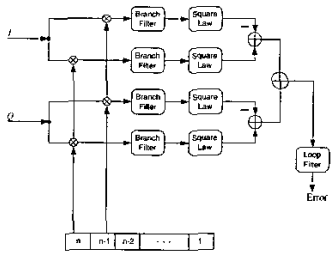

Figure 8: Non-coherent DLL block diagram

that with the late pattern, which can be described by

$$\begin{aligned} c(i,\delta) &= I_{e,i}^2 + Q_{e,i}^2 - I_{l,i}^2 - Q_{l,i}^2 \\ &= A^2N^2\left[R_c^2\left(\delta+\frac{\Delta}{2}\right) - R_c^2\left(\delta-\frac{\Delta}{2}\right)\right] \text{[5] (4)} \end{aligned}$$

In (4), $R_c(\cdot)$ is the correlation function and Δ is the time shift of the early and late patterns. Δ affects the gain and the lock-in range of the DLL. Δ is chosen as 1.0 for maximum DLL gain.

A hardware efficient algorithm is also adopted to improve the power consumption [6]. The error signal of the non-coherent DLL discriminator can be rewritten as

$$\begin{aligned} e &= I_{e,i}^2 + Q_{e,i}^2 - I_{l,i}^2 - Q_{l,i}^2 \\ &= (I_{e,i} - I_{l,i})(I_{e,i} + I_{l,i}) + (Q_{e,i} - Q_{l,i})(Q_{e,i} + Q_{l,i}) \\ &= I_{\Delta,i}I_{\Sigma,i} + Q_{\Delta,i}Q_{\Sigma,i} \qquad (5) \end{aligned}$$

The block diagram of this improved non-coherent DLL loop is shown in Fig.9. The power consumption of this structure will be reduced to about a half comparing to that of the conventional one and this simplification does not cause any degradation.

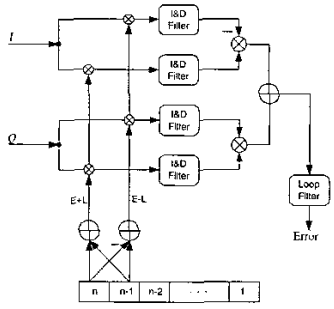

Figure 9: Improved non-coherent DLL block diagram

Moreover, A first order branch filter with bandwidth B_b is chosen whose transfer function is

$$H_b(z) = \frac{1-a}{1-az^{-1}} \quad , \quad a = exp(-2\pi B_b T_c) \qquad (6)$$

The filter bandwidth, B_b, is chosen to be about three times the symbol rate. The loop filter is also a first order filter similar to the branch filter. The performance influence of the branch filter is derived in many papers[6].

3.2 Carrier recovery

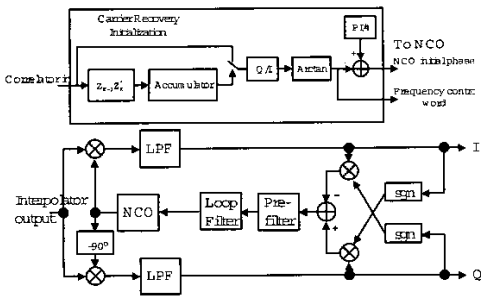

Figure 10: The carrier recovery block diagram with NCO initialization and the Costas loop

The block diagram of carrier recovery is shown in Fig.10. This loop adopts fast feed-forward data-aided digital algorithm for carrier phase and frequency offset estimation in a burst mode transmission[1]. The techniques are applicable to linear modulation (M-PSK, M-QAM) and based on oversampling of a known preamble. The estimated phase error is

$$\hat{\theta} = arctan\left[Im\left(\frac{1}{N}\sum_{n=i}^{l+N-1} z_n\right) \Big/ Re\left(\frac{1}{N}\sum_{n=l}^{l+N-1} z_n\right)\right] \quad (7)$$

whereas the estimated frequency error is

$$\hat{\Omega} = \frac{1}{L} arctan \frac{Im\left(\frac{1}{N}\sum_{n=l+L}^{l+N+L-1} z_n z_{n-L}^*\right)}{Re\left(\frac{1}{N}\sum_{n=l+L}^{l+N+L-1} z_n z_{n-L}^*\right)} \quad (8)$$

Here N is the length of the accumulation, and z is the input signal from the correlators.

The estimation range of frequency offset is restricted within π/L. N decides the range of estimation window. The performance degradation will be reduced if N is increased. L affects the range of frequency error estimation. A choice of N=31 and L=1 is made in this design, which is a compromise between acquisition time and estimation performance. After frequency and phase estimation, a modified Costas loop is implemented to track the residual carrier phase and frequency offset.

4. SIMULATION RESULTS

The simulations of the whole system are performed using C language. All filters in the upstream transmitter are designed with passband ripple smaller than 5×10^{-3}dB. The stopband attenuation of DAC output is more than 40dB. The upstream channel model contains AWGN, multi-path, impulse noise, burst noise, and ingress noise. Fig.11(a) shows the DLL output error in timing recovery when the symbol timing offset is -200ppm. Fig.11(b) shows the carrier recovery output error when the carrier frequency error is 100ppm, i.e 4kHz. Fig.12 shows the 64QAM constellation of recovered data.

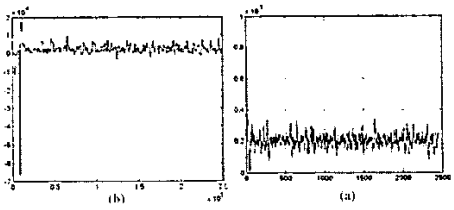

Figure 11: Output error of the timing and carrier recovery

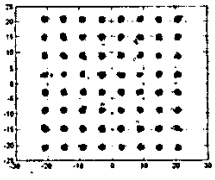

Figure 12: 64QAM constellations of recovered data

5. CONCLUSIONS

This paper presents an all digital CDMA architecture for upstream transmitter and a head-end baseband receiver in cable/HFC networks. The transmitter is featured by frequency agility of the carrier, QAM modulation variable symbol rates, and direct-digital up-conversion. The head-end baseband receiver is designed with 64QAM demodulation, fast timing and carrier recovery circuits for burst mode transmission. The timing recovery block can tolerate ±200ppm symbol timing offset and the carrier recovery can compensate ±100ppm carrier frequency offset.

6. REFERENCES

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