A BiCMOS Image Sensor with a Chopper-Stabilized Edge Detector and a Correlated-Double-Sampling Readout Circuit for Neural Network VLSI Operating at $77K$

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Abstract

This paper presents a new image sensor with a chopper-stabilized edge detector and a correlated-double-sampling readout circuit, based on a $2\mu m$ BiCMOS technology for pattern recognition neural network VLSI applications operating at $77K$. With the chopper-stabilized edge detector and the correlated-double-sampling readout technique, the two-dimensional photodiode array, which can be efficiently built with only one readout circuit, provides a bidirectional edge detection capability for high resolution image sensing applications operating at $77K$.

Summary

Recently, pattern recognition implemented by the neural network techniques has been the major method for machine vision applications. Usually, the image of the object is recorded by a 2D photodetector array such as charge-coupled device (CCD), followed by the edge detection of the object, then the recognition function is performed. Smart edge detectors resembling the response of a biological retina, which is made of over 30 transistors and one phototransistor as a pixel unit and can be used to extract the edge position of an object image, has been realized using CMOS analog VLSI circuit techniques [1]. A simpler "off-center" edge detector composed of two back-to-back-connected concentric or directional photodiodes realized by amorphous silicon technology has also been reported [2]. The generated edge signal, which can be either positive or negative, is proportional to the difference of the two photocurrents associated with two photodiodes if the edge of the image happens to fall on the detector. In this paper, a new image sensor using two pairs of cross-coupled BiCMOS photodiodes with chopper-stabilized switches and a correlated-double-sampling readout circuit operating at $77K$ for bidirectional edge detection, will be described.

This new image-sensor is composed of an edge detector array and a readout circuit. As shown in Fig. 1, a $2\mu m \times 2\mu m$ photodiode used in the edge detector array, which is between the base and collector regions of the BiCMOS structure, generates a zero-biased current of $20nA$ as illuminated by a tungsten light source. As shown in Fig. 1 in each pixel area, two cross-coupled pairs of back-to-back-connected photodiodes can be used to perform bidirectional edge detection. Different from traditional image sensors such as CCD, in the edge detector, each pair of photodiodes generate a nonzero net current only when an image edge falls on the detector. This arrangement facilitates an efficient recording of the edge information of an image. As for the readout circuit, there are a word-line decoder, a bit-line decoder, a current integrator/output buffer. As in SRAM memeory cells, together with the word-line and bit-line decoder outputs, 4 pass transistors utilizing chopper-stabilized techniques [3] are used to provide an access to the current integrator/output buffer for each individual pair of the photodiodes as shown in Fig. 2. In addition, the chopper-stabilized switches also facilitate bidirectional edge dectection as a result of the nonzero net current coming from the photodiode pair. Consequently, a two-dimensional edge detector array can be constructed with the basic edge detector cell, which is composed of two cross-coupled pairs of back-to-back-connected photodiodes and 8 switches. Furthermore, only one readout circuit is necessary for the whole edge detector array and the effective area in image sensing can be raised owing to the drastic reduction on the non-photodiode area. As shown in Fig. 2, the current integrator/output buffer, which is used to convert the photocurrent into an output voltage signal for further processing, is made of an op amp, an integrating capacitor, C_{int}, a reset switch SW1, and a feedback PMOS transistor to ensure a zero-biased operation for the accessed photodiodes at an optimized efficiency. Two PMOS source followers with a capacitor, C_D, and a switch SW2 are used as an output buffer with a correlated-double-sampling mechanism [4] to reduce noise effects and to facilitate recording of the nonzero net current from the photodiodes with clock timing as shown. During T1, SW3's are on and the selected photodiodes are connected to the readout circuit. As SW1 is high, the integrating capacitor, C_{int}, is grounded and the capacitor, C_D, is floating. As SW2 turns on and SW1 is off, the integrating capacitor, C_{int}, is charged by the photocurrent generated by the accessed photodiodes and the right plate of the capacitor, C_D, is grounded. At the end of the T1 period, the capacitor, C_D, contains the sampled reset noise and the charge associated with the photocurrent of the same photodiodes biased at a polarity set by SW3's. During T2, the polarity of the selected photodiodes is reversed and SW2 is always off. As SW1 turns off, the charge corresponding to the photocurrent of the same photodiodes with the polarity reversed by turning on SW4's is coupled to the capacitor, C_D. The difference in charge associated with the capacitor, C_D, between T1 and T2 shows up in the output voltage, V_{out}, at the end of the T2 period. Incorporating the modified correlated-double-sampling mechnism, the new detector

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circuit not only can detect a positive or negative photocurrent but also can reduce the thermal and flicker noise effects generated in the analog front end of the readout circuit. CMOS analog circuits operating at $77K$ offer low noise advantages [5], which are particularly important for high performance image sensing circuits [6]. Currently, SPICE device models are not sufficient for simulation of circuits operating at $77K$. In order to design the image sensor operating at $77K$, low temperature SPICE models have been successfully modified. Fig. 3 shows the IV characteristics of the NMOS and PMOS devices at $298K$ and $77K$. At $298K$, the SPICE model results match well with the measured data. However, at $77K$, the differences between the measured data and the SPICE model results are not negligible. Especially for the PMOS device, the SPICE model results are unacceptable for low temperature circuit simulation. Here, modified SPICE models at $77K$ with a much nicer fit to the measured results have been created for low temperature circuit simulation. With the appropriate low temperature models, a CMOS two-stage op amp as shown in Fig. 4 with a low noise input and a temperature-insensitive biasing scheme has been designed. As shown in Fig. 4, this low temperature op amp has a small signal dc gain of over 1000, a unity gain bandwidth of 2MHz, and a phase margin of over 60 degrees at a power dissipation of 4mW. Overall transient behavior of the image sensing circuit operating at $77K$ is shown in Fig. 5. In a pixel area, with the photodiode, D2, illuminated by a light source and the other photodiode, D1, masked, the output voltage, V_{out}, actually shows a larger value at the end of T2 as compared to that at the end of T1. On the other hand, with D2 masked and D1 illuminated, a smaller output voltage at the end of T2 can be seen. Experimental low temperature results confirm the simulation results as shown. Thus, the bidirectional edge detection capability of the new image sensing circuit using a chopper-stabilized edge detector and a correlated-double-sampling readout circuit has been verified. Fig. 6 shows the layout of the 2×2 image sensing circuit based on a $2\mu m$ BiCMOS technology. Digital bit-line and word-line decoder circuits are shown in the upper and central portions of the figure. Center right portion is the edge detector array and at lower right is the op amp related readout circuit. Total chip area is around $1400\mu m \times 1200\mu m$. In conclusion, with the chopper-stabilized edge detector and the correlated-double-sampling readout circuit, the new sensing circuit can provide a SRAM-type two-dimensional expansion capability in implementing pattern recognition VLSI for bidirectional edge detection at $77K$.

Acknowledgments

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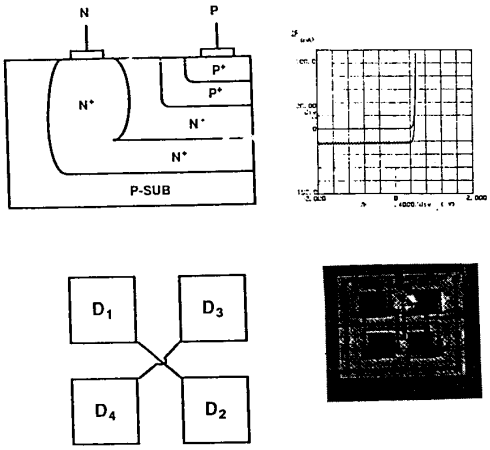

Fig. 1. (a)The photodiode structure. (b)IV characteristics of the photodiode. (c) tow cross-coupled pairs of back-to-back-connected photodiodes in each pixel area

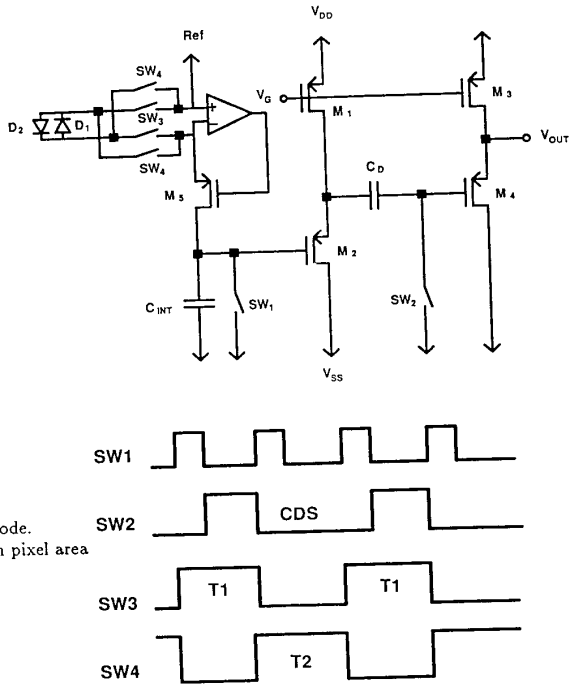

Fig. 2. The readout circuit.

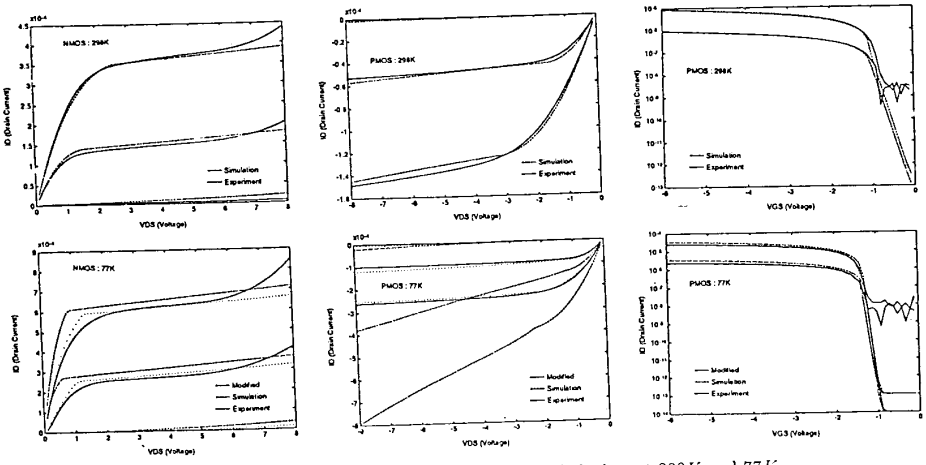

Fig. 3. IV characteristics of the NMOS and PMOS devices at $298K$ and $77K$.

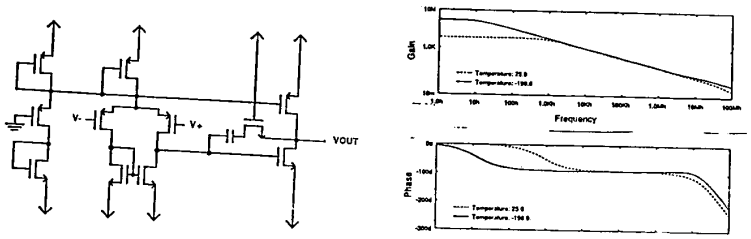

Fig. 4. The CMOS op amp operating at $77K$.

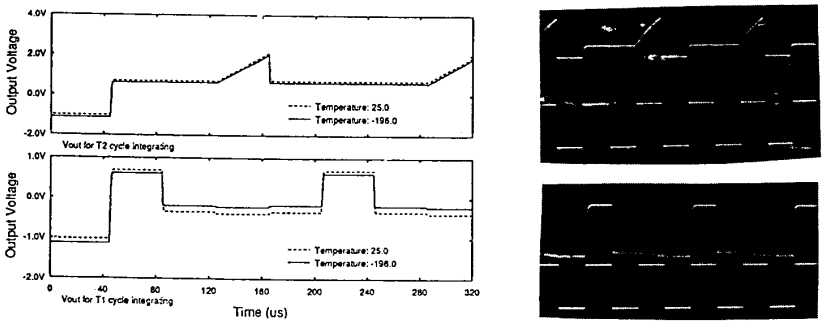

Fig. 5. Overall transient behavior of the image sensing circuit operating at $77K$.

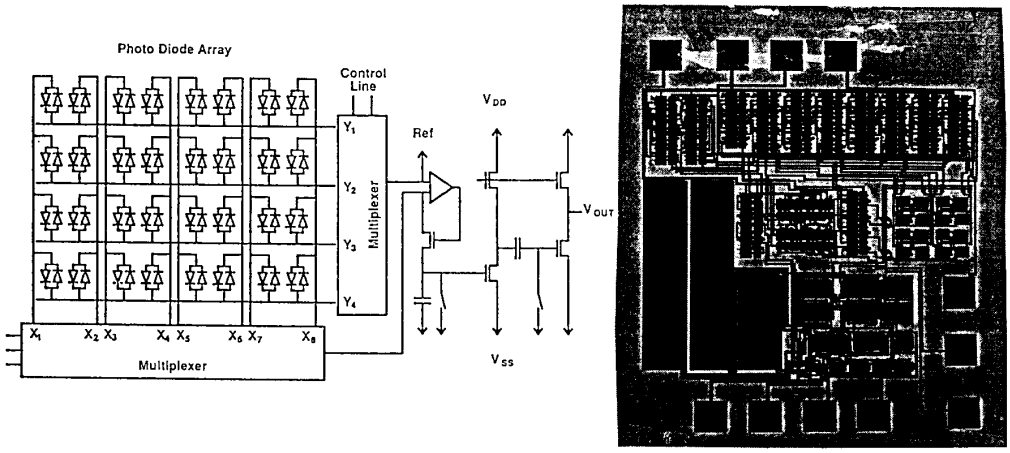

Fig. 6. Layout of the new imaging sensing circuit.