$A^2$/Hz. The calculated sensitivity, based on the integration of the noise spectrum over the operating bandwidth, was −14.5dBm at a bandwidth of 15Gbit/s and a wavelength of 1.55μm.

In conclusion, we have demonstrated a very high speed long-wavelength monolithic photoreceiver with a 3dB-down frequency of 11GHz. The epitaxial layers for the receiver were grown using single-step MOVPE. The *p*-type region of the *pin* PD was formed by Be-ion implantation. The 0.5μm gate-length HEMT showed a current gain cutoff frequency of 42GHz. This photoreceiver demonstrated an opened eye pattern for a 15Gbit/s NRZ light signal. The calculated sensitivity from the measured noise performance was −14.5dBm at the same bit rate. This was the first demonstration of a long-wavelength monolithic receiver that can receive a 15Gbit/s NRZ signal, and that is applicable for very-high-speed operation greater than 10Gbit/s.


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Y. Akahori, M. Ikeda and A. Kohzen (*NTT Opto-electronics Labs., 3-1 Morinosato Wakamiya, Atsugi-shi, Kanagawa Pref., 243-01, Japan*)

Y. Akatsu (*NTT Transmission Systems Labs. 1-2356 Take, Yokosuka-shi, Kanagawa Pref., 238-03, Japan*)

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## Closed-form physical model for VLSI bipolar devices considering energy transport

J.B. Kuo, H.J. Huang and T.C. Lu

*Indexing terms: Bipolar transistors, VLSI, Semiconductor device models*

A closed-form physical model is reported for VLSI bipolar devices considering energy transport. Based on the model, for a base width of 810Å, the bipolar device, biased at $V_{cb}$ = 2V, has a peak electron temperature of over 700K, which results in a 5% reduction in the collector current.

*Introduction:* For an advanced BiCMOS technology, the electric field in the bipolar devices can be large; the electric field affects the electron energy distribution. The electron temperature in the bipolar device may be much higher than the lattice temperature. Therefore, energy transport is important in determining the current conduction of a device [1]. For a bipolar device, the energy transport related effects based on numerical simulation have also been reported [2]. In this Letter, a closed-form physical model for bipolar devices considering energy transport is described.

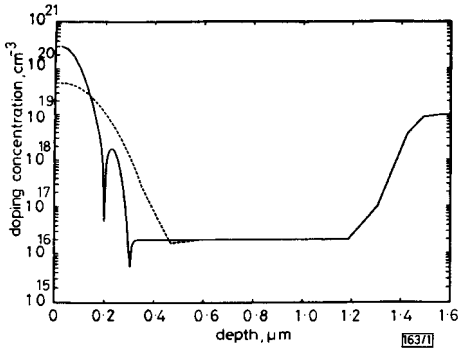


**Fig. 1** *Doping profiles of VLSI BJT device under study*

——— extrinsic doping profile
– – – – extrinsic doping profile

*Analytical model:* Consider a VLSI bipolar device [3] as shown in Fig. 1. Under a high electric field, the electron current density in the substrate direction of the bipolar device can be expressed as a function of the electron temperature $T_n$ [4] as shown in eqn. 1 in Appendix 1. For electrons in the base region, the electric field in the base region is as shown in eqn. 2. In addition to the electric field as shown in eqn. 2, the 'depletion layer tail induced' electric field is also important [5]. Considering the 'depletion layer' tail effect at the base side of the base/collector and base/emitter junctions, the total electric field in the base region is represented by eqn. 3. The electron temperature can be connected to the effective electric field through the power balance equation [2] as shown in eqn. 4. Including the velocity overshoot effect, a carrier temperature-dependent mobility model [6], and from eqn. 4 the electron temperature, is as shown in eqn. 5. For a bipolar device with a very narrow base biased in the forward active region, the electron distribution in the base region can be approximated as linear [5]. Therefore, the electron current density is given by eqn. 6. Without considering the energy transport effect, eqn. 6 is simplified to the results as derived by Kroemer [7].

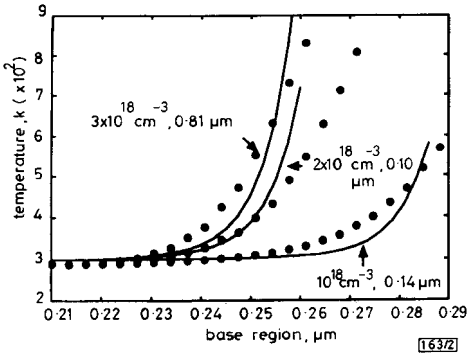


**Fig. 2** *Electron temperature distribution in substrate direction of BJT device for three base doping profiles*

Based on PISCES and analytical model results

● simulation result
——— model result

*Results:* To show the effectiveness of the closed-form analytical model considering energy transport for a VLSI bipolar device, PISCES simulation considering energy transport has been carried out. The device under study as shown in Fig. 1 has a base width of 1000Å, a peak base doping density of $2 \times 10^{18}$cm$^{-3}$, an emitter depth of 0.2μm, a peak emitter doping density of $3 \times 10^{20}$cm$^{-3}$ and a $2 \times 10^{16}$cm$^{-3}$ epi-collector region of 1.0μm. In addition to the base profile as described above, two other base profiles have also been considered: one is with a base width of 0.1414μm and a peak doping concentration of $10^{18}$cm$^{-3}$ and the other has a base width

of 0.081 μm and a peak density of $3 \times 10^{18}$cm$^{-3}$. Fig. 2 shows the electron temperature distribution in the base region of the bipolar device for three base profiles, based on the analytical model. For the three cases, the model results show a good match with the simulation results. As shown in the Figure, for a narrower base, the spread in the temperature distribution is larger. For a base width of 0.081 μm, the peak electron temperature is over 700K. For a base width of 0.1414 μm, the electron temperature distribution is rather flat.

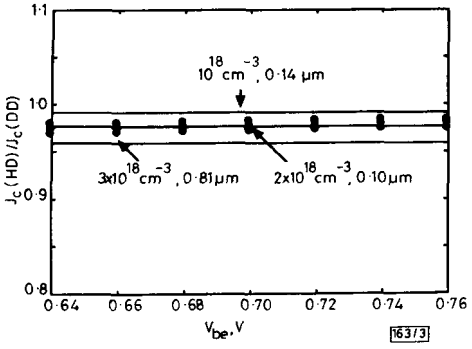


**Fig. 3** *Ratio of collector current considering energy transport to that without considering it against $V_{BE}$ of bipolar device for three doping profiles*

● simulation result
——— model result

Fig. 3 shows the ratio of the collector current density considering energy transport to that without considering it against $V_{be}$ of the bipolar device for three base doping profiles, using the closed-form analytical model and the PISCES simulation result. Generally speaking, the collector current density considering energy transport is less than that without considering it. The thermodiffusion effect in the base region can be identified as Δ, which makes the collector current smaller as compared to that without considering it. Among the three cases, the case with the narrowest base shows the smallest ratio, which is due to the highest electron temperature effect. Although the electron temperature degrades the collector current by only less than 5%, the electron temperature effect can be very important for an advanced bipolar device with very narrow base width.

*Appendix 1:*

$$J_n = q\mu_n nE + q\mu_n \frac{d\left(\frac{kT_o}{q} n\right)}{dx} \quad (1)$$

$$E = \frac{kT_o}{q}\left(\frac{1}{p}\frac{dp}{dx} - \frac{1}{n_i^2}\frac{dn_i^2}{dx}\right) \quad (2)$$

$$E_{total} = \frac{kT_o}{q}\left(\frac{1}{p}\frac{dp}{dx} - \frac{1}{n_i^2}\frac{dn_i^2}{dx}\right) + E_{tail(bc)} + E_{tail(be)} \quad (3)$$

$$nq\mu_n E_{eff}^2 = n\frac{3}{2}k\left(\frac{T_n - T_o}{\tau_n}\right) \quad (4)$$

$$T_n = T_o + \frac{2}{3}\frac{k}{q}\tau_n\left(\frac{-1+\sqrt{1+4\alpha(\mu_o E_{eff}^2)^\beta}}{2\alpha}\right)^{\frac{1}{\beta}} \quad (5)$$

$$J_n = \frac{(-1+\Delta+\delta)e^{\frac{v_{bi}}{\frac{kT_o}{q}}}}{\int_0^W \frac{p(x)}{kT_o\mu_n n_i^2(x)}dx} \quad (6)$$

$$\Delta = \int_0^W \frac{p(x)}{n_i^2(x)}\frac{n_i^2(0)}{p(0)}\frac{d\left(\left(\frac{T_n(x)}{T_o}-1\right)\left(\frac{W-x}{W}\right)\right)}{dx}dx$$

$$\delta = \int_0^W \frac{1}{\frac{kT_o}{q}}\frac{p(x)}{n_i^2(x)}\frac{n_i^2(0)}{p(0)}\left(\frac{W-x}{W}\right)(E_{tail(bc)} + E_{tail(be)})dx$$


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J. B. Kuo, H. J. Huang and T. C. Lu (*Rm. 338, Dept. of Electrical Eng., National Taiwan University Roosevelt Rd. Sec. 4, #1, Taipei, Taiwan 106-17, Republic of China*)

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## Low temperature InP/Si technology: From Si substrate preparation to epitaxial growth

L. González, Y. González, M.L. Dotor, D. Golmayo, D. Gómez and F. Briones

*Indexing terms: Semiconductor technology, Silicon, Indium phosphide*

InP layers have been grown on Si (001) substrates by using a low temperature process, both for the Si surface preparation (400°C < $T_{Si}$ < 550°C) and for the growth process itself ($T_g$ < 350°C) using solid source atomic layer molecular beam epitaxy. Strain-free InP on Si layers, with an etch pit density of ~1–2 × $10^7$cm$^{-2}$, showing an excellent morphology and good optical quality have been obtained using a buffer layer involving strain layer superlattices (SLS) of elastically dissimilar materials. This result implies an actual advancement towards monolithic integration of III-V devices to conventional CMOS-Si circuits.

The successful assessment of an actual III-V/Si technology is strongly dependent on reducing the temperature of the full growth process, from the Si surface preparation to the epitaxial growth itself, to make the III-V and CMOS based Si technologies compatible.

We present experimental results of InP epitaxially grown by an ALMBE [1] solid source at $T_g$ = 350°C on Si substrates, introducing an $In_{0.4}Ga_{0.6}As$/InP SLS as a dislocation filter structure. Both the Si surface substrate preparation and the growth itself are technological processes fully compatible with conventional silicon technologies. Results on the characterisation of these layers by X-ray diffraction etch pit density evaluation (EPD) and photolumi-