A Pspice-Compatible Model of PWM IC for Switching Power Converters with Soft-Start Characteristic

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Abstract

A new PSpice-based model is developed for simulating the soft-start characteristics of switching power supplies. Three commonly-used control ICs: TL494, SG3525 and UC3825 are considered. Using this model, starting characteristics of power supply circuits can be simulated effectively even with popular personal computers.

I. Introduction

There are many Spice-based models developed for simulating switching converters in recent years [1]-[5]. In general, there are two types of model used for simulating the control ICs: the detailed model and the state-space average model. The detailed model responds to details within the PWM switching cycle, including the effects of parasitics. However, to simulate the switching converter using the detailed model generally requires the use of high-performance workstation, and often takes unbearably long time. State-space average model, on the other hand, is a functional model that ignores the switching behavior but can be used very effectively to simulate the gross behavior of the converter. While both types of models have been used successfully, soft-start characteristics of switching converters have never been dealt with effectively.

Soft-start is a feature commonly used in commercial PWM control ICs to avoid converter output voltage overshoot, large transistor current spike and possible transformer saturation at the turn-on of the power supplies. Usually, the function is controlled through a pin called "dead-time (DT) control" or "soft-start (SS) control" of a PWM IC. By controlling the voltage applied to the DT-pin (or SS-pin), V_C, the output duty-cycle increases from zero to its steady-state operating value very "softly". Due to its importance for starting transient, soft-start has become a basic function of modern power supply circuits.

The focus of the present paper is to develop a soft-start subcircuit compatible with popular Pspice which can be used easily. By combining this model with the state-space average model proposed by Dr. V. Bello [1], the starting transient prediction can be achieve accurately and cost-effectively.

In this paper, Section II provides the related waveforms of a PWM IC to demonstrate the operation principles of the soft-start function. The details of how the soft-start subcircuit is developed and combined to the existing PWM model in [1] are given in Section III. The model parameters extraction will be given in section IV since , in some cases, they are not provided by the ICs' data sheets. In section V, three examples are presented to verify the developed model by comparing the simulation results and experimental results. Section VI concludes the paper.

II. Operation Principles of Soft-Start Function

The soft-start operation timing chart is illustrated in Fig. 1 to observe and study the starting behavior of a PWM IC. In the figure, V_e is the output voltage of error- amplifier, and V_C is the input voltage of the SS-pin. The timing clock of the IC, V_{ramp}, is essentially a sawtooth waveform generated by an internal oscillator. In general, the oscillation frequency, determined by external timing components R_T and C_T (or

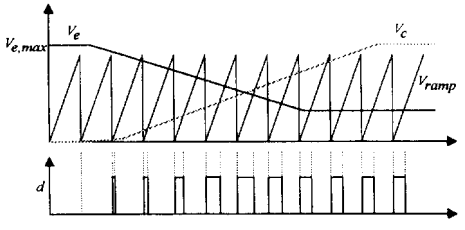

Fig.1 The Timing Chart of Soft-Start Operation

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only C_T), is equal to the switching frequency of the converter. Duty-cycle d is the output signal of the PWM IC and determines the turn-on ratio of the main switch.

When power is turned on, as shown in the timing chart, the voltage V_C rises slowly and is lower than the error-voltage V_e . The comparator's output pulse is mainly determined by V_C until V_e is equal to V_C . As the output voltage is increasing, the error-voltage V_e drops gradually in this period. However, when V_e exceeds V_C , then the IC enters the normal operation mode and is mainly controlled by the error-voltage V_e .

To compare with the turn-on transient shown in Fig. 1, Fig. 2 shows the timing diagram of a IC which does not employ the soft-start function. It can be seen that the output pulse width increases "abruptly" at the instant of turn-on and usually causes large stress on the components of the circuit.

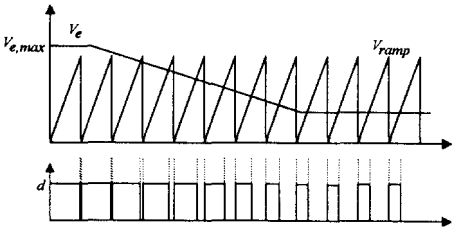


Fig.2 The Timing of a PWM IC without Employing Soft-Start Function

III. Modeling of Soft-Start Control Function

According to the description given in Section II, the subcircuit of soft-start can be developed and used. Take the commercial PWM IC, TL494, as an example. When the voltage at pin 4 is 2.3V, the maximum duty cycle is 0 percent. When the voltage is 0V, the maximum duty cycle is limited to 83 percent. When the applied voltage is between 0V and 2.3V, the relationship between the voltage and maximum duty cycle is linear. Summarize the above description, one obtain equation (1) for soft-start function of TL494.

$$d_{max} = 0.83 - 0.36V_C \qquad 0 \le V_C \le 2.3 \qquad \text{.....(1)}$$

where

V_C : voltage applied to the soft-start control pin

d_{max} : maximum duty cycle

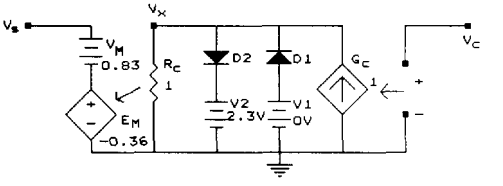


Fig.3 Soft-Start Subcircuit

The PSpice model for realizing equation (1) is given in Fig. 3. In the figure , the ideal diodes D1, D2, and the independent sources V1 and V2 limit the range of V_X between 0V to 2.3V. The controlled current source G_C and resistor R_C form a high input impedance buffer. Thus, V_X is equal to V_C while V_C is between 0V and 2.3V. From the model the output voltage V_S is given:

$$V_S = E_M + V_M = 0.83 - 0.36V_X$$
$$= 0.83 - 0.36V_C \qquad \text{when} \quad 0 \le V_C \le 2.3 \qquad \text{.....(2)}$$

From eqs.(1) and (2), it can be seen that V_S represents d_{max} . Figs. 4(a) and 4(b) show the block diagram and the entire model for TL494, respectively. The PSpice listing corresponds to Fig. 4(b) is given in Fig. 4(c). To be notice that the soft-start subcircuit is enclosed by the dotted line. The subcircuit beyond the dotted block is a PWM model (without soft-start function) similar to that developed in [1]. With the same approach given above, the soft-start model of other ICs can be obtained. The PSpice listing of subcircuits SG3525 and UC3825 are provided in the Appendix.

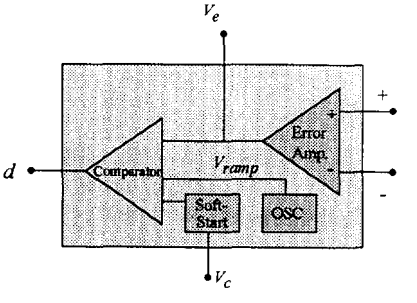


Fig.4(a) Block Diagram of PWM IC

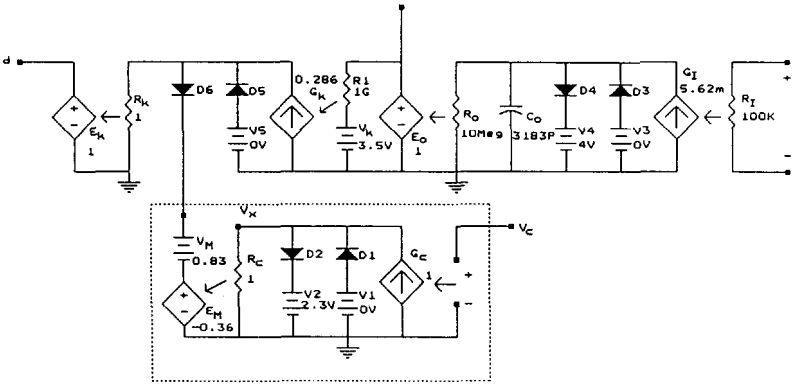


Fig.4(b) Entire Model for TL494

```
*%%%%%%%%%%%%%%%%%%%%%%%%%
*%%    PWM Control IC Model ---- TL494    %%
*%%%%%%%%%%%%%%%%%%%%%%%%%
* Connections:      1 non-inverting input(+)
*                  2 inverting input(-)
*                  3 compensation
*                  4 output
*                  5 soft-start
*
.SUBCKT TL494   1 2 3 4 5
*############################
*##     Error - AMP  Section     ##
*############################
          RI 1 2 100K
          GI 0 13 1 2 5.62m
          D3 12 13 ideal
          D4 13 11 ideal
          V3 12 0 0
          V4 11 0 4
          Ro 13 0 10MEG
          Co 13 0 3183P
          Eo 3 0 13 0 1
*############################
*##     Comparator  section     ##
*############################
          R1 3 21 1G
          Vk 21 0 3.5
          Gk 0 22 21 3 0.286
          D5 23 22 ideal
          D6 22 24 ideal
          V5 23 0 0V
          Rk 22 0 1
          Ek 4 0 22 0 1
*############################
*##     Soft-Start  section     ##
*############################
          Gc 0 31 5 0 1
          D1 32 31 ideal
          V1 32 0 0V
          D2 31 33 ideal
          V2 33 0 2.3V
          Rc 31 0 1
          EM 34 0 31 0 -0.36
          VM 24 34 0.83V
          .MODEL ideal D(N=0.001)
.ENDS
```

Fig.4(c) Listing of Subcircuit TL494

IV. Model Parameter Extraction

The model parameters described above are for a particular control IC TL494. For other control ICs, the models are similar but the parameters are different. These parameters are sometimes provided by the data sheet but sometimes must be extracted by experimental measurement. Fig. 5 shows the circuit diagram for parameters extraction. The procedures for the extraction are listed as following:

1) Connect V_{CC}-pin and GND-pin of the tested IC to the DC power supply.
2) Select adequate oscillation components, R_T and C_T, according to the operating frequency of the designed power circuit. Therefore, the sawtooth waveform generates.
3) This step is divided into two cases, depending on the synchronous schemes of the tested ICs. If the IC is worked with rising edge synchronous, the non-inverting input of error-Amp. is connect to the reference voltage and the inverting input is connected to ground. On the other hand, If the IC is worked with falling edge synchronous, it is necessary to exchang the connections.
4) Connect a variable resistor to the SS-pin and the reference voltage, as shown in Fig. 5. Therefore, the relationship between output duty-cycle and SS-pin voltage V_C can be obtained by adjusting the variable resistor and the pulse width measurement of the output waveform from oscilloscope.

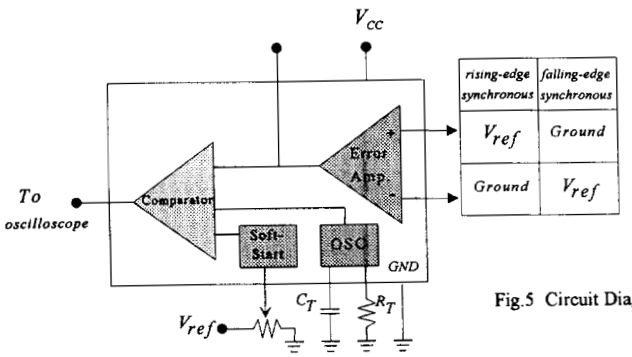
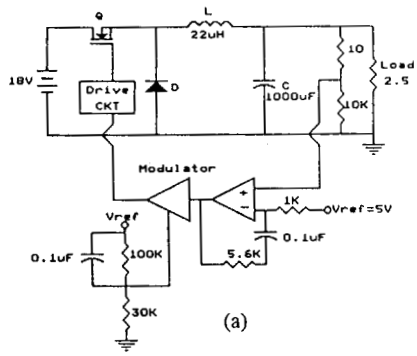
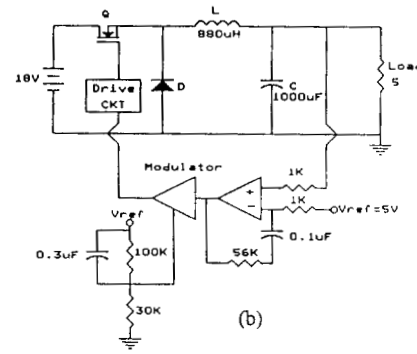


Fig.5 Circuit Diagram for Parameter Extraction

V. Verification

Using the proposed model for TL494, two buck converter circuits and a forward converter circuit shown in Fig. 6 are simulated. Fig. 7 shows the simulated results and the experimental results of the starting transient. In general, the agreement between the two is very good. From the figures, it also show the starting characteristic deviates from the reality when starting characteristic model is not included. The simulation time in this case is less than 20 seconds using a 386-based personal computer.





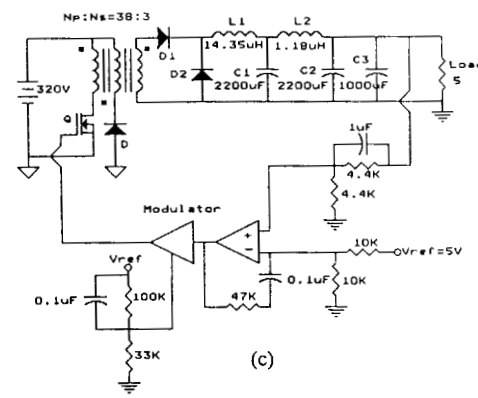
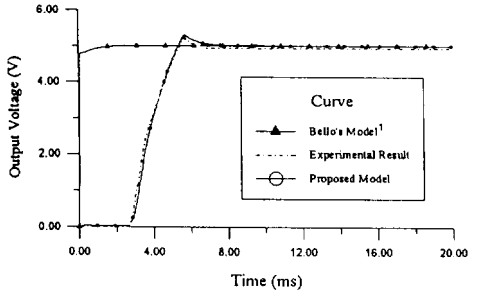
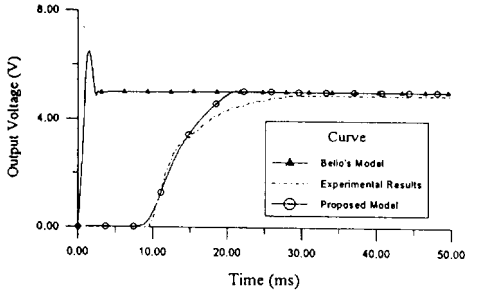


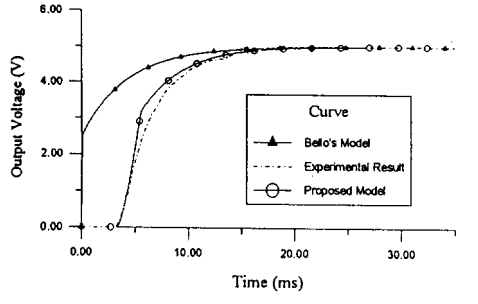
Fig.6 Three Circuits Used in Experimental Study
(a) and (b) : Buck Converters with Different Value of Circuit Elements
(c) : Forward Converter



(a)



(b)



(c)

Fig.7 (a) Experimental and Pspice Simulation Results of the Buck Converter in Fig.6(a)
(b) Experimental and Pspice Simulation Results of the Buck Converter in Fig.6(b)
(c) Experimental and Pspice Simulation Results of the Forward Converter in Fig.6(c)

1. Bello's Model (without modeling starting circuit) : see reference [1]

VI. Conclusions

The proposed model for simulating the starting characteristics provides the designer a very useful tool for assessing the component stress during the turn-on of a switching power supply. This model can be easily incorporated into existing converter simulation programs and can be used to simulate the starting characteristics very efficiently even with a popular 386-based personal computers.

Appendix

a. Listing of subcircuit SG3525

```
*%%%%%%%%%%%%%%%%%%%%%%%%
*%%   PWM Control IC Model ---- SG3525   %%
*%%%%%%%%%%%%%%%%%%%%%%%%
* Connections:      1 non-inverting input(+)
*                  2 inverting input(-)
*                  3 compensation
*                  4 output
*                  5 soft-start
*
.SUBCKT SG3525   1 2 3 4 5
*############################
*##     Error - AMP  Section     ##
*############################
          RI 1 2 100K
          GI 0 13 1 2 0.5m
          D3 12 13 ideal
          D4 13 11 ideal
          V3 12 0 0.2V
          V4 11 0 5.6V
          Ro 13 0 10MEG
          Co 13 0 795P
          Eo 3 0 13 0 1
*############################
*##     Comparator section     ##
*############################
          R1 3 21 1G
          Vk 21 0 0.8V
          Gk 0 22 21 3 0.4
          D5 23 22 ideal
          D6 22 24 ideal
          V5 23 0 0V
          Rk 22 0 1
          Ek 4 0 22 0 1
*############################
*##     Soft-Start section     ##
*############################
          Ic 0 5 50U
          Rss 5 0 1MEG
          Gc 0 31 5 0 1
          D1 32 31 ideal
          V1 32 0 0.8V
          D2 31 33 ideal
          V2 33 0 3.3V
          Rc 31 0 1
          EM 34 0 31 0 0.2
          VM 24 34 -0.16V
          .MODEL ideal D(N=0.001)
.ENDS
```

b. Listing of subcircuit UC3825

```
*%%%%%%%%%%%%%%%%%%%%%%%%%
*%%    PWM Control IC Model — UC3825   %%
*%%%%%%%%%%%%%%%%%%%%%%%%%
* Connections:      1 non-inverting input(+)
*                  2 inverting input(-)
*                  3 compensation
*                  4 output
*                  5 soft-start
*
.SUBCKT UC3825   1 2 3 4 5
*############################
*##      Error - AMP  Section      ##
*############################
          RI 1 2 100K
          GI 0 13 1 2 4.47m
          D3 12 13 ideal
          D4 13 11 ideal
          V3 12 0 0.5V
          V4 11 0 4.7V
          Ro 13 0 10MEG
          Co 13 0 159P
          Eo 3 0 13 0 1
*############################
*##      Comparator  section      ##
*############################
          R1 3 21 1G
          Vk 21 0 1.0V
          Gk 0 22 21 3 0.556
          D5 23 22 ideal
          D6 22 24 ideal
          V5 23 0 0V
          Rk 22 0 1
          Ek 4 0 22 0 1
*############################
*##      Soft-Start  section      ##
*############################
          Ic 0 5 9U
          Rss 5 0 1MEG
          Gc 0 31 5 0 1
          D1 32 31 ideal
          V1 32 0 2.25V
          D2 31 33 ideal
          V2 33 0 3.9V
          Rc 31 0 1
          EM 34 0 31 0 0.515
          VM 24 34 -1.158V
          .MODEL ideal D(N=0.001)
.ENDS
```

References:

1. V. Bello, "Computer-Aided Analysis of Switching Regulators Using SPICE-2", IEEE PESC 1980, pp. 112-119.
2. V. Bello, "Using the SPICE2 CAD Package for Easy Simulation of Switching Regulators in Both Continuous and Discontinuous Conduction Modes", Powercon 8, H-3, 1981.
3. V. Bello, "Using the SPICE2 CAD Package to Simulate and Design the Current Mode Converter", Powercon 11, H-2, 1984.
4. V. Joseph Thottuvelil, "Using SPICE to Model the Dynamic Behavior of DC-to-DC Converters Employing Magnetic Amplifiers", IEEE APEC 1990, pp.750-759.
5. Daniel Edry and Sam Ben-Yaakov, "A SPICE Compatible Model of Magamp Post Regulators", IEEE APEC 1992, pp.793-800.