

**SoC / IP 設計方法與驗證教學研討會**  
**執行成果報告**

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國立台灣大學電機系

吳安宇

執行單位：台灣大學電機工程學系  
執行期間：900501~900731

# **SoC / IP 設計方法與驗證教學研討會**

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## 一、前言：

針對國內 3C 整合學程及 3C 整合科技研究所需之課程與技術，台灣大學電機系、成功大學電機系及 NII 產業發展協進會，於民國 90 年 6 月 26 日至 28 日三天於台北(台大總圖國際會議廳)及台南(成大電機系演講廳)同時舉辦『SOC/IP 設計與驗證教學研討會』。本次研討會由教育部及行政院國家科學委員會贊助，對象為從事有關 SoC/IP 方面之學術界教授、學生及研究單位與產業界研發人士。針對國內 3C 整合學程及 3C 整合科技研究所需之課程與技術，邀請海外具豐富實務經驗的晶片計畫負責人，介紹時下業界系統晶片 (SoC) 設計之技術，包含了計畫的軟硬體分割、設計方法及驗證流程等。俾能使參與之學生、教授及工程師們能對系統整合及矽智產 (IP) 設計的相關實務問題有更清楚的認知。希冀經由講演者的經驗分享，提昇目前國內學術界及產業界之系統整合技術及 SoC/IP 設計環境。

## 二、活動舉辦情形：

### (一) 舉辦日期及地點

日期：90 年 6 月 26 至 28 日

地點：台北台大總圖國際會議廳

台南成大電機系演講廳

### (二) 工作進度表

主要工作項目	預定完成日期
邀請講員	90/2/15~3/25
計畫書確定	90/3/23
講座地點、經費來源及講員確定	90/3/25
經費補助申請文件送出	90/3/31
註冊、印刷及其他準備工作	90/5/20
教學研討會會前會議	90/6/1
教學研討會	90/6/26~6/28
結案報告送件	90/9/3

## 籌備委員及任務編組

姓名	服務單位	職稱	負責項目
夏漢民	NII 產業發展協進會	董事長	1、總召集人 2、整體規劃、推動與協調
陳良基	國立台灣大學 電機工程學系	教授	1、台北區召集人 2、整體規劃、推動與協調
劉濱達	國立成功大學 電機工程學系	教授	1、台南區召集人 2、整體規劃、推動與協調
吳安宇	國立台灣大學 電機工程學系	副教授	1、中美雙邊協調 2、台北會場事務規劃、協調 與執行監督
王進賢	國立中正大學 電機工程學系	副教授	台南會場事務規劃、協調 與執行監督
黃英哲	國立中山大學 電機工程學系	副教授	台南會場事務規劃、協調 與執行監督
張貞貞	國立台灣大學 電機工程學系	助理	會議行政
陳昭君	國立成功大學 電機工程學系	助理	台南會場庶務行政
黃玉安	國立台灣大學 電機工程學系	助理	台北會場庶務行政
蕭邦傑	NII 產業發展協進會	資訊管理師	協助整體規劃
陳少民	華美半導體協會	副會長	1、美國講員邀請 2、中美雙邊協調

## (四) 會議議程表

台北會場：

	6/26 (Tue)	6/27 (Wed)	6/28 (Thu)
8:30~9:00	報 到		
9:00~9:10	致 詞	講員介紹	講員介紹
9:10~10:30	Dr. David Chang	Dr. Johnny Wang	Dr. J. C. Wang
10:30~10:40	中 場 休 息		
10:40~12:00	Dr. David Chang	Dr. Johnny Wang	Dr. J. C. Wang
12:00~13:00	午餐時間 (自理)		
13:00~14:20	Dr. David Chang	Dr. Johnny Wang	Dr. J. C. Wang
14:20~14:40	中 場 休 息		
14:40~16:00	Dr. David Chang	Dr. Johnny Wang	Dr. J. C. Wang
16:00~16:30	Panel Discussion	Panel Discussion	Panel Discussion
16:30	散 會		

台南會場：

	6/26 (Tue)	6/27 (Wed)	6/28 (Thu)
8:30~9:00	報 到		
9:00~9:10	致 詞	講員介紹	講員介紹
9:10~10:30	Dr. Johnny Wang	Dr. J. C. Wang	Dr. David Chang
10:30~10:40	中 場 休 息		
10:40~12:00	Dr. Johnny Wang	Dr. J. C. Wang	Dr. David Chang
12:00~13:00	午餐時間 (自理)		
13:00~14:20	Dr. Johnny Wang	Dr. J. C. Wang	Dr. David Chang
14:20~14:40	中 場 休 息		
14:40~16:00	Dr. Johnny Wang	Dr. J. C. Wang	Dr. David Chang
16:00~16:30	Panel Discussion	Panel Discussion	Panel Discussion
16:30	散 會		

三、研討會內容及概要：

主辦單位特別邀請了在 SoC/IP 應用領域極具盛名的 Dr. David Chang, VP of Engineering empowerTel Networks; Dr. Johnny Wang, Senior Engineering Manager at Internet Platform Laboratory, NEC Electronics 及 Dr. Jin-Chin Wang, VLSI Integration Engineering Manager, Broadcom Corporation. 為本次研討會做演講；為深入介紹完整的 SoC 設計流程，本次研討課程將採取實例研討方式，演講內容包含

1. 『Network Processors – Architecture to Integration』
2. 『SOC Design Methodology for An Multimedia Controller』
3. 『SoC Design Example: Internet Appliance』

等三個單元。各單元的講演者將分別以一整天的時間，藉由其在資訊家電、多媒體、網路晶片的研發計劃，來呈現符合市場趨勢的 SoC 設計經驗，內容重點為(註：各講師的簡介及演講內容請參考附件資料)：

- 背景介紹：市場趨勢和技術基礎
- 計畫規格及設計流程
- 主要 IP 發展：設計流程及驗證
- 系統整合時的 IP 整合及驗證：例如，軟、硬體協同模擬和驗證
- 系統整合測試及整合於電路板上的驗證
- EDA 工具在 SoC 設計流程中之角色
- SoC 設計流程之未來的發展趨勢

- 除以一天的課程講解其系統晶片整合設計，並安排一場座談會（Panel Discussion）來讓講員及學員互動討論。

#### 四、心得與成效：

本次研討會的內容分三天進行，三位主講人均來自不同的領域，且對 SoC/IP 設計方法與驗證均有豐富的經驗，內容十分的豐富充實，透過講師深入淺出的講解方式，此令學員豁然開朗受益非淺，每人均有了不少的收穫。研討會總共有三種不同的主題，因此可由不同的專家學者汲取更多思考的角度與方式。藉由講演者的經驗分享，可幫助提昇目前台灣學術界及產業界之系統整合及 SoC/IP 設計環境，並能與各界從事相同的工作的產、學業界人士的共聚一堂及相互切磋。同時透過座談會（Panel Discussion），增加了講員與現場學員的互動，激發新的想法並強化吸收成效。

#### 五、聯絡人：

姓名	職稱	服務機構	電話	傳真
黃玉安	助理	國立台灣大學 電機工程系	(02) 23635251 轉 234	(02) 23681679

#### 六、附件：

附件一：講師簡介及課程摘要

附件二：支出明細表：

附件三：研討會教材及海報

## 附件一：講師簡介及課程摘要

### **Talk1 : Network Processors – Architecture to Integration**

#### *Abstract:*

Networks Processors are programmable processors designed specifically to handle the tasks of packet processing, manipulation and forwarding. In particular, they include special functionality to reduce memory and/or caching latencies and to accelerate common functions such as classification, checksums, lookups, etc.

In this tutorial, I will give an overview of the Network Processor Space. We will look into different characteristics of Networks Processors in Data Communications (to handle data) vs. Telecommunications (to handle voice). Then we will learn design issues related to Network Processor Hardware and Software. We will discuss architectures and applications of some popular Network Processors from Agere Systems, Conexant/MindSpeed, Motorola/C-Port, and IBM. Then I will use empowerTel's MxP1070 (Media Express Processor) as the case study for a SoC (System-on-a-Chip) design which is used in Voice over Internet Protocol (VoIP) carrier-class switch system. Finally, I will use this chip implementation to show the challenges of SOC design methodology in various aspects (architecture / logic design / verification / validation / DFT / timing / physical design), the challenges of VDSM (Very Deep Sub-Micron) design, and the design issues related to soft/hard IP integration.

#### *Speaker 1 :*

*David C. W. Chang, Ph.D.*

*Vice President, Engineering*

*empowerTel Networks*

David Chih-Wei Chang received his Ph.D. degree in Electrical Engineering from the University of Southern California in 1988.

Currently he is Vice President of Engineering and is responsible for the Media Express Processors development at empowerTel Networks. From 1997 to 1999, he was Director of Engineering of Desktop Graphics and Integration Graphics (with VIA, ALI) at Trident Microsystems. From 1991 to 1997, he was Sr. Manager at Fujitsu/HAL Computer Systems, where he worked on SPARC 64-bit 4-way

super-scalar, speculative out-of-order execution microprocessors. From 1988 to 1991, he was a Sr. Staff Engineer at Siemens/Pyramid Technology, where he worked on RISC-based multiprocessor design. From 1985 to 1988, he was a Design Engineer at Citicorp/Quotron, designing tightly-coupled multiprocessors.

Dr. Chang was a part-time professor in the Electrical Engineering Department at the San Jose State University from 1989 to 1993. He holds four patents and has published fifteen technical papers in VLSI/computer/networking areas. He is a Sr. Member of IEEE, and on the Board of Directors of CASPA (Chinese American Semiconductor Professional Association). His research interests include telecommunication/networking, computer architecture, multimedia, and VLSI/CAD.

## **Talk2 : SOC Design Methodology for An Multimedia Controller**

### *Abstract:*

In this tutorial, an SOC design flow will be presented in a greatly detailed fashion. We will emphasize on the area of chip level design, hierarchical netlist partition, design for test, netlist release, timing closure to GDS sign-off. We will also talk about the design methodology migration when face different deep submicron technologies, e.g., how to address the EM issues, coupling issues, and IR drop issues. At the end, we will show you a multi-medium SOC design evolvement.

### *Speaker 2 :*

*Jin Chin Wang, Ph.D.*

*VLSI Integration Engineering Manager*

*Digital Video Technology*

*Broadcom Corporation*

Jin Chin Wang received his Ph.D. degree in Computer Engineering from the University of Southern California in 1990, his M.S. degree in Electrical Engineering from the University of Southern California in 1987, and his B.S. degree in Electrical Engineering from the Chung Yuan Christian University in 1982.

Currently he is the VLSI Integration Engineering Manager of Digital Video Technology at Broadcom Corp. and is responsible for the high-end set-top box backend chip BCM7020, BCM7030 VLSI development. From 1997 to 1999, he was a Senior Engineering Manager of Advanced Processor Development at NEC Electronics, where he worked on MIPS 64-bit 2-way super-scalar VR5464A and VR5432 microprocessors. From 1996 to 1997, he was a Staff Engineer at SunMicro Electronics, where he worked on Ultra-Sparc III reference platform development. From 1991 to 1996, he was an Advisory Engineer at IBM-Austin, where he worked on RISC-based multiprocessor chipset design. From 1990 to 1991, he was a Staff Design Engineer at Tandem Computers, designing tightly coupled fault tolerant multiprocessors.

Dr. Wang holds three U.S. patents with 12 patent application pending for review, has published fourteen technical referred papers in IEEE transaction of computers and in other IEEE conference proceedings in cache multiprocessors area. He is a member of IEEE, and an honor member of Phi Tau Phi. His research interests include VLSI integration, SOC flow, computer architecture, digital video, and microprocessor.

### **Talk3 : SoC Design Example: Internet Appliance**

#### *Abstract:*

Internet Appliance is becoming a major post-PC product. The nature of IA - is a service product. Estimated sales volume will exceed PC before year 2005. Besides OEM manufacturers, there are many new players, such as Internet Service Provider and Software / System Integrator, etc.

Internet Appliance (pocket PC, handheld PC and set top box etc.) is not a PC product. PC is a standard product with WinTel solutions. For IA products however, there are too many integration options with different CPU / chipset / peripherals / OS / GUI / Browser etc. to fit different applications.

Brief discussions of key hardware components (CPU, Memory, I/O bus, communication, graphics, LCD panel, and battery etc.) and software (OS, debug monitor, peripheral drivers and application programs etc.) selection for various IA markets (PPC, HPC, STB) will be covered in this presentation. Middleware and system integration are stepping stones for a SOC solution. Some design cases will be used as examples for discussion in this presentation as well.

In summary, IA is comprised of 3C (Computer, Communication and Consumer) in one service product. There are many different applications with large sales potential. To be successful in this new opportunity, it requires good tailored solutions for a variety of markets and the ability to bundle correct hardware and software along with the proper endorsement from customers as well as the lowest possible cost. These questions demand the full attention from all IA manufacturers.

*Speaker 3 :*

*Mr. Jonny Wang*

*Senior Engineering Manager*

*NEC*

Johnny Wang is a senior engineering manager at Internet Platform Laboratory of NEC Electronics. His major job responsibilities are leading hardware engineers team and software engineers team to build Internet reference design, based on NEC's VR MIPS CPUs and chipsets, for NEC's customers.

His current job focus is 'Internet Appliance' and 'Digital Set Top Box' reference design. In the past several years, his team had built pocket PC and hand held PC reference design with complete OS, peripheral device drivers and application programs ported.

To help NEC's customers to reduce time to market, his team makes reference design very close to production ready prototype with finished mechanical mockup run by rechargeable battery. The major targeted OS for their reference design boards were based on WindowsCE. The newly targeted OS is Linux OS.

Due to his job requirements, he had many chances to talk to worldwide IA vendors to jointly define appropriate system architecture for various Internet appliance platform. In order to get better system integration, he has to talk to various hardware / software vendors to understand new available technologies on the market so that he can recommend best suitable solutions for NEC's IA customers.

He has BSEE and MSEE degrees.

附件二：支出明細表：

經費核定清單

項 目	申請金額	說明
人事費	NT\$10,000	臨時工資
雜支	NT\$368,000	場地出租費、器材租用及搬運費、會場佈置、演講器材、租車費、國內航空及接機費用、印刷打字費、郵電費、文具紙張費、國內交通旅運費、影印、研討會及座談會出席、規劃諮詢費、底片、沖洗相片、餐點費
合計	NT\$378,000	

支出明細

【人事費】

項目	明細	金額	總金額
臨時工資	台南工作人員	4,608	NT \$ 10,000
臨時工資	台北工作人員	5,392	

【雜支】

項目	金額	總金額
場地出租費	40,500	NT \$ 36800
會場佈置	45,904	
印刷打字費	65,389	
郵電費	13,841	
文具紙張費	13,073	
國內交通旅運費	9,010	
影印	30,708	
研討會及座談會出席	7,000	
規劃諮詢費	46,000	
底片	410	
沖洗相片	622	
餐點費	95,543	

總計：NT \$ 378,000