A Programmable Filter with Self-Tuning for DMT VDSL Receiver

Chia-Hua Chou
Department of Electrical Engineering,
National Taiwan University,
Taipei, Taiwan
chou@aic.ee.ntu.edu.tw

Chien-Chih Lin
Department of Electrical Engineering,
National Taiwan University,
Taipei, Taiwan
tmt@aic.ee.ntu.edu.tw

Chorng-Kuang Wang
Graduate Institute of Electronics Engineering and,
Department of Electrical Engineering
National Taiwan University
ckwang@cc.ee.ntu.edu.tw

ABSTRACT

This paper presents a programmable filter with a self-tuning mechanism. Conformed with the DMT-VDSL system, the filter is configured as a 4-th order Chebyshev low-pass filter with programmable bandwidth in which the ripple is set to $0.5dB$. The cut-off frequencies are 1.104×2^n MHz, where n is 0, 1, 2, 3, 4, corresponding to different transmission rates. The filter is self-tuned by the proposed tuning mechanism that is based on the relation between DC and fundamental components of a filtered clock signal. Peak-and-Valley detection is employed to observe the two frequency components in time domain. Implemented in $0.35\mu m$ 1P4M digital CMOS technology, the circuit occupies an active area of $1.3 \times 1.4mm^2$. According to the post-layout simulation, it achieves 55dB THD using 2V supply voltagem while the output swing is $120mV_{pp}$. The power consumption for the core filter is 2.8mW, whereas the overall system, including the filter, the output buffer, and the tuning circuits, consumes $28mW$ power.

1. INTRODUCTION

In the Very-high-speed digital subscriber loop (VDSL) receiver path, a low-pass filter is required to reject interferences as well as high frequency components of POTS or ISDN, and to equip anti-aliaing for analog-to-digital conversion. Corresponding to different data rates transmitted and the variety of subchannel number, this filter requires to be programmable. Based on T1E1.4 specification [3], the subcarrier number is $N_{sc} \times 2^n$ with $N_{sc} = 256$ and n being 0, 1, 2, 3, or 4. Since the subchannel spacing is 4.3125 kHz, the passband frequency of this filter will be 1.104×2^n MHz, where n is 0, 1, 2, 3, or 4.

In view of the poor absolute accuracy in time constants of continuous-time (CT) filter, automatic tuning mechanism is unavoidable in CT filter design. The filter tuning strategies may be separated into two categories - direct and indirect [4]. The former feeds the reference signal and tunes the filter directly by detecting the output from the filter. While the latter is based on master-slave approach in which a master circuit with similar time constants as in the actual filter, also called slave, is tuned to track an external reference and the tuning signal is indirectly applied to tune the slave. Eliminating replica circuits in indirect scheme, this design incorporates a direct tuning mechanism based on the proposed clock reference detection.

This paper is organized as follows. Section 2 describes the filtercircuit architecture. The circuit simulation and its layout is shown in section 3. Finally, the conclusion is drawn in section 4.

2. CIRCUIT ARCHITECTURE

Fig.1 shows the complete block diagram of the filter and the tuning circuit. This filter incorporates the automatic gain-

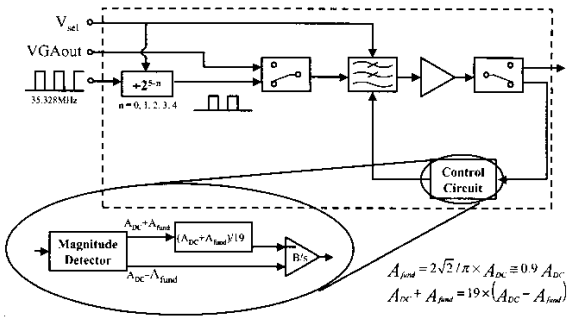

Figure 1: Filter and tuning circuit block diagram

controlled amplifier (AGC) to accomplish the analog frond-end in the receiver chain. In order to conform the DMT VDSL system, the filter is configured as a 4-th order Chebyshev low-pass filter with 0.5dB ripple in the passband. The passband corner frequency is programmable to be 1.104×2^n MHz, where n is controlled by the V_{sel} signal. The filter is followed by an output buffer stage to drive the succeeding circuits in AGC. The switching circuits select the input signal of the filter from the variable gain amplifier (VGA) in the

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previous stage and its output signal to ADC for digitization during general operational mode.

When the circuit is switched to tuning mode, the filter has the input signal from a reference clock. The clock frequency is 35.328MHz, which is divided by 2^{5-n}, where n is set by V_{sel} signal. Expanded by Fourier series, the output signal of this clock signal passed through the designed filter whose -3dB cut-off frequency is set to f_0 will be

$$CLK_{out}(t) = A \times \{b_0 + \sum_{n=1}^{\infty} b_n \cos(2\pi n f_0 t)\} \quad (1)$$

By observing the DC and fundamental frequency components, it can be derived that

$$\frac{b_1}{b_0} = \frac{\pi/2}{0.5} \times \frac{1}{\sqrt{2}} \approx 0.9 \quad (2)$$

Fig.2 illustrates the filtering of the clock signal mentioned above.

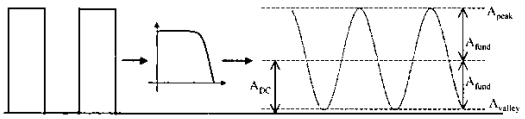

Figure 2: DC shifted clock signal before and after filtering

If the -3dB corner frequency is precisely at the clock frequency, the amplitude of the fundamental frequency component, A_{fund}, of the filtered clock signal will be 0.9 times the DC component, A_{DC}. Thus, the peak and valley of the waveform in the time domain will be,

$$A_{peak} = 19 \times A_{valley} \quad (3)$$

By (3), the filter cut-off frequency can be directly tuned to meet the ratio 19. However, this tuning scheme is only suitable for high order filters whose transition band is sharp. In this design, the 4-th order Chebyshev filtering function is employed, which provides about 26.5dB/oct in the transition band and causes the second harmonic component to be 27dB below the fundamental frequency component.

The capacitance values, with C_1 is used for active inductance synthesis and C_2 is the capacitor from LC-ladder prototype, in Gyrator-C filter can be expressed by:

$$C_1 = \frac{L_0 \times Z \times g_m^2}{FSF} = \frac{L_0 \times g_m}{FSF} \quad (4)$$

$$C_2 = \frac{C_0}{FSF \times Z} = \frac{C_0 \times g_m}{FSF} \quad (5)$$

where g_m is the transconductance of the gyrator, Z is the impedance scaling factor, and FSF is the frequency scaling factor. The equality of (4) and (5) holds by setting $Z = 1/g_m$. Since C_1, C_2, L_0, C_0 are constants, the cut-off frequency of the filter $f_{3dB} = \frac{1}{2\pi} \times FSF$ is proportional to the transconductance g_m. Hence the cut-off frequency can be tuned by adjusting the transconductance in the circuit.

Mathematical model is constructed to perform the analysis of the tuning mechanism. Since the DC gain of the filter is almost constant irrelevant of tuning, the DC component at the output of the filter can be normalized to 1. Hence the fundamental frequency component of the filter output has the amplitude A_{fund} as

$$A_{fund}(v_e) = \begin{cases} 0.9 + G_f \times v_e & , v_e \leq \frac{0.1}{G_f} \\ 1 & , v_e > \frac{0.1}{G_f} \end{cases} \quad (6)$$

where G_f is the gain of the filter from its control signal input to the fundamental frequency component of the clock signal after filtering. The magnitude detection can be expressed as:

$$v_{det}(A_{fund}) = -\frac{18}{19} + G_{det} A_{fund} \quad (7)$$

where $G_{det} = \frac{20}{19}$ when A_{DC} is normalized to 1. The complete mathematical model is constructed as shown in Fig.3. The closed loop transfer function of the tuning mechanism

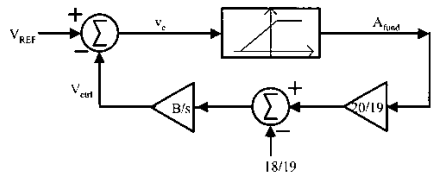

Figure 3: Mathematical model of the tuning mechanism

is:

$$H(s) = \frac{G_f \times G_{det} \times B}{s + G_f \times G_{det} \times B}, \quad v_e \leq \frac{0.1}{G_f} \quad (8)$$

When $v_e > \frac{0.1}{G_f}$, the output of the filter becomes a constant 1, and the loop acts like an integrator. v_{ctrl} thus is increased to pull v_e into the condition of (8). With the first order transfer function of (8), the error signal will come to 0 when f_{3dB} of the filter is adjusted to the desired frequency.

2.1 Low-Pass-Filter

For high frequency operation and insensibility to process variation, a *Gm-C* circuit based on *LC* ladder prototype, as shown in Fig.4, is used to synthesize the filter. Each transconductor in this filter is designed to be programmed by the V_{sel} signal as indicated in the figure. The transconductance of Gm_i ranges from g_{mui} to $16g_{mui}$, where g_{mui} is the unit transconductance value. Fig.5 shows the transcon-

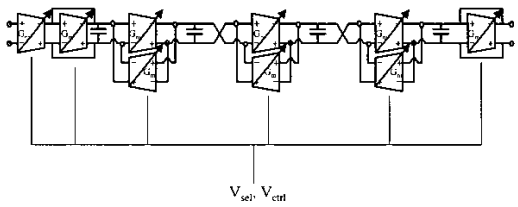

Figure 4: 4^{th} Order gyrator-c low-pass-filter

ductor schematic for the *Gm-C* filter. The input stage contains M_1 and M_2 that convert the voltage signal into current signal. The V_{sel} signal controls the transmission gate which

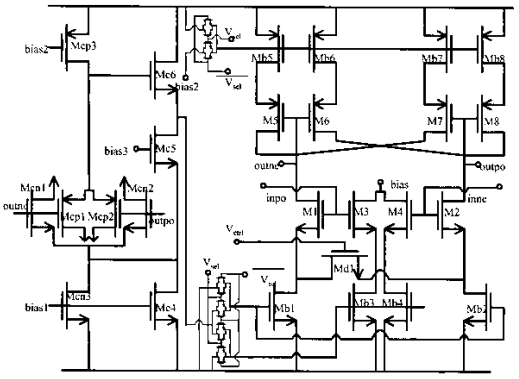

Figure 5: G_m cell using NRL(Negative Resistance Load)

turns on/off the bias current provided by M_{b1} to M_{b8} to select one of the five G_m values in each transconductor stage. A dummy input pair by M_3 and M_4 is added to compensate the parasitic capacitance at the input. V_{ctrl} is generated from the tuning circuits and used to fine tune the G_m value through the degeneration transistor M_{d1} such that the filter bandwidth can be set to the predefined value. To increase the output impedance without sacrificing power dissipation, the negative resistance load (NRL) by M_5-M_8 is used [2].

A complementary common mode feedback (CMFB) is configured for low-voltage operation. An n-type source-coupled pair (n-SCP) by M_{cn1} and M_{cn2} and a p-type SCP (p-SCP) by M_{cp1} and M_{cp2} are utilized as the input stage similar to conventional rail-to-rail amplifiers. The CMFB voltage is extracted by the n-SCP with a common gate amplifier and the p-SCP with a source follower and fed back to the tail currents for the core cell. The two pairs, n-SCP and p-SCP, compensate the nonlinearities of each other and hence increase the output swing of the Gm cell.

2.2 Magnitude Detector

The magnitude detection circuit is essentially a peak detector that is taken to find the peaks and valleys of the filtered clock waveform. As shown in Fig.6, the detector cell is composed of an amplifier, a current source, and a capacitor. The magnitude detector comprises two cells that take turns to track the peak value. A discharge MOSFET is added to each cell for resetting the peak value stored in the capacitor every two clock periods. Thereby, the peak value can be continously extracted and the detector does not produce extra poles in the loop. The valley detector is based on the same architecture and uses NMOS for the current source and PMOS for the discharging transistor.

Due to the finite gain of the amplifier, the peak detector suffers from an offset error as

$$V_{err} = V_o - V_{i,pk} = \frac{\Delta V}{G_{amp}} \tag{9}$$

where ΔV is the voltage difference between the current source bias point and the gate voltage to turn off the current source, and G_{amp} is the gain of the amplifier. Considering the technology used in this design, the error is about 50mV which causes about 3% cut-off frequency drift. To overcome this problem, the current source is biased at its subthreshold region [1]. Thus, ΔV can be reduced and the V_{err} may be reduced within 10mV.

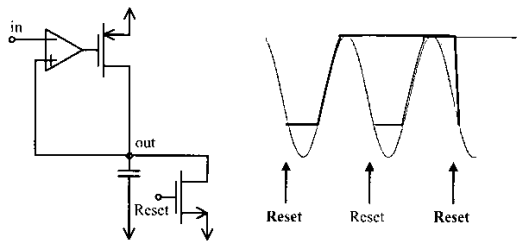

Figure 6: Magnitude detector

2.3 Division-by-19 and -3dB Cut-off Detection

Equation (3) is used to monitor the accuracy of the filter cut-off frequency. It calls for a divide-by-19 circuits to compare the extracted valley with the $\frac{1}{19}$-th the peak value. This division is realized with a resistor string. The voltage between the terminals of the $1k\Omega$ resistor in the $9k$-$1k$-$9k$ string is $\frac{1}{19}$ times the input of the resistor string from the peak detector. In this design, P+ diffusion without silicide is chosen for the resistors. The required tolerance for resistor matching is within $\pm 4\%$ which can be achieved by the technology used.

The error signal is therefore generated by subtracting the output of divide-by-19 circuit from the valley signal generated by the magnitude detector. It is followed by an integrator to generate the mean value that controls the -3dB cut-off frequency of the main filter. The subtraction and integration circuit is realized by a folded-cascode amplifier with two input pairs, as shown in Fig.7. The gate nodes of M_{11}, M_{12}, M_{13}, and M_{14} are connected to node A so as to make the cascode stage immune against process variation in low voltage design.

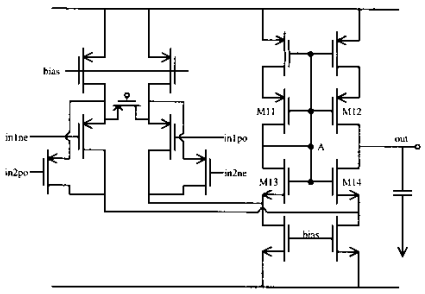

Figure 7: Subtraction and integration

3. CIRCUIT SIMULATION AND LAYOUT

Using $0.35\mu m$ CMOS technology, the filter with five steps programmability is designed and its frequency responses in temperature and process variation conditions are simulated.

For each designated corner frequency, the tuning range attains to ±30% extent. Fig.8(a) shows the frequency response under temperature variation from $0°C$ to $100°C$. In the presence of ±20% capacitance variation in the filter, the passband bandwidth can be tuned to the predefined range, as shown in Fig.8(b). The closed-loop simulation shows

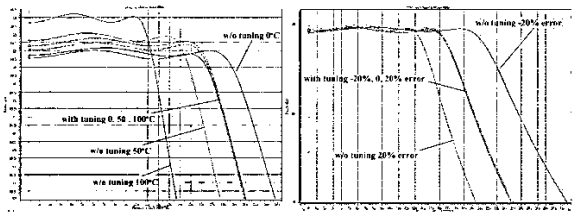

Figure 8: Filter's responses when subject to (a) temperature variations (b) capacitance variations

that the cut-off frequency can be controlled to 5% accuracy [5], which meets system requirement. Only the DC gain is slightly affected during varying conditions, but this can be resolved by the cooperating AGC loop. The normalized frequency responses of the filter for 1.104×2^n MHz programmability are shown in Fig.9. The transient simulation

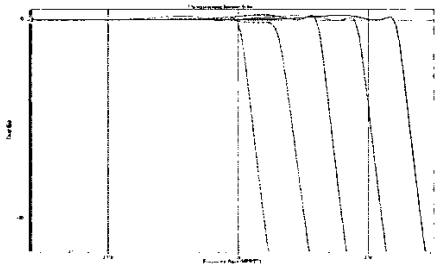

Figure 9: 5-Step normalized frequency responses

shows that the total harmonic distortion with 10 harmonics inside the passband is below $-55dB$. Operated in 2V supply voltage, the filter consumes 2.8mW. Together with the output buffer and the tuning circuit, the total circuit consumes 29mW. Fig.10 shows the layout of this design and Table1 displays the performance summary from the post-layout simulations. This chip is sent to be fabricated using 0.35μ 1P4M digital CMOS technology.

Technology	TSMC $0.35\mu m$ CMOS 1P4M
Supply voltage	2V
Filter type	4-th Order Chebyshev LPF with $\delta_p = 0.5dB$
Cut-off frequency	1.014×2^nMHz with n=0, 1, 2, 3, 4
Total harmonic distortion	$< -55dB$ at $150mV_{pp}$ input
Power consumption	Filter: 2.8mW Output buffer: 19.2mW Tuning circuit: 6mW

Table 1: Post-layout simulation results

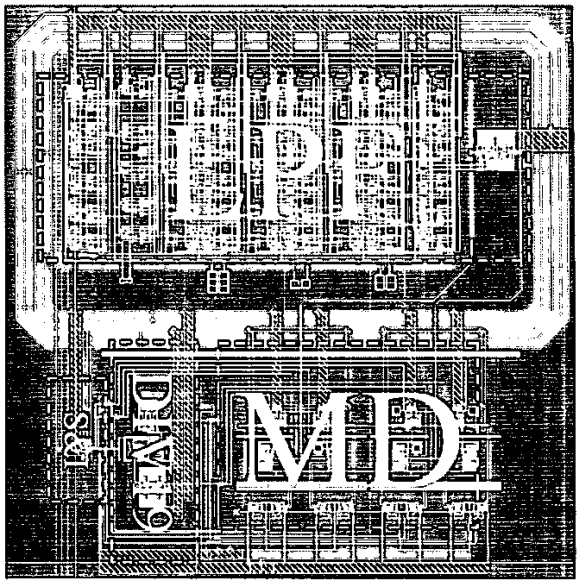

Figure 10: Layout

4. CONCLUSIONS

A programmable low-pass filter for DMT-VDSL receiver is proposed in this paper. Its cut-off frequency can be programmed to be 1.104×2^n MHz, where n is 0, 1, 2, 3, or 4, depending on the transmission rates specified by the system. A new mechanism to self-tune the corner frequency is presented, which is based on the ratio between the magnitudes of DC and fundamental components of a filtered clock signal. The filter consumes a little power and is used to cooperate with an AGC loop to provide the analog front-end for VDSL receiver.

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