Current-mode pseudo-exponential circuit with tunable input range

Cheng-Chieh Chang and Shen-Iuan Liu

A current-mode pseudo-exponential circuit is presented based on Taylor's series expansion. It is composed of MOS transistors operating in saturation and its input range can be tuned by adjusting the biased current. The proposed circuit has been verified with the 0.8μm CMOS technology by HSPICE simulations. The simulation results confirm the feasibility of the proposed pseudo-exponential circuit.

Introduction: Exponential circuits are one of the important building blocks for telecommunication applications, medical equipment, hearing aid and disk drives, etc. [1 – 5]. Traditionally, they are implemented using the exponential-law characteristics of transistors, such as bipolar transistors and MOS transistors in weak inversion. Since MOS transistors in weak inversion have a poor frequency response and limited input range compared with those in saturation, pseudo-exponential circuits [1 – 4] have been presented using several kinds of approximation method.

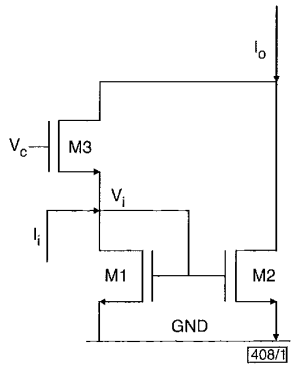

Fig. 1 *Current-mode building block [6] for proposed pseudo-exponential circuit*

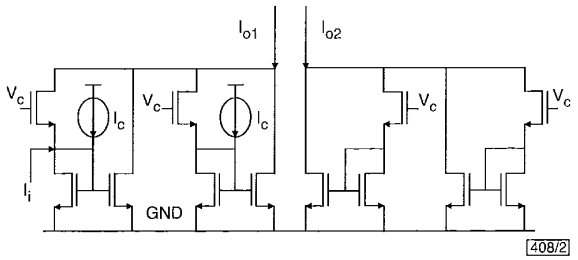

Fig. 2 *Proposed current-mode pseudo-exponential circuit with tunable input range*

Circuit description: The Taylor's series expansion of the exponential function can be expressed as

$$e^x = 1 + \frac{1}{1!}x + \frac{1}{2!}x^2 + \cdots + \frac{1}{n!}x^n + \cdots \quad (1)$$

If $x \ll 1$, eqn. 1 can be approximated as

$$e^x \simeq 1 + \frac{1}{1!}x + \frac{1}{2!}x^2 \quad (2)$$

The calculated results show that, when $-0.575 \leq x \leq 0.815$, the errors of eqn. 2 will be < 5%. Furthermore, the generalised expression for eqn. 2 can be written as

$$2b^2 \cdot e^{\frac{a}{b}x} \simeq b^2 + (b + ax)^2 \quad (3)$$

where a and b are constants and $|(a/b)x|$ should be less than unity.

The building block [6] for the pseudo-exponential function of eqn. 3 is shown in Fig. 1. Assume that all the transistors operate in saturation. The characteristic function of Fig. 1 can be given as

$$I_O = G + \frac{I_i^2}{4G}$$

where I_O is the output, I_i is the input and $G = (K/2)(V_C - 2V_T)^2$ is a constant. It is a current-mode squarer and its operating conditions are $V_C - V_i > V_T$ and $V_i > V_T$, where $V_i = V_C/2 + I_I/[2K(V_C - 2V_T)]$. According to eqn. 3, to synthesise a pseudo-exponential function, two squarers are needed. The proposed current-mode pseudo-exponential circuit is shown in Fig. 2. Two left-hand building blocks with biased currents I_C realise the pseudo-exponential function with an extra DC term and two right-hand building blocks without the biased currents are used to cancel the unexpected DC term. The output current of Fig. 2 can be defined as follows:

$$I_O \equiv I_{o1} - I_{o2} = \left[G + \frac{(I_C + I_i)^2}{4G}\right] + \left(G + \frac{I_C^2}{4G}\right) - G - G \quad (4)$$

According to eqn. 3, it can have the pseudo-exponential function

$$I_O = \frac{I_C^2}{4G} + \frac{(I_C + I_i)^2}{4G} \simeq \frac{I_C^2}{2G} e^{\frac{I_i}{I_C}} \quad (5)$$

where eqn. 5 should meet $|I_i/I_C| < 1$. If the input current $|I_i| < I_C$, the biased current I_C can adjust its input range.

To consider the mobility reduction effect [7] of transistors, the simplified I-V characteristics of an NMOS can be modelled as

$$I_D = \frac{K(V_{GS} - V_T)^2}{1 + \theta(V_{GS} - V_T)} \quad (6)$$

where θ is the mobility degradation parameter. Substituting eqn. 6 into eqn. 4 and neglecting the higher-order terms of θ, the output current deviation can be given as

$$\Delta I_O \simeq \frac{2I_i\Delta I_i + (\Delta I_i)^2}{4G} \quad (7)$$

where $\Delta I_i = K\theta[(V_i - V_{SS} - V_T)^3 - (V_C - V_i - V_T)^3]$. The mobility reduction will contribute the nonideality.

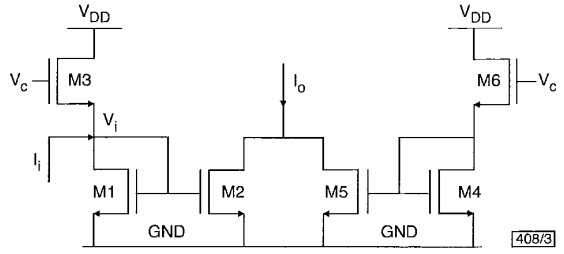

Fig. 3 *Compact current-mode pseudo-exponential circuit*

In fact, the drain current of M2 in Fig. 1 possesses the square-law characteristic and can be given as

$$I_{M2} = K\left[\left(\frac{V_C}{2} - V_T\right) + \frac{I_i}{2K(V_C - 2V_T)}\right]^2 \quad (8)$$

A compact pseudo-exponential circuit can also be realised, as shown in Fig. 3. According to eqn. 3, the output current of this pseudo-exponential circuit can be expressed as

$$I_O = I_{M2} + I_{M5} \simeq 2K\left(\frac{V_C}{2} - V_T\right)^2 \cdot e^{\frac{I_i}{K(V_C - 2V_T)^2}} \quad (9)$$

However, to keep all transistors operating in saturation, the biased voltage V_C is generally fixed. This results in a fixed input range rather than the tunable one in Fig. 2.

Simulation results: The proposed current-mode pseudo-exponential circuit in Fig. 2 was verified in 0.8μm CMOS technology by HSPICE simulations. The aspect ratios of all transistors in Fig. 2 were 5μm/5μm. The proposed circuit was simulated with a supply voltage of 3V and biased voltage V_C = 3V. The simulated transfer curves with the different biased currents I_C are shown in Fig. 4 and the ideal curves are calculated from the left-hand part of eqn. 3. For the biased current I_C = 50μA, the output dynamic range of Fig. 2 is ~12dB with an error < 2.5% when the input current ranges between –30 and 47μA. If the biased current I_C =

30μA, the output dynamic range is 13dB with an error < 2% when the input current ranges between –17.5 and 30μA.

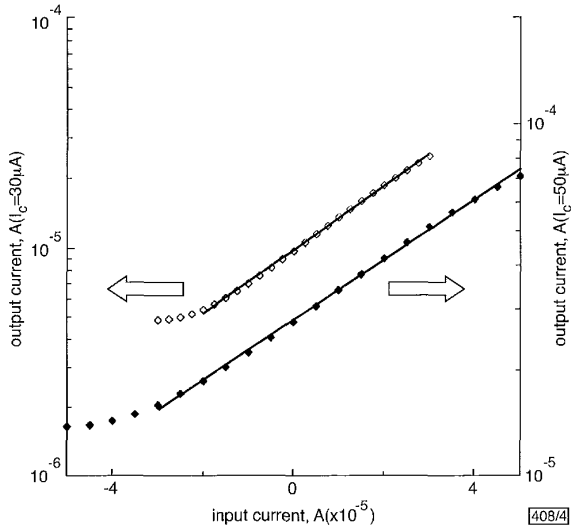

Fig. 4 *Simulated transfer curves of pseudo-exponential circuit in Fig. 2*

——— ideal curve
◇ simulated for I_C = 30μA
◆ simulated for I_C = 50μA

Conclusions: Current-mode pseudo-exponential circuits have been introduced. They are based on the approximated Taylor's series and the square-law characteristics of MOS transistors in saturation. One of the circuits has an input range that can be tuned by means of the biased current I_C, while the other has a compact structure. The simulation results confirm the feasibility of the proposed circuits. To obtain a wider output dynamic range, the pseudo-exponential circuits can be cascaded with squarers.

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Three-phase current-fed soft-switching PWM converter with auxiliary commutation inductors and resonant snubber

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A new three-phase current-fed soft-switching PWM converter is presented. This converter utilises two types of switching commutation scheme to improve the PWM current utilisation rate. It is shown by means of computer simulation that this converter has low THD and offers unity power factor correction.

Introduction: An active three-phase current-fed zero current switching (ZCS) PWM converter using a resonant DC link snubber was introduced by the authors in [1]. However, this converter suffers from the disadvantage that the PWM current is reduced during the commutation period. A new soft-switching converter topology is introduced to solve this problem. By using power source inductor commutation in addition to resonant DC link commutation, the proposed converter can achieve soft-switching operation without reducing the PWM current to such an extent. This Letter describes the operating principle of the new soft-switching scheme and the characteristics of the converter operation.

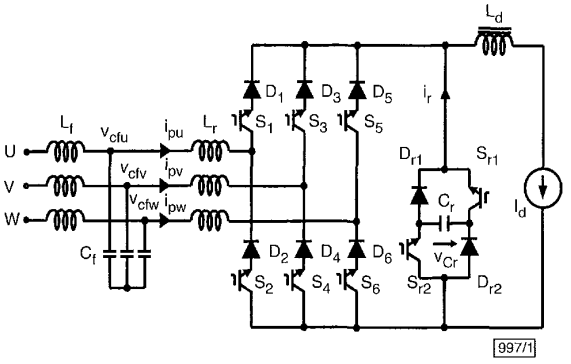

Fig. 1 *Proposed soft-switching converter*

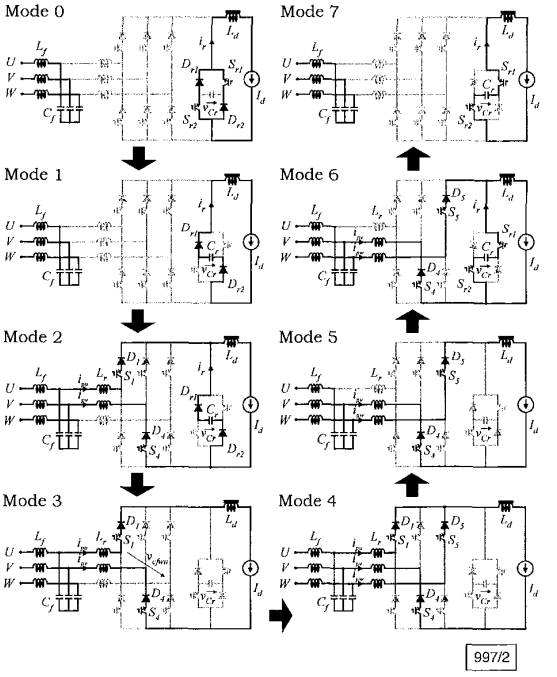

Fig. 2 *Equivalent circuit for commutation mode*

Circuit configuration: Fig. 1 shows the main power circuit configuration of the proposed three-phase current-fed PWM converter. This main power circuit bridge is constructed with the active switches composed of IGBTs (S_1-S_6) in series with reverse block-